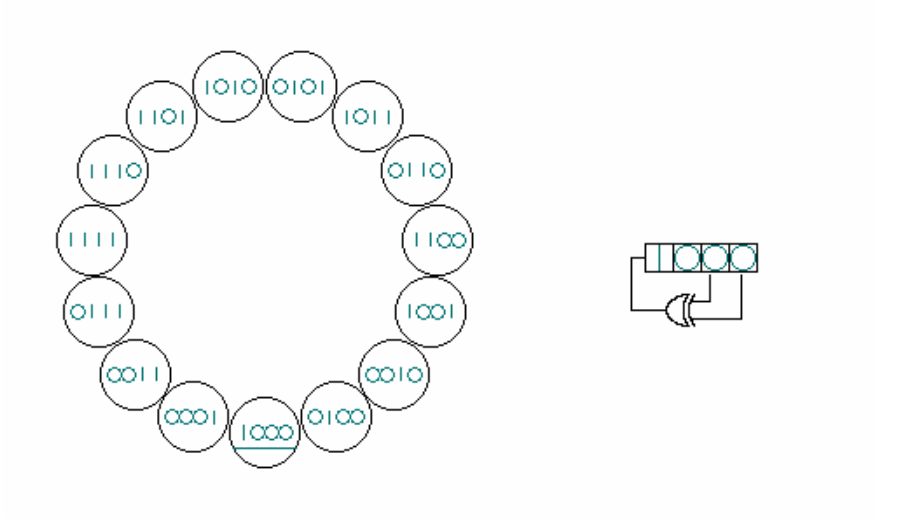
Project

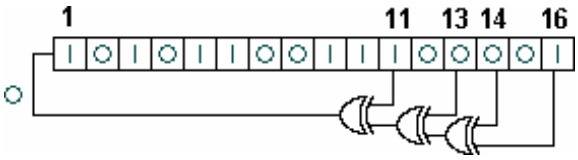
- **Pseudo Random Number Generator (PRNG)**
- **A 'counter' producing an output sequence that approximates the properties of random numbers**
- **Pseudo random sequences have many applications**
  - **Spread spectrum communication**
  - **Whitening**
  - **Monte-Carlo simulation**
  - **Stream ciphers**
  - **Test pattern generation**
  - **…**

4-bit Fibonacci LFSR



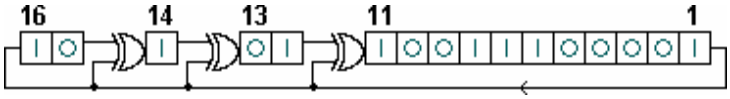
http://en.wikipedia.org/wiki/Linear_feedback_shift_register

Fibonacci vs. Galois Style



- Fibonaci

Can expect differences in speed/power tradeoff



- Galois

Requirements (partial)

- **8 bit PRNG**
- **Tap positions at 8, 6, 5, 4 for Fibonaci type**
- **Choose between Fibonacci or Galois (adapt 'taps' for Galois)**
- **Clock frequency to be specified (must use clock)**
- **Ideal non-overlapping 2-phase clock is made available**
- **90nm UMC CMOS technology**
- **10 fF load at each output**
- **Circuit – Simulation – Layout – Extraction – Spectre Simulation**

- **Deliverables (electronically):**
  - **GDS file**
  - **Poster (design report)**

Competition

- Competition: lowest power requirements
  - All will use same test bench
  - VDD is variable (design specific)
  - Area of layout is not of concern
- Final grade 50/50% project/exam
- Project: 60/40 design/poster+presentation

- Design: correctness, creativity, elegance, robustness

- Bonus points for top-n
  - 2 points for winner team
  - 1.5 points for 2nd place, 1 for 3rd, 0.5 for 4th, 5th place
  - Bonus to be added to overall mark
  - (When enough participants)

Poster, not Report

- Why is your design good
- What is special about it
- Present design decisions, trade-offs, …
- Present overall layout
- Include important schematics, waveforms, …
- Everything needed for demonstrating functionality and performance
- References/citations (!)

- 1 x A1, legible at >2m, 8 minutes
  - Easy: ppt slides, 6-up handout format enlarged
- Minimum number of words, maximum amount of information
- Poster printing will be arranged (at University)

Feel free to

- **Use any circuit style (Chapter 6)**
  - complementary CMOS, ratioed logic, DCVSL, pass-transistor logic, CPL, dynamic logic, …
    (No need to stick to style from book)
- **Any clocking scheme / Flip Flop type (Chapter 7)**
  - single phase, two phase, four phase, ...
  - Avoid Races
- **Consider any known (or unknown ☺) technique to improve power**
  - ckt level: body bias, sub-threshold logic, …,
  - design: automatic sizing, …

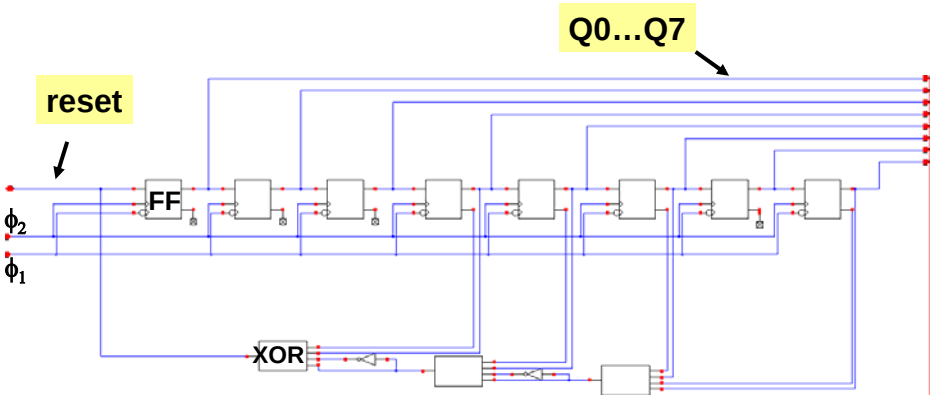
2-phase Clock

- **2-phase clock is made available, can use 1 phase if you want**
- **More advanced clock has to be derived from it**
- **Only circuit design, no layout needed for clock generation**
- **Report (poster) should show schematic, design rationale, resulting waveforms**

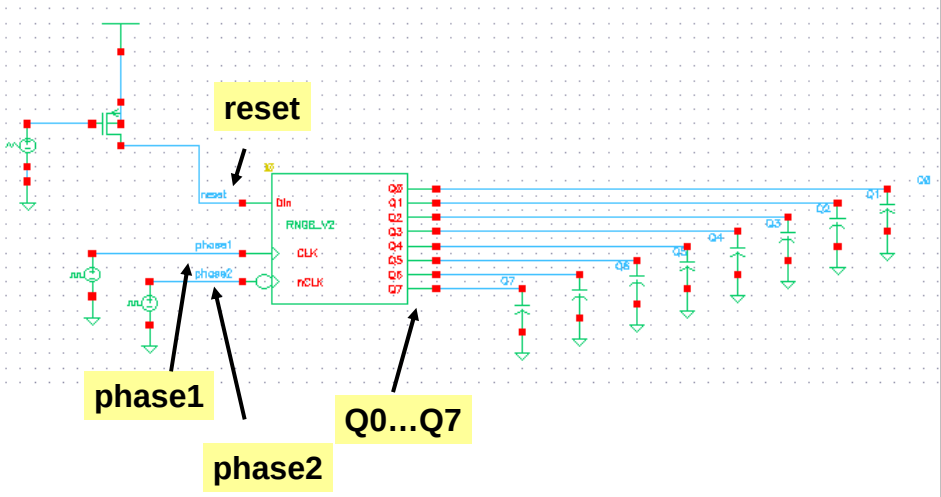
Reference Schematic

- Reference netlist is made available
- This netlist is not tuned, transistors are minimum size, topology not necessarily optimal

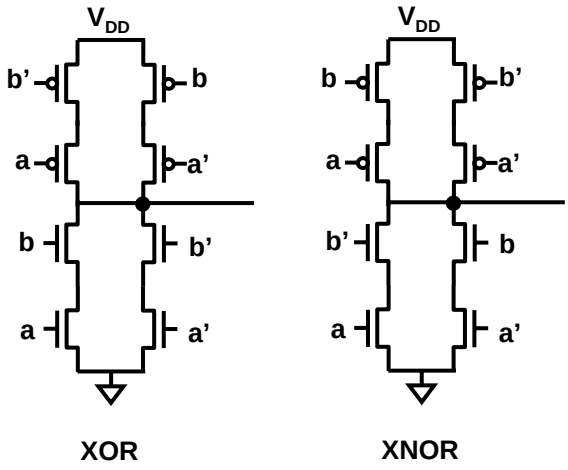
LFSR8



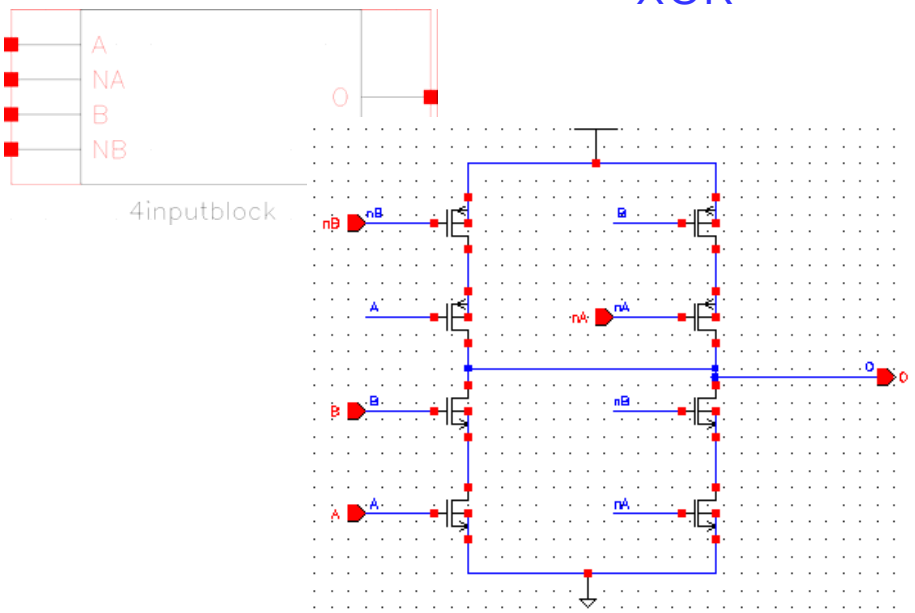
Test Bench



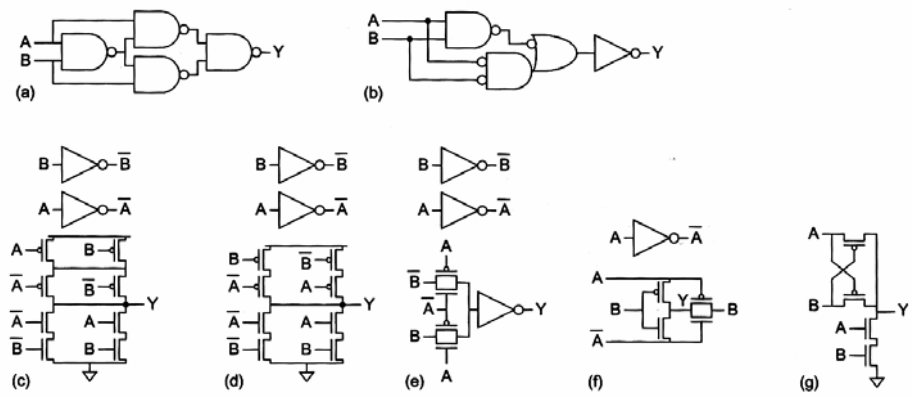
XOR – XNOR



XOR



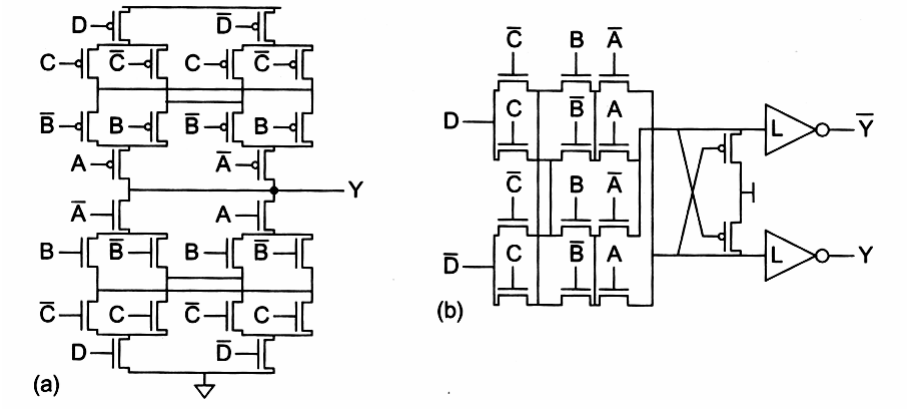
XOR-2 alternatives



[Weste/Harris]

AB=00→$V_{out} = |V_{TP}|$

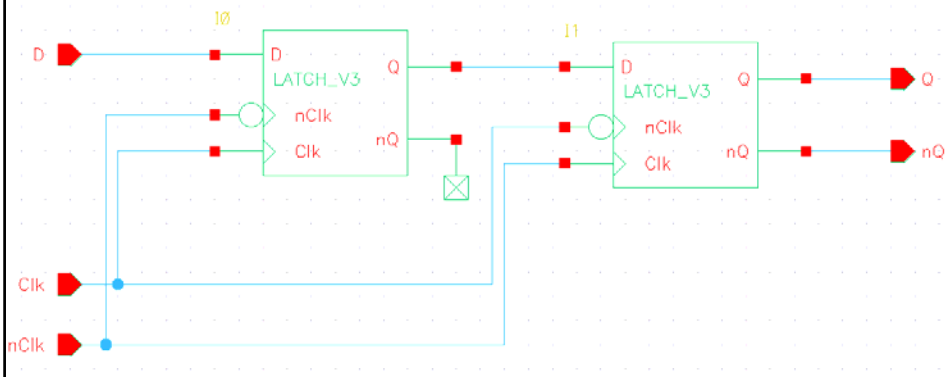
XOR-4 alternatives



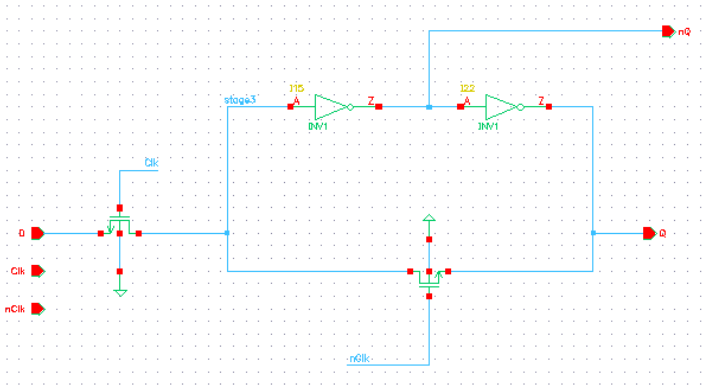
[Weste/Harris]

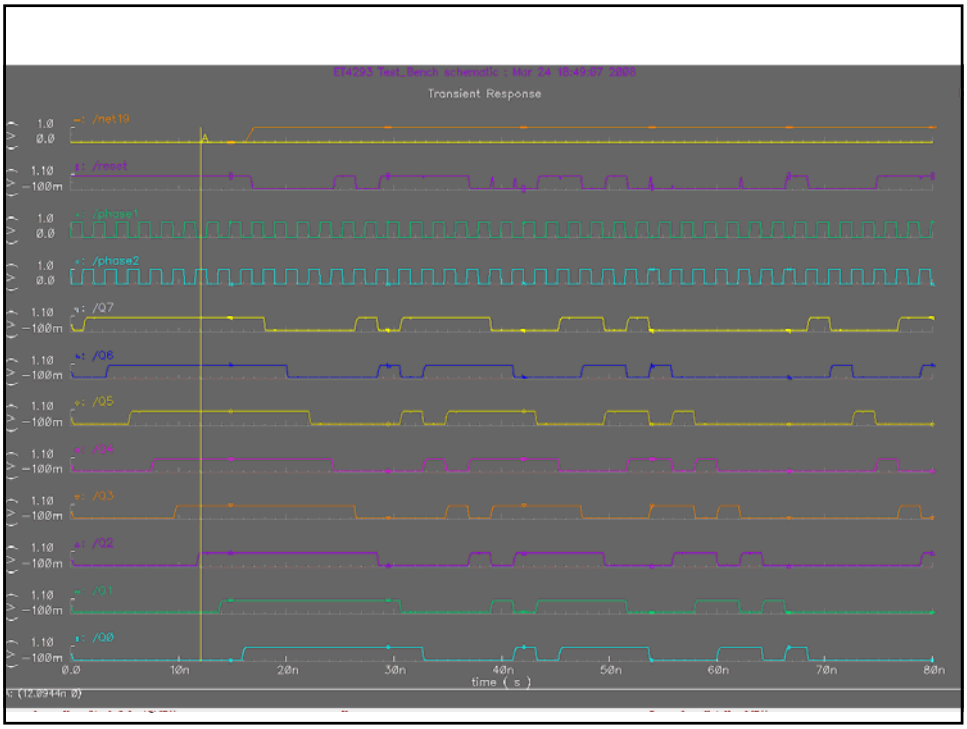
- **Can be more compact, not necessarily faster than xor2**

DFF



Latch


nQ
stage3
I15
A
Z
INV1
I22
A
Z
INV1
Clk
D
Clk
nClk
Q
nClk


Transient Response
/net19
/reset
/phase1
/phase2
/Q7
/Q6
/Q5
/Q4
/Q3
/Q2
/Q1
/Q0
1.1Ø
-1ØØm
1.Ø
Ø.Ø
Ø.Ø
1Ø0n
2Ø0n
3Ø0n
4Ø0n
5Ø0n
6Ø0n
7Ø0n
8Ø0n
time (s)