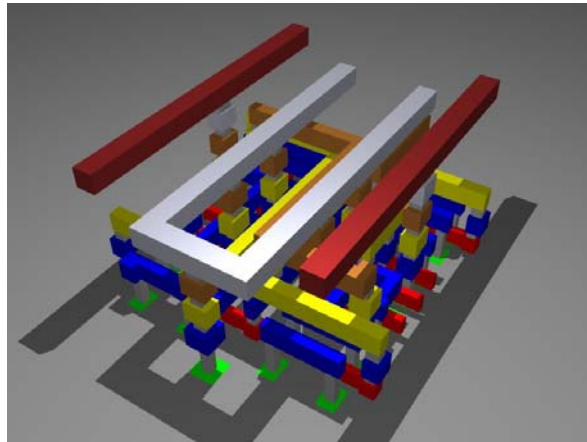


## MODULE 9

### Chapter 7



## SEQUENTIAL ELEMENTS

## Exam

- April 3<sup>rd</sup>, 9am – 12am
- Written exam, open book, also printed slides with your notes on it.
- **Prepare yourself** – eg. Rabaey exercises, book problems (answers in back)

Material	Topic	Remarks
Ch 1	Intro	Completely, pay attention to §1.3
Ch 2	Manufacturing	Only §2.1 - §2.3
Ch 3	Devices	Completely
Ch 4	Interconnect	Except §4.4.5, §4.5
Ch 5	Inverter	Completely
Ch 6	Combinational	Only §6.1, §6.2
Ch 7	Sequential	Only §7.1, §7.2

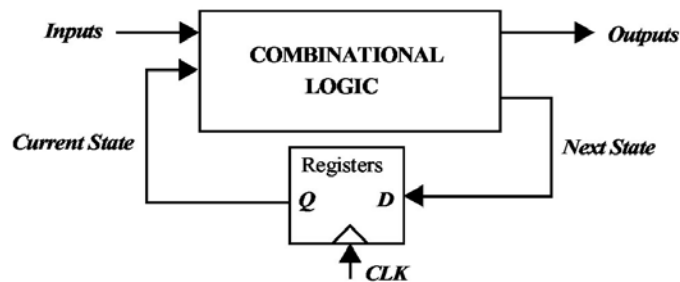
## Announcements

- Information meeting (lunch) on MSc topics@CAS section:
- Tuesday March 17, 12:30-13:30
- Next week, Wed April 2<sup>nd</sup> (tentatively): license server maintenance (it was hacked)
  - No Cadence, no ...

## Sequential Elements - Outline

- Background
  - Timing, terminology, classification
- Static Flipflops
  - Latches
  - Registers
- Dynamic Flipflops
  - Latches
  - Registers

## FSM with Positive Edge Triggered Registers



- Flip-flops provide **memory/state**
- VLSI uses predominantly **D-type flip-flops**

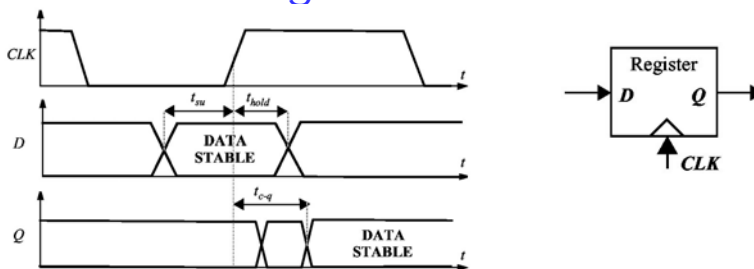
## Memory elements

- Store a **temporary value**, remember a **state**
- Typically controlled by **clock**.
- May have load signal, etc.
- In CMOS, memory is created by:
  - **capacitance** (dynamic);
  - **feedback** (static).
- Also see [http://en.wikipedia.org/wiki/Flip-flop\\_\(electronics\)](http://en.wikipedia.org/wiki/Flip-flop_(electronics))

## Variations in memory elements

- Form of required clock signal.
- How behavior of data input around clock affects the stored value.
- When the stored value is presented to the output.
- Whether there is ever a combinational path from input to output.

## Timing Metrics Reminder



$t_{c-q}$  : delay from clock (edge) to Q

$t_{su}$  : setup time

$t_{hold}$  : hold time

$t_{plogic}$  : worst case propagation delay of logic

$t_{cd}$  : best case propagation delay (contamination delay)

$T$  : clock period

$$T \geq t_{c-q} + t_{plogic} + t_{su}$$

$$t_{cdregister} + t_{cdlogic} \geq t_{hold}$$

## Latches vs. Registers

### Latch

**Level-sensitive**

**Transparent** when clock is active

Clock active high: **positive** latch

Clock active low: **negative** latch

**Faster, smaller**

### Register

**Edge-triggered**

Input and output **isolated**

Sampling on 0 → 1 clock: **positive edge triggered**

Sampling on 1 → 0 clock: **negative edge triggered**

**Safer**

## Static vs. Dynamic Memory Elements

### Static

Operate through **positive feedback**

**Preserve state** as long as power is on

Can work when clock is **off**

More **robust**

### Dynamic

**Store charge** on (parasitic) capacitor

Charge **leaks** away (in milliseconds)

Clock must be kept **running** (for periodic refresh)

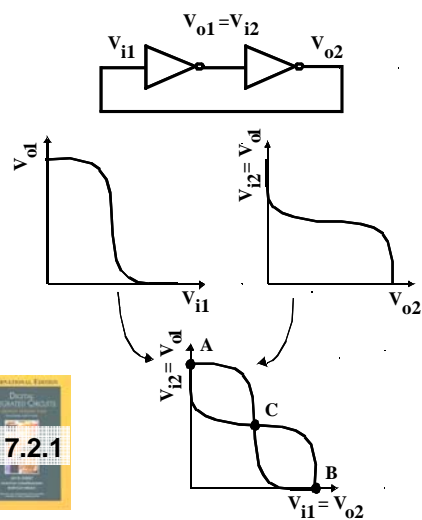
**Faster, smaller**

## Static Flipflops

### ■ Latches

### ■ Registers

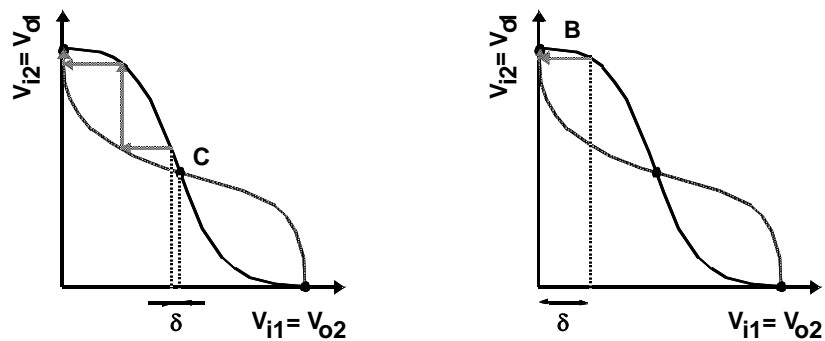
## Positive Feedback: Bi-Stability



- Loop-gain in A,B  $\ll 1$
- A,B: **stable** points
- Loop-gain in C  $\gg 1$
- C: **meta-stable** point



## Meta-Stability



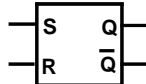
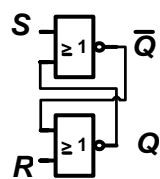
- Gain should be **larger than 1** in the transition region
- **Smaller than 1** in stable region

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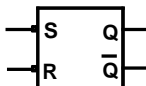
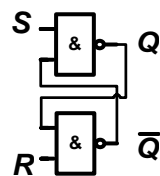
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## SR-Latch



S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

← forbidden



S	R	Q	$\bar{Q}$
1	1	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

← forbidden



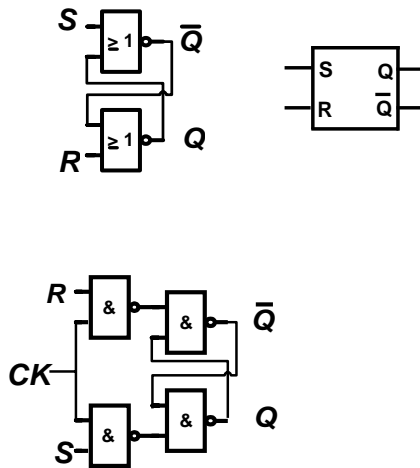
- Construction of **D-latch**
- D-latch **most common in VLSI**

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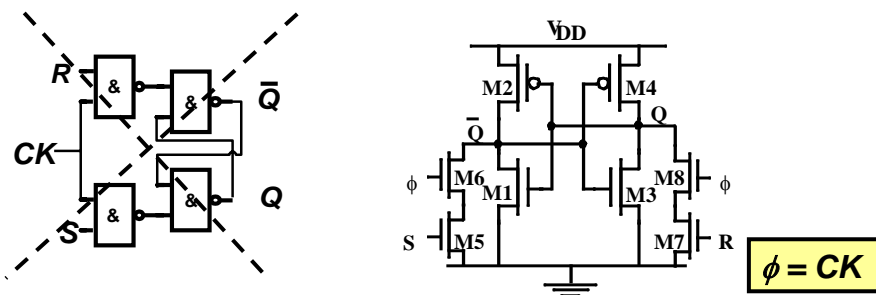
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## Clocked SR-Latch



- Naïve implementation
- 16 transistors
- D latch requires 9xN, 9xP
- Master-slave D-register needs 18xN, 18xP
- Larger area, cost, power

## CMOS Clocked SR-Latch



- Save 6 (incl. 4 large) PMOS transistors and 2 NMOS
- D-latch requires 7 x N, 3 x P (instead of 9xN, 9xP)

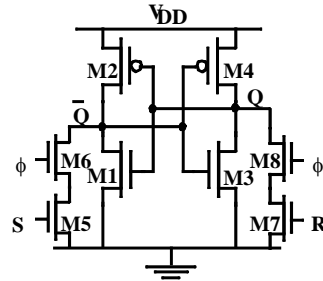
**Q:** Is this a **ratioed** design or not?  
Does it consume static power?





## Sizing for 'Set' Action

- $M_3$ - $M_4$  form conventional inverter
- Model  $M_5$ - $M_6$  as one equivalent (double length) transistor  $M_{56}$
- Assume  $Q = 0 \rightarrow M_1$  is off,  $M_2$  is on
- $M_2$ - $M_{56}$  operate like ratioed pseudo NMOS inverter
- Latch switches when  $M_{56}$  pulls input of  $M_3$ - $M_4$  below their switching threshold (assume  $V_{DD}/2$ )
- Positive feedback amplifies switching
- $M_2$  and  $M_{56}$  both in velocity saturation around  $V_Q = V_{DD}/2$



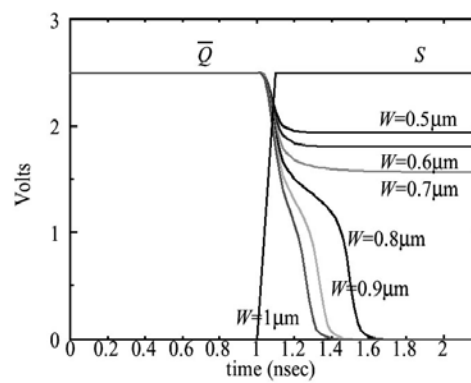
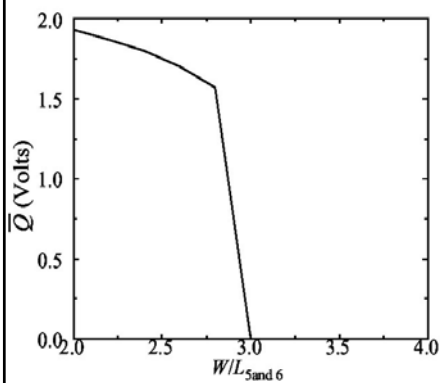
$$k'_n \left( \frac{W}{L} \right)_{5-6} \left( (V_{DD} - V_{Tn}) V_{DSATn} - \frac{V_{DSATn}^2}{2} \right) = k'_p \left( \frac{W}{L} \right)_2 \left( (-V_{DD} - V_{Tp}) V_{DSATp} - \frac{V_{DSATp}^2}{2} \right)$$

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## Sizing for 'Set' Action

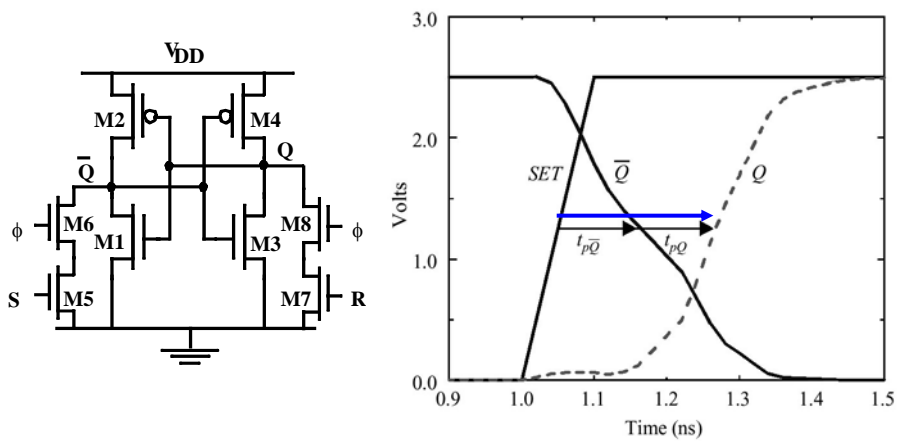


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## SR Latch Timing

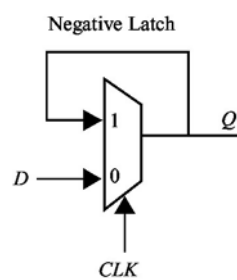


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## Multiplexer-Based Latches

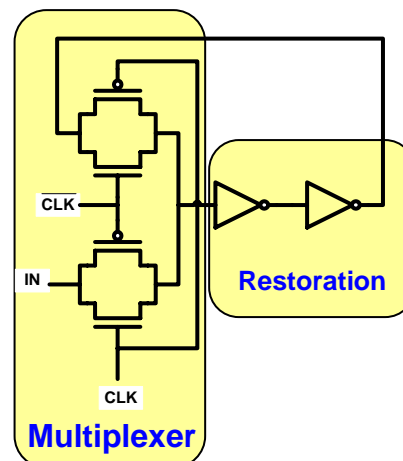


### Recirculating latch



§ 7.2.2

Mux-based latches much more common in modern dig. IC's

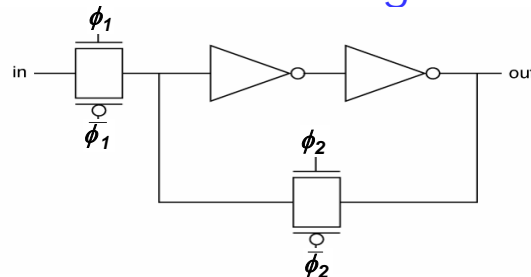


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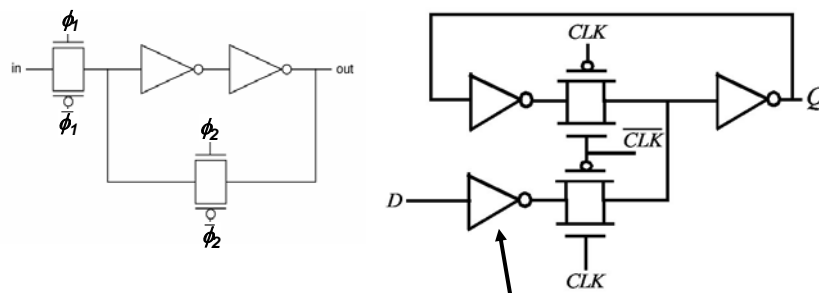
20

## Recirculating latch



- **Quasi-static**, static on one phase
- Feedback **restores** value
- Requires 4 x N, 4 x P, minimum size  
(compare 7 x N, 3 x P, non-minimum size)
- $\phi_1$  and  $\phi_2$  inverse but should be non-overlapping
- Can suffer from **charge sharing** (when  $\phi$  not non-overlapping)
  - Output connected directly to input
  - $C_{in}$  and  $C_{load}$  form communicating vessels

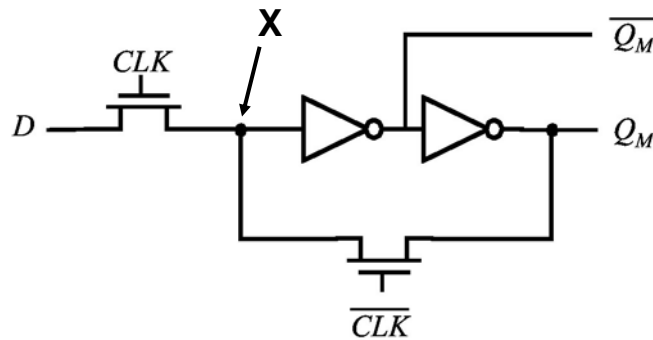
## Insensitive for Charge Sharing



- **Non ratioed**
- **High load to CLK**

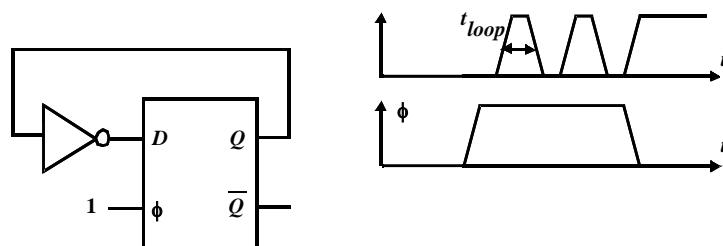
Uni-directionality of this inverter prevents coupling between Q and D

## Recirculating NMOS Latch.



- Degraded 1 at X
- Lower noise margin, higher delay, power

## Latch Designs can Suffer from Race Problems

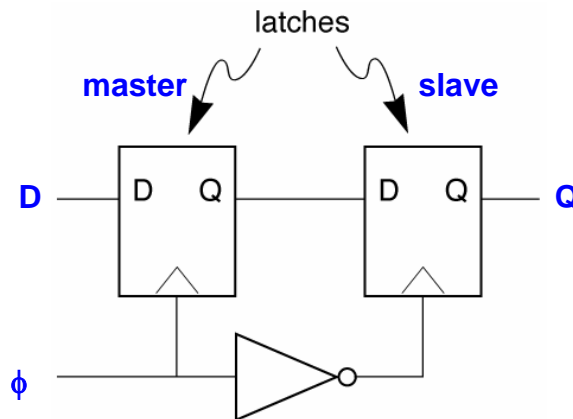


Signal can **race around** during  $\phi = 1$



## Registers

- Not transparent—use multiple storage elements to isolate output from input.
- Master-slave, edge triggered principle

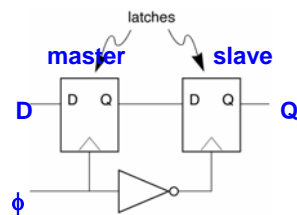


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## Master-slave operation



$\phi = 0$ :

- master latch is disabled;
- slave latch is enabled,
- but master latch output is stable,
- so output does not change.

$\phi = 1$ :

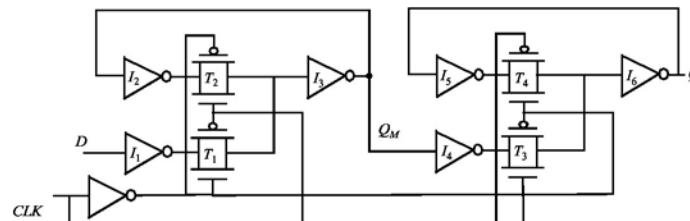
- master latch is enabled,
- loading value from input;
- slave latch is disabled,
- maintaining old output value.

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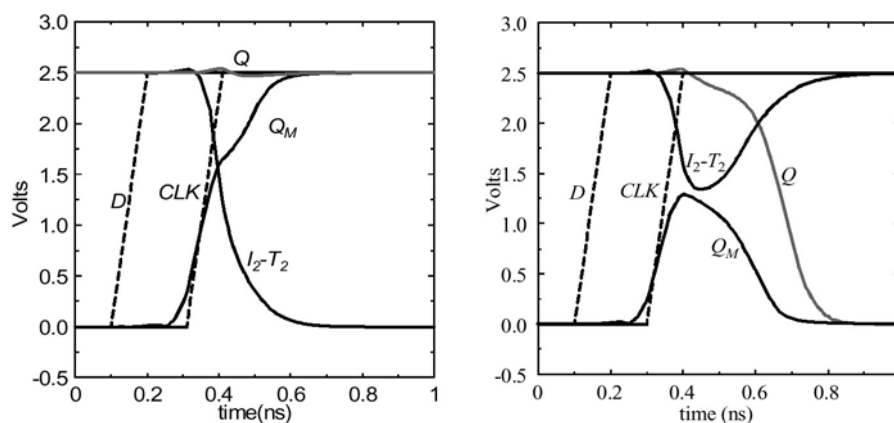
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## Transistor Level Master Slave Positive Edge Triggered Register



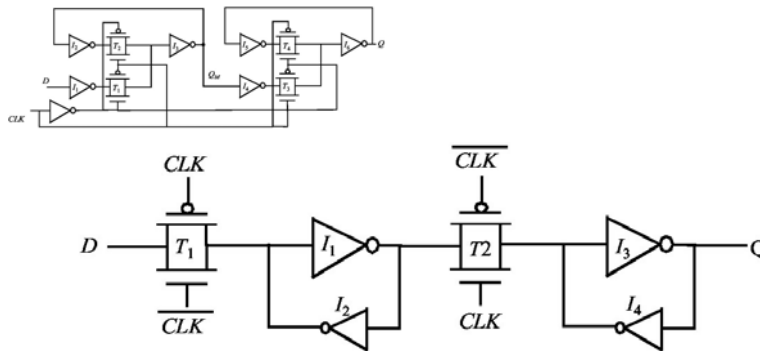
- Robust Design
- Can eliminate  $I_1$  and  $I_4$ , however, they make design more robust (avoid charge sharing, robust input)
- High Clock Load (8 x)

## Set-up Time Simulation



**Slightly smaller delay  
between D and CLK**

## Ratioed Reduced Clock Load Register



- $I_2$  and  $I_4$  are small, even long
- Lower clock load
- Increased design complexity
- Reduced robustness (reverse conduction)

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CMOS Flip-Flop Construction - Microsoft Internet Explorer

File Edit View Favorites Tools Help

Back Forward Stop Search Favorites Go Links

Address [http://www.play-hookey.com/digital/cmos\\_d\\_flip-flop.html](http://www.play-hookey.com/digital/cmos_d_flip-flop.html)

## CMOS Flip-Flop Construction

CMOS technology allows a very different approach to flip-flop design and construction. Instead of using logic gates to connect the clock signal to the master and slave sections of the flip-flop, a CMOS flip-flop uses *transmission gates* to control the data connections. (See the [CMOS gate electronics page](#) for a closer look at the transmission gate itself.)

The result is that a controllable flip-flop can be built with only inverters and transmission gates — a very small and simple structure for an IC.

The basic CMOS D flip-flop is shown below.

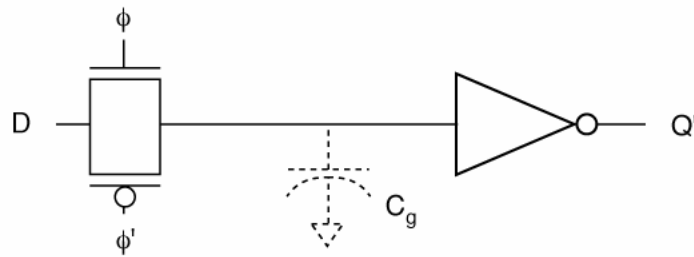
[www.play-hookey.com](http://www.play-hookey.com)

clickable

Internet

## Dynamic latch

Stores charge on inverter gate capacitance:

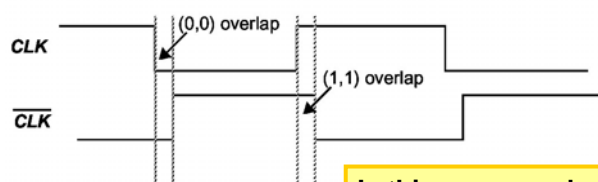
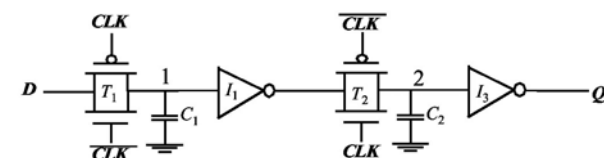


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## Dynamic Edge Triggered Register



Is this a + or - edge triggered reg?

$t_{su}$

$t_{hold}$

$t_{cq}$

$t_{overlap\ 0-0}$

$t_{hold}$

$t_{T1}$

approximately zero

$t_{I1} + t_{T2} + t_{I3}$

$< t_{T1} + t_{I1} + t_{T2}$

$> t_{overlap\ 1-1}$

Prevent race through  $T_1, I_1, T_2$

Enforce hold-time constraint

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## Summary

- **Background**
  - Timing, terminology, classification
- **Static Flipflops**
  - Latches
  - Registers
- **Dynamic Flipflops**
  - Latches
  - Registers