Power

- Dynamic Power
- Static Power
- Metrics

www.quitpc.com

24 hours audio playback time

CMOS Power Dissipation

- Power dissipation is a very important circuit characteristic
- CMOS has relatively low static dissipation
- Power dissipation was the reason that CMOS technology won over bipolar and NMOS technology for digital IC's
- (Extremely) high clock frequencies increase dynamic dissipation
- Low V_T increase leakage
- Advanced IC design is a continuous struggle to contain the power requirements!

Power Density

Estimate

- **Furnace: 2000 Watt, r=10cm ➔ P ≈ 6Watt/cm^2**
- **Processor chip: 100 Watt, 3cm^2 ➔ P ≈ 33Watt/cm^2**

Power-aware design, design for low power, is blossoming subfield of VLSI Design

Where Does Power Go in CMOS

- **Dynamic Power Consumption**
  - **Charging and discharging capacitors**
- **Short Circuit Currents**
  - **Short circuit path between supply rails during switching (NMOS and PMOS on together)**
- **Leakage**
  - **Leaking diodes and transistors**
  - **May be important for battery-operated equipment**

Dynamic Power

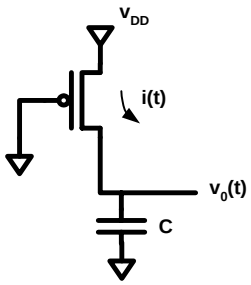
Dynamic Power

- E_i = energy of switching event i
  - independent of switching speed
  - depends on process, layout
- Power = Energy/Time

$$P = \frac{1}{T}\sum_i E_i$$

- E_i = Power-Delay-Product P-D
  - important quality measure
- Energy-Delay-Product E-D
  - combines power∗speed performance

Low-to-High Transition Energy



Equivalent circuit for low-to-high transition

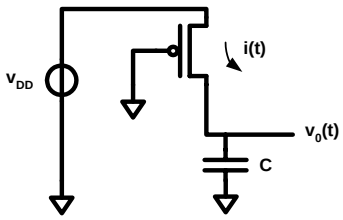
E_C - Energy stored on C

$$E_C = \int_0^\infty i v_0 dt \qquad v_0 = v_0(t) \qquad i = i(t) = C\frac{dv_0}{dt}$$

$$= \int_0^\infty C v_0 \frac{dv_0}{dt} dt$$

$$= \int_0^{V_{DD}} C v_0 dv_0 = \frac{1}{2} C v_0^2 \Big|_0^{V_{DD}} = \frac{1}{2} C V_{DD}^2$$

Low-to-High Transition Energy



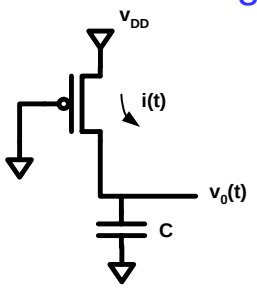
$E_{V_{DD}}$ **Energy delivered by supply**

$$E_{V_{DD}} = \int_0^\infty i(t) V_{DD} dt = \int_0^{V_{DD}} C V_{DD} \frac{dv_0}{dt} dt = C V_{DD}^2$$

$$E_{V_{DD}} = C V_{DD}^2 \qquad E_c = \frac{1}{2} C V_{DD}^2$$

Where is the rest?

Low-to-High Transition Energy



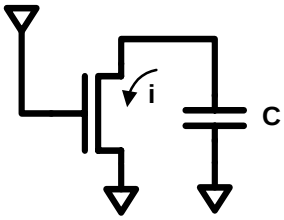
E_{diss} **Energy dissipated in transistor**

$$E_{diss} = \int_0^\infty i(V_{DD} - v_0) dt$$

$$= \int_0^\infty i V_{DD} dt - \int_0^\infty i v_0 dt$$

$$= E_{V_{DD}} - E_c$$

High-to-Low Transition Energy



Equivalent circuit

Exercise: Show that the energy that is dissipated in the transistor upon discharging C from V_{DD} to 0 equals $E_{diss} = ½CV_{DD}^2$

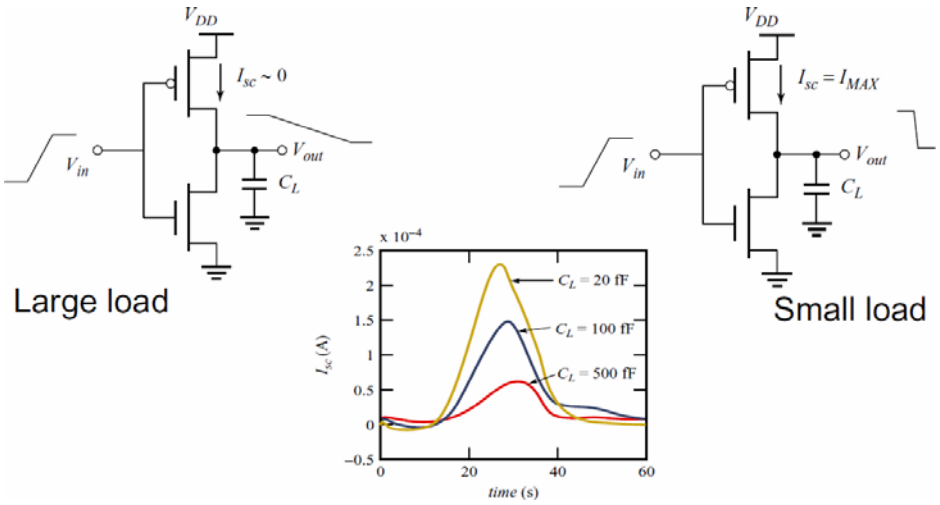
CMOS Dynamic Power Dissipation

$$Power = \frac{Energy}{Time} = \frac{Energy}{transition} \times \frac{\#\,transitions}{time}$$

$$= CV_{DD}^2 \times f$$

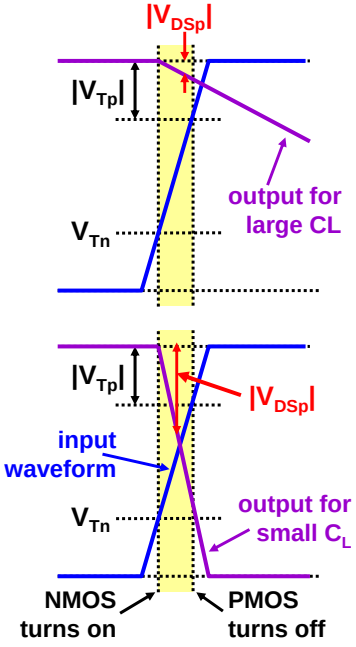
- Independent of transistor on-resistances
- Can only reduce *C*, V_{DD} or *f* to reduce power

Short Circuit Current



Best to maintain approximately equal input/output slopes

Short Circuit Current

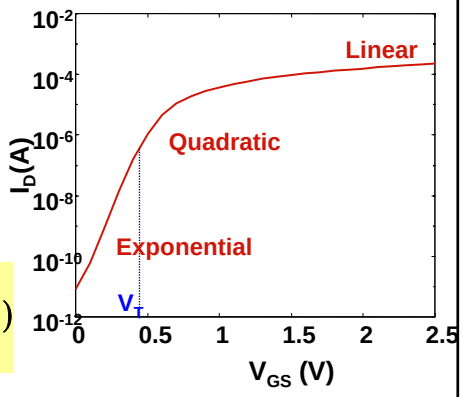


- **Input** and **output** waveforms of inverter loaded with a large capacitance (top) and with a small capacitance (bottom).
- **Shaded area** is where both pull-up and pull-down transistors are on (this is when short-circuit current can exist). This region is determined by crossings of input waveform with V_{Tn} and V_{DD}-$|V_{Tp}|$.
- Short-circuit current increases with $|V_{DSp}|$. This is clearly much larger for small C_L compared to large C_L.
- Similarly, short-circuit current can exist for low-to-high transition at output.

Leakage

- **Leakage current of reverse biased S/D junctions**
- **Sub-threshold current of MOS devices**
  - **no channel ➔ parasitic bipolar device: n+ (source) – p (bulk) – n+ (drain)**
  - **Important source of leakage**

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right)\left(1 + \lambda \cdot V_{DS}\right)$$



Sub-Threshold Current

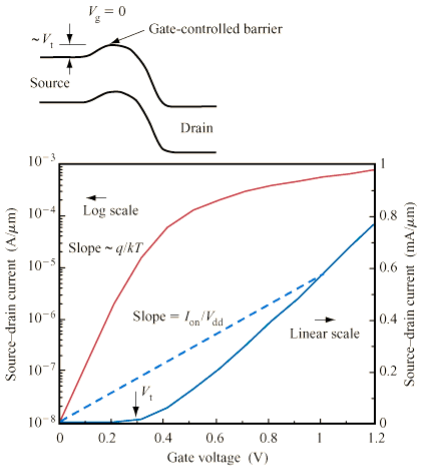


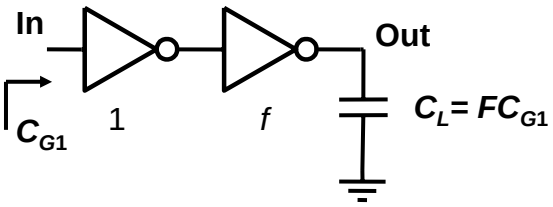
Figure 2

MOSFET current in both logarithmic (left) and linear (right) scales vs. gate voltage. The slope of the dotted line represents the large-signal transconductance for a digital circuit. Inset shows the band diagram of an n-MOSFET. The barrier height at $V_g = 0$ is proportional to V_t.

- **Rapidly becomes bottleneck with lowering threshold voltages**
- **Modern technologies offer low-Vt and hi-Vt devices Balance speed and power**

Y. Taur, CMOS design near the limit of scaling, IBMJRD, Volume 46, Numbers 2/3, 2002

Transistor Sizing for Minimum Energy



- Goal: Minimize Energy of whole circuit
  - Design parameters: f and V_{DD}
  - $t_p \leq t_{pref}$ of circuit with $f = 1$ and $V_{DD} = V_{ref}$

$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right)$$ (For this particular case of N=2)

$$t_{p0} \propto \frac{V_{DD}}{V_{DD}-V_{TE}}$$

See Eq. 5.21

$V_{TE} = V_T - \frac{1}{2}V_{DSAT}$: Effective V_T

Transistor Sizing (2)

$$t_p = t_{p0}\left(\left(1+\frac{f}{\gamma}\right)+\left(1+\frac{F}{f\gamma}\right)\right) \qquad t_{p0} \propto \frac{V_{DD}}{V_{DD}-V_{TE}}$$

Performance Constraint ($\gamma = 1$):

$$\frac{t_p}{t_{pref}} = \frac{t_{p0}}{t_{p0ref}}\frac{\left(2+f+\frac{F}{f}\right)}{(3+F)} = \frac{V_{DD}}{V_{ref}}\frac{V_{ref}-V_{TE}}{V_{DD}-V_{TE}}\frac{\left(2+f+\frac{F}{f}\right)}{(3+F)} = 1$$

Energy for single Transition:

$C_{g1} + C_{int}$ — Size of 1st + 2nd inverter

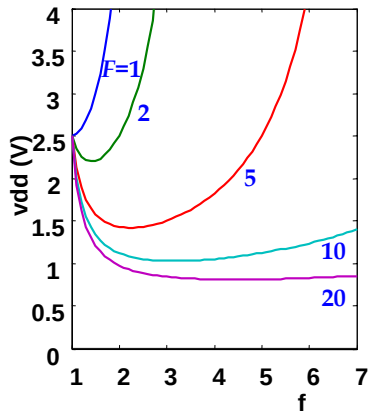
$$E = V_{DD}^2 C_{g1}\left[(1+\gamma)(1+f)+F\right]$$

$C_L = FC_{G1}$

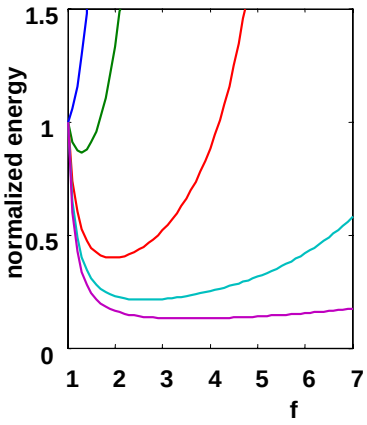
$$\frac{E}{E_{ref}} = \left(\frac{V_{DD}}{V_{ref}}\right)^2\left(\frac{2+2f+F}{4+F}\right)$$

Transistor Sizing (3)

V_{DD}=f(f)



E/E_{ref}=f(f)

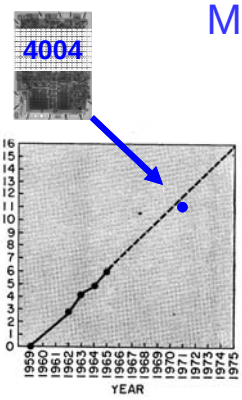


- Device sizing is effective
- Oversizing is expensive for power
- Optimal sizing for energy slightly different from sizing for performance

Technology Scaling

Also see: IBM JRD, Vol 46, no 2/3, 2002
Scaling CMOS to the limit
http://www.research.ibm.com/journal/rd46-23.html

Moore's Law



The number of transistors that can be integrated on a single chip will double every 18 months

Gordon Moore, co-founder of Intel [Electronics, Vol 38, No. 8, 1965]

Why Scaling

- Reduce **price per function**:
  - Want to sell more functions (transistors) per chip for the same money ➔ **better products**
  - Build same products cheaper, sell the same part for less money ➔ **larger market**
  - Price of a transistor has to be reduced
- But also want to be **faster, smaller, lower power**

Scaling Models

Fixed Voltage Scaling

- most common model until 1990's
- only dimensions scale, voltages remain constant

Full Scaling (Constant Electrical Field)

- ideal model — dimensions and voltage scale together by the same factor S

General Scaling

- most realistic for today's situation —
- voltages and dimensions scale with different factors

Scaling for Velocity Saturated Devices

Constant Field Scaling: S = U

Parameter	Relation	General Scaling
W, L, t_{ox}		1/S
V_{DD}, V_T		1/U
N_{SUB}	V / W_{depl}^2	S^2/U
Area / Device	WL	$1/S^2$
C_{ox}	$1/t_{ox}$	S
C_{gate}	C_{ox} W L	1/S
k_n, k_p	C_{ox} W / L	S
I_{sat}	C_{ox} W V	1/U
Current Density	I_{sat} / Area	S^2/U
R_{on}	V / I_{sat}	1
Intrinsic Delay	$R_{on} C_{gate}$	1/S
Power / Device	I_{sat} V	$1/U^2$
Power Density	P / Area	S^2/U^2

IC Technology Scaling

Scaling improves density and performance

- First order scaling theory

		2008 / 1971
dimensions,	1/S	0.007
voltages	1/S	0.007
intrinsic delay	1/S	0.007
power per transistor	$1/S^2$	0.00004

- Scaling trend

1971 S=1 (10μm) first μproc

1982 S≈5

2008 S≈150 (65nm)

2010 S≈200

Technology Practice & ITRS

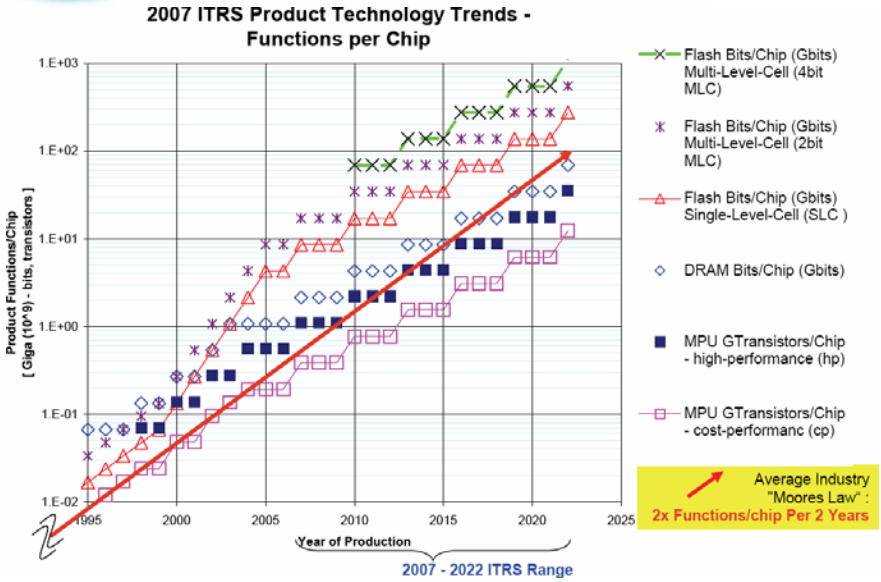
- Scaling – Technology Generations
- $S \approx 1.4 \approx 2^{0.5}$ per generation
- … – 250 – 180 – 130 – 90 – 65 – 45 – 35 – 22 – … nm

- ITRS: International Technology Roadmap for Semiconductors
  Industry-wide organization for forecasting technology developments – and (planning) requirements

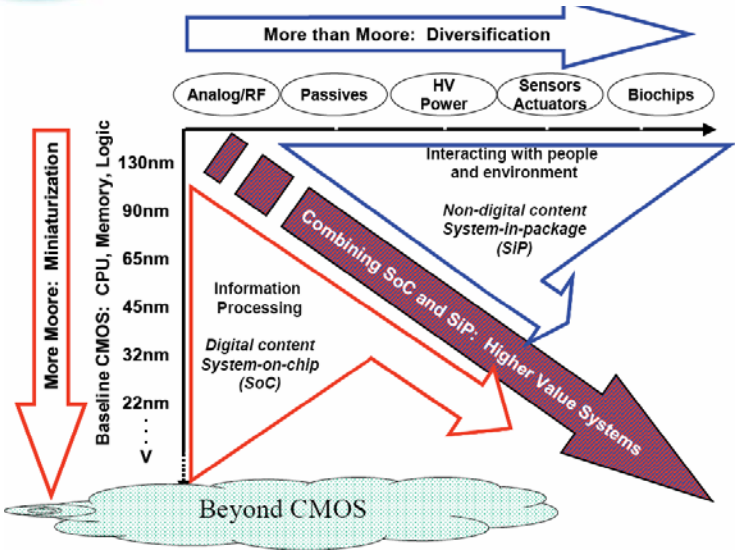
http://www.itrs.net/home.html

Not really – it is more like science
(and a self-fulfilling prophecy at the same time)

International Technology Roadmap for Semiconductors



International Technology Roadmap for Semiconductors



Summary

- Digital Gate Characterization (§ 1.3)
- Static Behavior (Robustness) (§ 5.3)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance) (§ 5.4)
  - Capacitances
  - Delay
- Power (§ 5.5)
  - Dynamic Power, Static Power, Metrics
- Scaling (§ 5.6)