CMOS INVERTER
dynamic behavior (performance)

- **Capacitances**
- **(Dis)charge times**
- **Delay**

- **Before: propagation delay analysis**

$$t_p \approx 0.69 \times \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)C_L$$

- **Next: propagation delay**
  from a design perspective
  inverter sizing

Reducing t_p

$$t_{pHL} \approx 0.69 \times \frac{3}{4}\frac{V_{DD}}{I_{DSAT_n}}\left(1-\frac{5}{6}\lambda V_{DD}\right)C_L$$

$$I_{DSAT} = k'\frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT}-\frac{1}{2}V_{DSAT}^2\right]$$

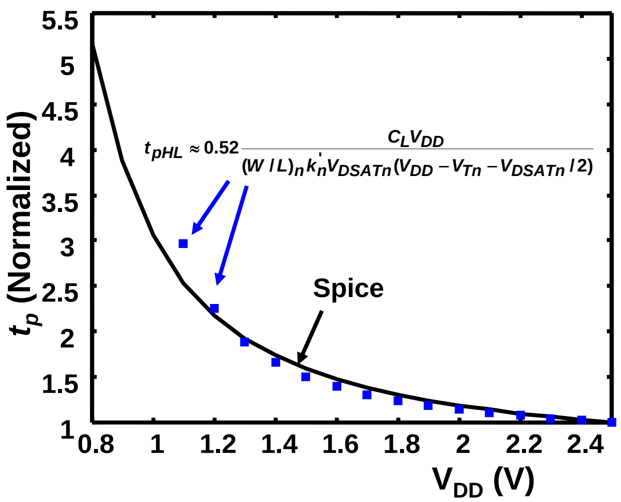
λ=0 $\Rightarrow$

$$t_{pHL} \approx 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD}-V_{Tn}-V_{DSATn}/2)}$$

Propagation Delay t_p can be reduced by

- **Increasing V_{DD} (until $V_{DD} >> V_T + V_{DSAT}/2$)**
- **Increasing W**
- **Reducing C_L**

Delay as a function of V_{DD}



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Sizing

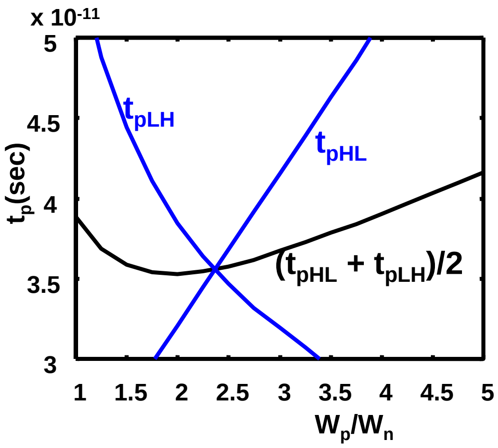
Propagation Delay t_p can be reduced by

- Increasing V_{DD} (until $V_{DD} >> V_T + V_{DSAT}/2$)
- **Increasing W**
- **Reducing C_L**

$$t_{pHL} = 0.52 \frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)} \propto \frac{C_L}{W}$$

- **C_L can be reduced by good layout design**
- **But part of C_L depends on W!**

t_p as a function of W_p/W_n

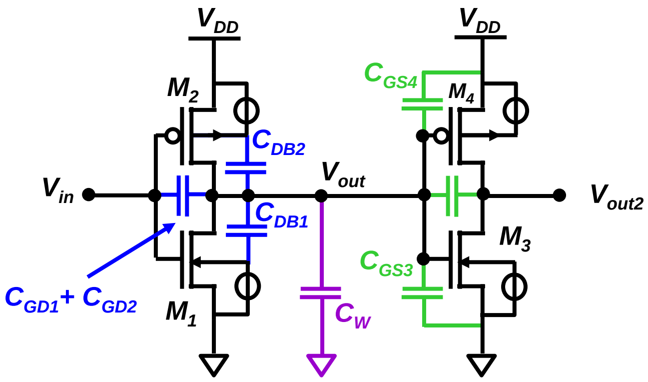


$W_n\uparrow \begin{cases} \Rightarrow I_{pd}\uparrow \Rightarrow t_{pHL}\downarrow \\ \Rightarrow C_D\uparrow \Rightarrow t_{pLH}\uparrow \end{cases}$

$W_p\uparrow \begin{cases} \ldots \\ \ldots \end{cases}$

Min t_p in general not when $t_{pLH} = t_{pHL}$
Save area, time at expense of robustness

Intrinsic vs Extrinsic vs Parasitic Load Cap



- $C_{int} = C_{DB1} + C_{DB2} + 2(C_{GD1} + C_{GD2})$ — **Intrinsic load**
- $C_{ext} = C_{GS3} + C_{GS4} + C_{GD3} + C_{GD4}$ — **Extrinsic / fan-out load**
- $C_{par} = C_w$ — **Parasitic load**

Isolated Inverter Sizing

$$t_p = 0.69 R_{eq}(C_{int} + C_{ext}) = 0.69 R_{eq} C_{int}\left(1 + \frac{C_{ext}}{C_{int}}\right)$$

Assume C_{par} can be ignored or its effect can be absorbed in other C

R_0: resistance of minimum size inverter (assume proper $\beta = W_p / W_n$ ratio)

C_0: intrinsic load (output, drain) cap of min. size inverter

$t_{p0} = 0.69\ R_0C_0$:
intrinsic or unloaded delay
basic time constant for technology
minimum delay possible in technology given V_{DD}

S: sizing factor for W_n, W_p of driving inverter
$W_n = S\ W_{min}$, $W_p = S\ \beta\ W_{min}$

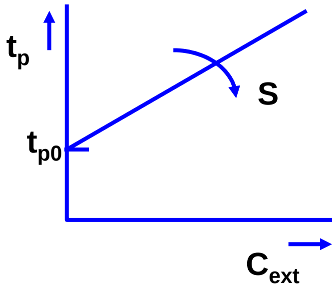
➔ $R_{eq} = R_0 / S$ $\quad C_{int} = SC_0$

$$\Rightarrow t_p = t_{p0}\left(1 + \frac{C_{ext}}{SC_0}\right)$$

Isolated Inverter Sizing

$$t_p = t_{p0}\left(1 + \frac{C_{ext}}{SC_0}\right)$$

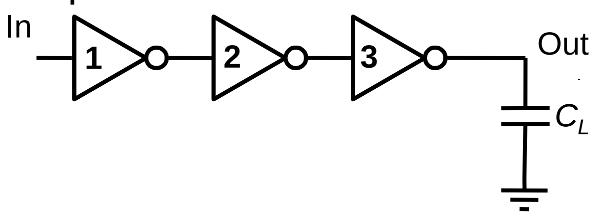
Increasing S reduces delay until $SC_0 >> C_{ext}$



Inverter Chain

Assume sizes of inverter 1 and 3 are fixed.

- ☺ **Increasing S of inverter 2 reduces t_p of inverter 2**
- ☹ **But it increases t_p of inverter 1 (higher load cap)**
- ☺ **Expect an optimum!**



If C_L is given:
- How many stages are needed to minimize the delay?
- How to size the inverters?

Inverter Chain

Assume size of inverter 1 is fixed.

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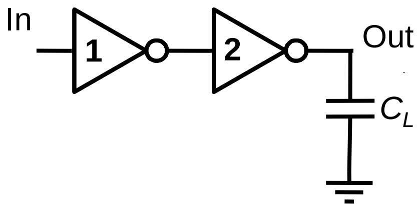
☺ **Expect an optimum!**



If C_L is given:

- How many stages are needed to minimize the delay?

- How to size the inverters?

Delay Formula

$$t_p = t_{p0}\left(1 + \frac{C_{ext}}{SC_0}\right) = t_{p0}\left(1 + \frac{f}{\gamma}\right)$$

C_{gin} input gate capacitance

$\gamma = C_{int}/C_{gin} = SC_0/C_{gin}$

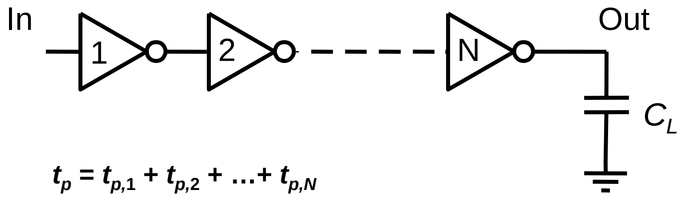
self loading coefficient

property of technology, typically $\gamma \approx 1$

$f = C_{ext}/C_{gin}$ effective fanout

$$\frac{f}{\gamma} = \frac{C_{ext}}{\cancel{C_{gin}}} \times \frac{\cancel{C_{gin}}}{SC_0}$$

Apply to Inverter Chain



$t_p = t_{p,1} + t_{p,2} + \ldots + t_{p,N}$

$$t_{p,j} = t_{p0}\left(1 + \frac{f_j}{\gamma}\right) = t_{p0}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right), \quad C_{gin,N+1} = C_L$$

Apply to Inverter Chain

Delay equation has N-1 unknows, $C_{gin,2}$ … $C_{gin,N}$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right), \quad C_{gin,N+1} = C_L$$

Make N-1 partial derivatives for $C_{gin,j}$ zero for minimization:

$$\frac{\partial t_p}{\partial C_{gin,j}} = t_{p0}\left(\frac{1}{\gamma C_{gin,j-1}} - \frac{C_{gin,j+1}}{\gamma (C_{gin,j})^2}\right) = 0, \quad j = 2 \ldots N-1$$

Size of each stage is geometric mean of 2 neighbors:

$$\boxed{C_{gin,j} = \sqrt{C_{gin,j-1} \times C_{gin,j+1}}, \quad j = 2 \ldots N-1}$$

Optimal Tapering for Given N

Size of each stage is geometric mean of 2 neighbors:

$$\boxed{C_{gin,j} = \sqrt{C_{gin,j-1} \times C_{gin,j+1}}, \quad j = 2 \ldots N-1}$$

$$\Rightarrow \quad C_{gin,j}^2 = C_{gin,j-1} \times C_{gin,j+1}$$

$$\Rightarrow \quad \frac{C_{gin,j}}{C_{gin,j-1}} = \frac{C_{gin,j+1}}{C_{gin,j}}$$

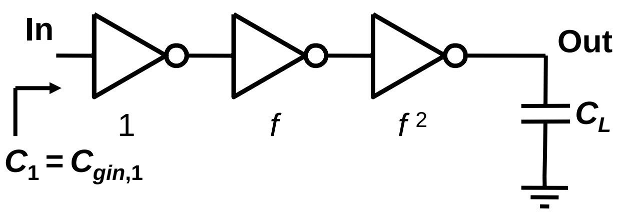
Load cap / input cap ratio same for each stage

$$\Rightarrow \quad f_j = \frac{C_{gin,j+1}}{C_{gin,j}} = \sqrt[N]{\frac{C_L}{C_{gin,1}}} = \sqrt[N]{F}$$

$F = C_L/C_{gin,1}$: path fan-out. Same fan-out, same delay for each stage.

$$\Rightarrow \quad \boxed{t_{p,j} = t_{p0}\left(1 + \frac{f_j}{\gamma}\right) = t_{p0}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right) = t_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)}$$

Optimal Tapering for Fixed-N Summary

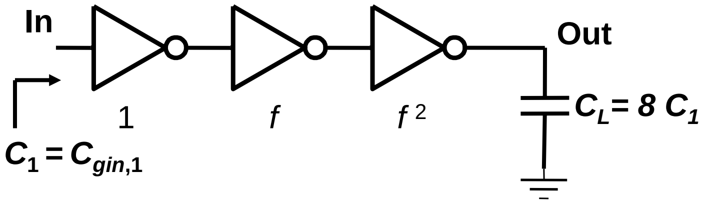


Delay per stage and total Path Delay

$$\boxed{t_{p,j} = t_{p0}\left(1 + \frac{f_j}{\gamma}\right) = t_{p0}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right) = t_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)} \qquad \boxed{t_p = N t_{p0}\left(1 + \frac{f_j}{\gamma}\right)}$$

$f_1 = f_2 = f_3 = \ldots = F^{1/N}$ $\qquad f_1 \times f_2 \times f_3 \times \ldots = F$ $\qquad F = C_L/C_{gin,1}$

Example



C_L/C_1 has to be evenly distributed across N = 3 stages:

$$f = \sqrt[3]{8} = 2 \qquad t_p = 3t_{p0}\left(1 + \frac{\sqrt[3]{8}}{\gamma}\right) = 9t_{p0} \quad \text{for } \gamma = 1$$

Optimum Number of Stages

For a given load, C_L and given input capacitance C_{in}

find optimal f if N is free (and possibly non-integer)

$$C_L = F \cdot C_{in} = f^N C_{in} \quad \text{with } N = \frac{\ln F}{\ln f}$$

$$t_p = N t_{p0}\left(1 + \frac{f}{\gamma}\right) = \frac{t_{p0} \ln F}{\gamma}\left(\frac{f}{\ln f} + \frac{\gamma}{\ln f}\right)$$

$$\frac{\partial t_p}{\partial f} = \frac{t_{p0} \ln F}{\gamma} \cdot \frac{\ln f - 1 - \gamma/f}{\ln^2 f} = 0$$

$$f = \exp\left(1 + \frac{\gamma}{f}\right)$$

Closed-form solution only for $\gamma = 0$

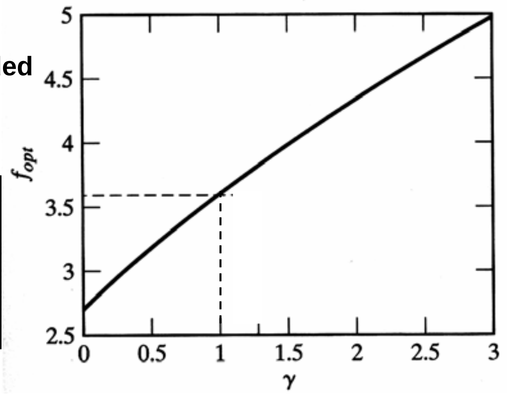
Optimum Effective Fanout *f*

Optimum *f* for given process defined by γ

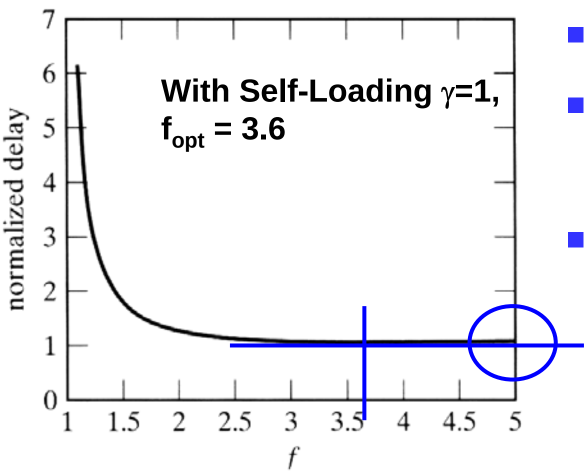
$$f = \exp\left(1+\frac{\gamma}{f}\right) \qquad N = \frac{\ln F}{\ln f}$$

(In practice, N must be rounded up or down to integer value)

	γ=0	γ=1
f_{opt}	e=2.72	3.6
N_{opt}	ln*F*	0.78ln*F*



Normalized t_p vs. *f*



- Slight increase of t_p for $f > f_{opt}$
- Choosing too few stages ($f > f_{opt}$) is relatively harmless for delay and saves area
- Too many stages is expensive in terms of delay

Fan-out of 4 is safe common practice

Normalized delay function of *F*

$$t_p = N t_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right) \qquad (\gamma = 1)$$

F	Unbuffered	Two Stage	Inverter Chain
10	11	8.3	8.3
100	101	22	16.5
1000	1001	65	24.8
10,000	10,001	202	33.1