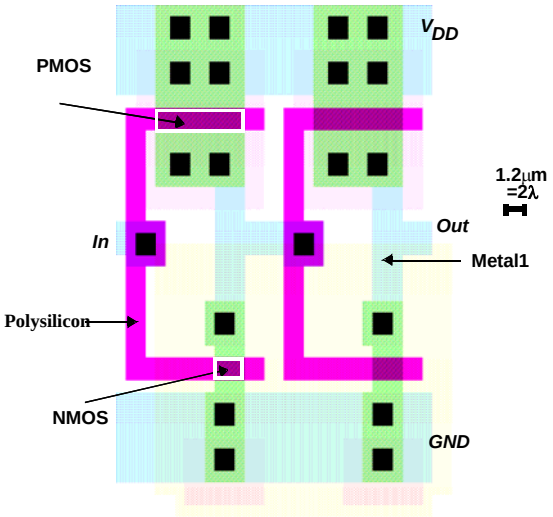
CMOS INVERTER
dynamic behavior (performance)

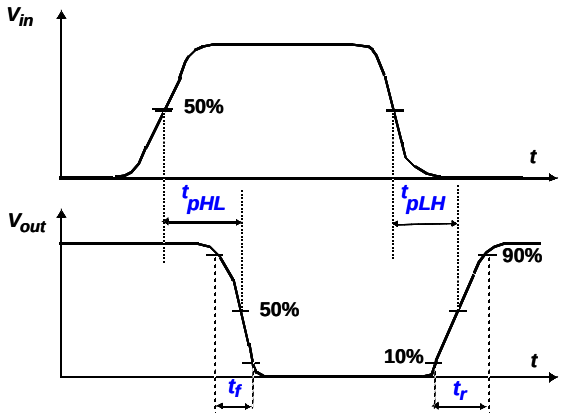
- **Capacitances**
- **(Dis)charge times**
- **Delay**

CMOS Inverters



- **What causes the delay?**
- **Where are the capacitances?**
- **Which capacitances determine t_p?**
- **How can we estimate (dis)charge times?**

Delay Definitions

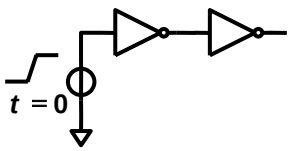


$$t_p = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right)$$

t_p : property of gate

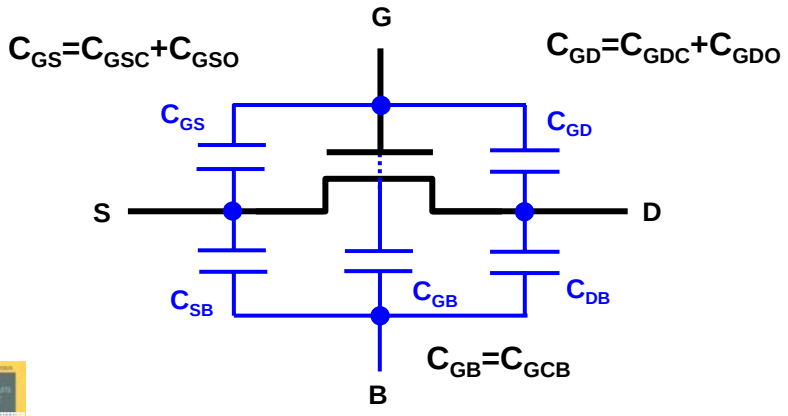
t_r , t_f : property of signal

CMOS Inverter Rise/Fall Delay

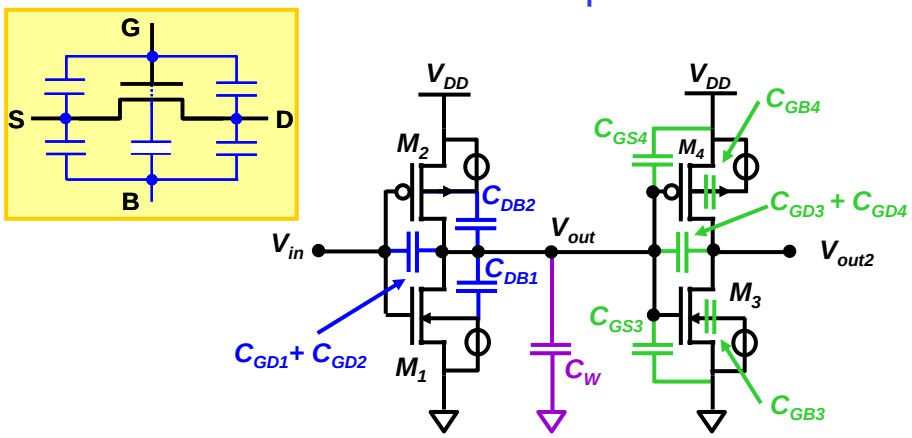


- Goal: determine t_{pLH}, t_{pHL}, t_f, t_r
- First: compute relevant capacitances
- Second: compute the time for (dis)charging those capacitances

MOS Capacitance Model



Inverter Cascade Capacitances

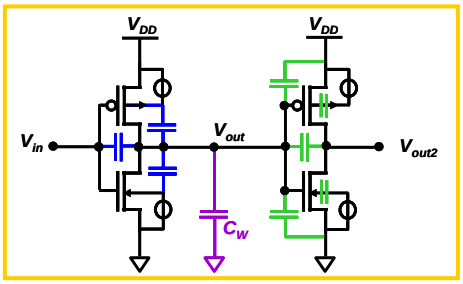


- $C_{GD1,2}$, $C_{DB1,2}$: drain (output) of driving inverter
- $C_{GS3,4}$, $C_{GD3,4}$, $C_{GB3,4}$: gate (input) of loading inverter (fanout capacitances)
- C_W : parasitic (wire) capacitances

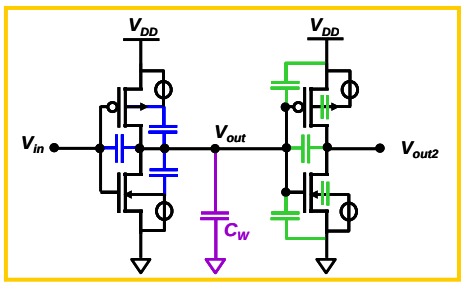
Manual Delay Estimation

- Now, we (sort of) know the capacitances that determine inverter delay
- (Drastic) simplification needed for hand calculation

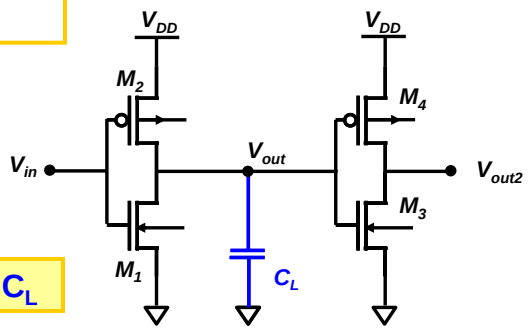
- Replace these C's by one lumped linear capacitance connected to ground.
- This is an approximation, because:
  - Most C's are non-linear
  - They are not between V_{out} and a fixed potential



Lumped Capacitance Model



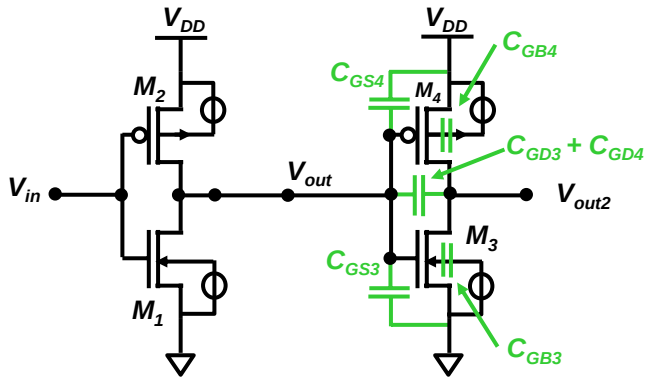
For Manual Delay Estimation



Next: How to estimate C_L

Gate Caps of Loading Inverter

- Consider 3 groups of caps separately
- Begin with gate caps of loading inverter



Gate Caps of Loading Inverter (2)

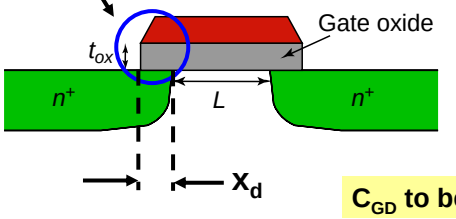
$C_G = C_{GS} + C_{GD} + C_{GB}$ when in off-state (no channel)

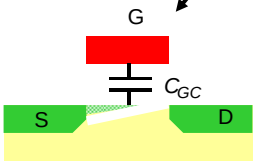
$= C_{GCS} + C_{GSO}$

C_{GCS} → Part of gate-channel cap attributed to source, depends on level of saturation

C_{GSO} → Gate-source overlap capacitance

$C_{GSO} = C_{GDO} = C_{ox}\, x_d\, W = C_o\, W$





C_{GD} to be decomposed similarly as C_{GS}

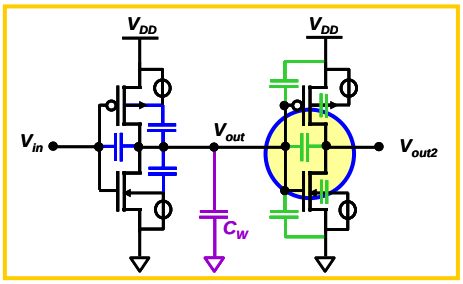
Gate Caps of Loading Inverter (3)

$C_G = C_{GS} + C_{GD} + C_{GB}$

- C_{GD} connected between V_{out} and V_{out2}
- Swing on V_{out2} is (almost) zero for 50% swing of V_{out}
- C_{GS} and C_{GB} between V_{out} and fixed potential

Conclusion

C_G of loading inverter can be considered between V_{out} and fixed potential



Gate Caps of Loading Inverter (4)

$C_G = C_{GS} + C_{GD} + C_{GB}$
$= C_{GCS} + C_{GSO} + C_{GCD} + C_{GDO} + C_{GB}$

- **Overlap capacitances** are linear
- **'active' capacitances** are highly non-linear but….
- their sum is much more linear, given by C_{ox} W L

Conclusions

1. C_G between V_{out} and fixed potential
2. $C_G = C_{ox}$ W L + $2C_{ox}$ x_d W

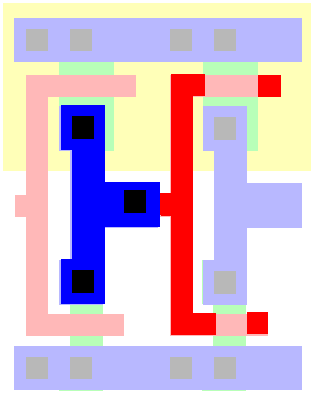
Capacitances in 0.25 µm CMOS process

	C_{ox} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9


```
simulator lang=spectre
model nmos bsim3v3
+version=3.1
+type =n
+tnom = 25          xl = 3e-8
+xw   = 0          tox = 5.8e-9
...
+mj   = 0.4960069   pb = 0.9173808  cjsw  = 2.751528e-10
+mjsw = 0.443145  pbsw = 0.9173808  cjswg = 2.135064e-10
...
+cgdo = 3.11e-10  cgso = 3.11e-10  capmod = 0
...
```

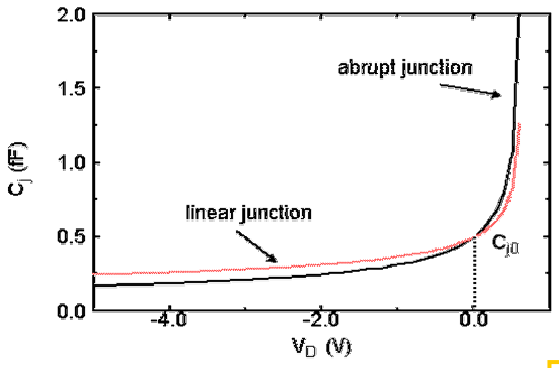
$$C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-12}}{5.8 \times 10^{-9}} = 5.95 \ fF/\mu m$$

Wire Capacitances



- (Almost) perfectly linear
- Usually computed by layout-to-circuit extraction
- Coupling capacitances usually considered grounded for manual calculation
- Highlighted part connected to V_{out} and not accounted for with device cap
- Wire (a.k.a. interconnect) capacitance
- Connected between V_{out} and (to first order) fixed potential of bulk

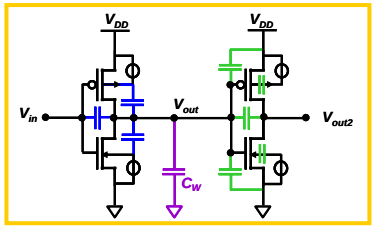
Drain Caps of Driving Inverter



- Junction capacitance C_{DB}
- Highly Non-linear

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\varphi_0}\right)^m}$$

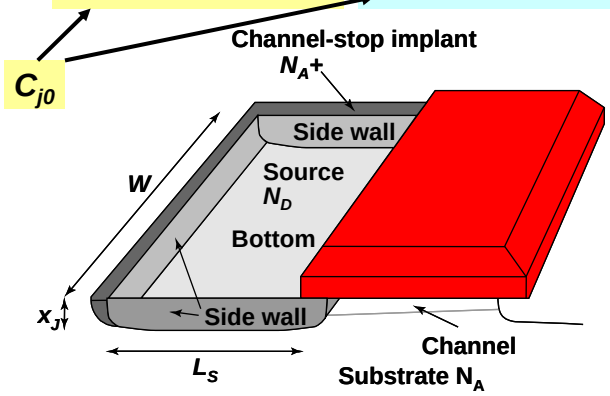
m=0.5: abrupt junction
m=0.33: linear junction



Junction Caps in 0.25 μm CMOS process

	C_{ox} (fF/μm²)	C_O (fF/μm)	C_j (fF/μm²)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\varphi_0}\right)^m}$$



Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

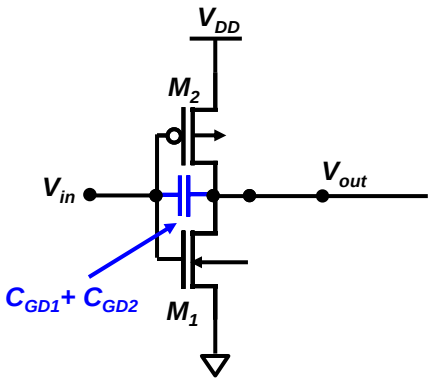
	High-to-Low		Low-to-High	
	K_{eqb}	K_{eqsw}	K_{eqb}	K_{eqsw}
NMOS	0.57	0.61	0.79	0.81
PMOS	0.79	0.86	0.59	0.70

Junction Caps in 0.25 μm CMOS process

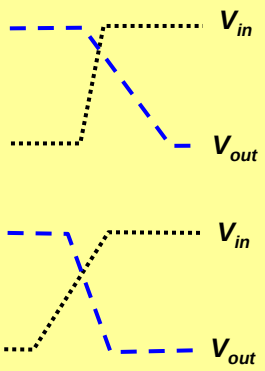
	C_{ox} (fF/μm²)	C_O (fF/μm)	C_j (fF/μm²)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9


```
simulator lang=spectre
model nmos bsim3v3
+version=3.1
+type =n
+tnom = 25          xl = 3e-8
+xw   = 0          tox = 5.8e-9
...                                  cj    = 2.024128e-3
+mj   = 0.4960069   pb = 0.9173808  cjsw  = 2.751528e-10
+mjsw = 0.443145  pbsw = 0.9173808  cjswg = 2.135064e-10
...
+cgdo = 3.11e-10  cgso = 3.11e-10  capmod = 0
...
```

Gate-Drain Cap of Driving Inverter



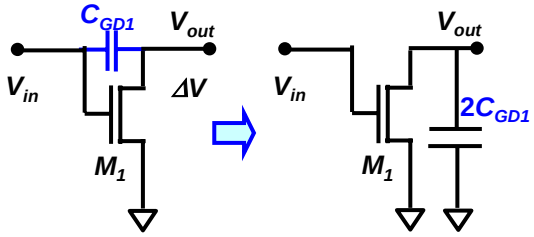
Example waveforms



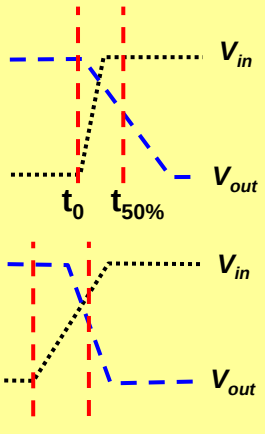
- Non-constant voltage at either side of C_{GD}
- Needs to be accounted for during modeling
- Effect depends on relative slopes of V_{in} and V_{out}

Equivalent Grounded Drain Cap

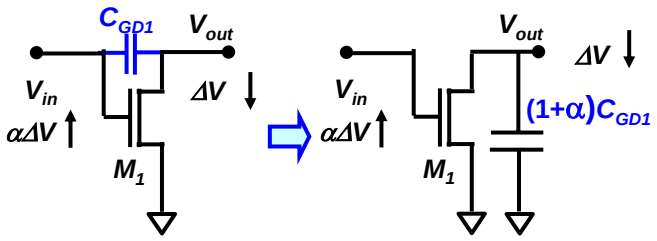
- Effective voltage swing across capacitor is sum of swing of V_{in} and V_{out} in interval from t_0 to $t_{50\%}$
- For a ΔV swing on output, $\alpha\Delta V$ swing on input
- Effective swing ~$(1+\alpha)\,\Delta V$
- α=1 is usual approximation
- Coupling cap modeled as 2x ground cap



Example waveforms

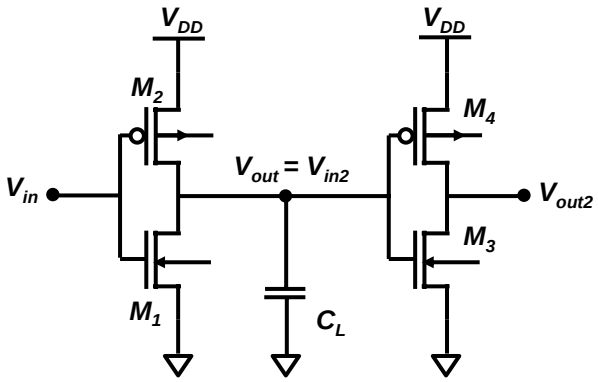


Equivalent Grounded Drain Cap



- Typically, α is taken 1 (but it is only an approximation)
- This may remind you of the Miller effect in analog circuits
- But it is not the same as the Miller effect
- …although it is sometimes denoted as 'digital Miller effect'

Lumped Capacitance Model Result

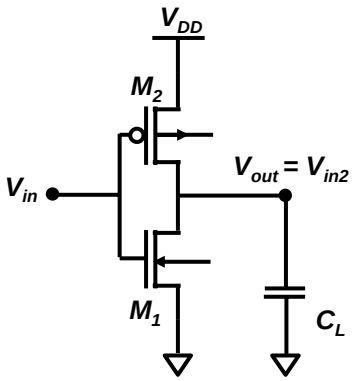


Sum of all Caps connected to Vout, with C_{GD} of driver counted twice to account for 'digital Miller effect'

$$C_L = 2(C_{GD1} + C_{GD2}) + C_{DB1} + C_{DB2} + C_{G3} + C_{G4} + C_W$$

($C_{G3} = C_{GS3} + C_{GD3} + C_{GB3}$, $C_{G4} = \ldots$)

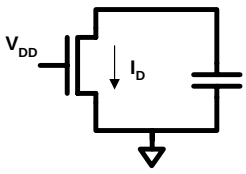
(Dis)charge Time



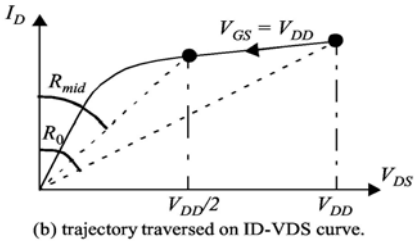
- Use equivalent R_{on}
  $t_p = 0.69\, R_{on}\, C_L$
- Or integrate transistor current

$$t_p = \int_{v_1}^{v_2} \frac{C_L}{i(v)} dv$$

Equivalent R_{on} (R_{eq})



(a) Schematic



(b) trajectory traversed on ID-VDS curve.

$$R_{eq} = \frac{1}{2}\left[\frac{V_{DD}}{I_{DSAT}\left(1+\lambda V_{DD}\right)} + \frac{V_{DD}/2}{I_{DSAT}\left(1+\lambda V_{DD}/2\right)}\right]$$

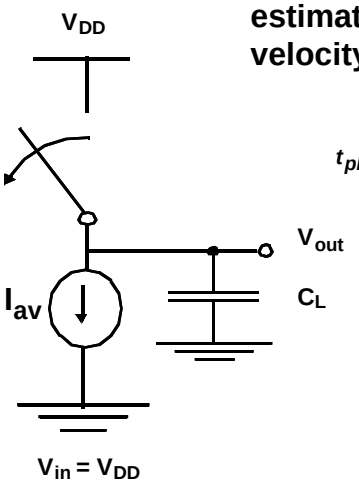
$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

$$t_p \approx 0.69 \times \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right) C_L$$

Current Based Estimate for t_p

Alternative current-based estimate for t_p, assuming velocity saturation

$$t_{pHL} = \frac{C_L \frac{V_{swing}}{2}}{I_{av}} \approx \frac{C_L V_{DD}}{2 I_{DSAT}\left(1+\frac{3}{4}\lambda V_{DD}\right)}$$



Exercise (Problem 5.4): Derive the expression above

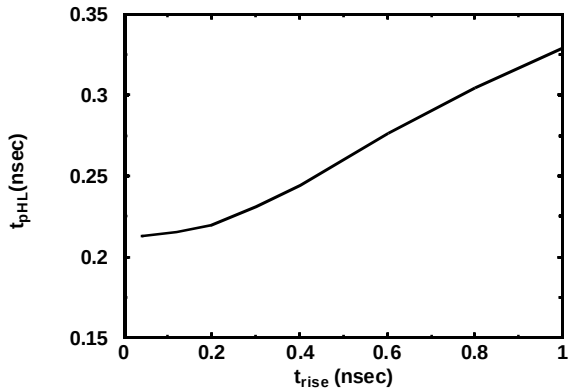
Comparison

With V_{DD}=2.5, λ=0.06 :

$$t_p \approx 0.69 \times \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)C_L \Rightarrow t_p \approx 1.13\frac{C_L}{I_{DSAT}}$$

$$t_p \approx \frac{C_L V_{DD}}{2 I_{DSAT}\left(1+\frac{3}{4}\lambda V_{DD}\right)} \Rightarrow t_p \approx 1.12\frac{C_L}{I_{DSAT}}$$

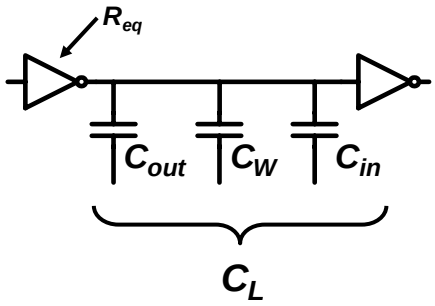
Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Empirical from the first edition of book

Inverter Propagation Delay Summary



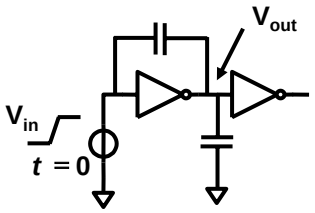
$$t_{pHL} = 0.69 R_{eqn} C_L$$

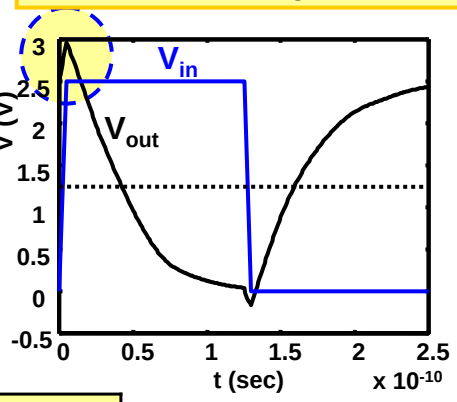
$$t_{pLH} = 0.69 R_{eqp} C_L$$

$$t_p = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right)$$ **Propagation time**

Simulation Results

Overshoot due to 'Digital Miller Effect'

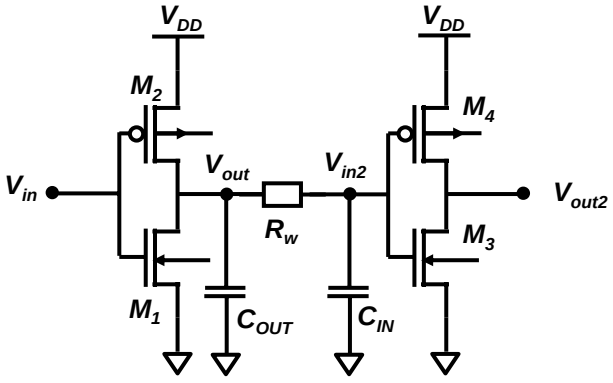




	analysis	simulation
t_{pHL} (ps)	36	39.9
t_{pLH} (ps)	29	31.7

- Good accuracy
- Is in fact good luck

Lumped Capacitance Model with Interconnect Resistance



$C_{out} = 2C_{GD12} + C_{DB1} + C_{DB2} + C_w/2$

$C_{in} = C_{g3} + C_{g4} + C_w/2$

$$t_{pHL} = 0.69 R_{eqn} C_{out} + 0.69(R_{eqn} + R_W) C_{in}$$