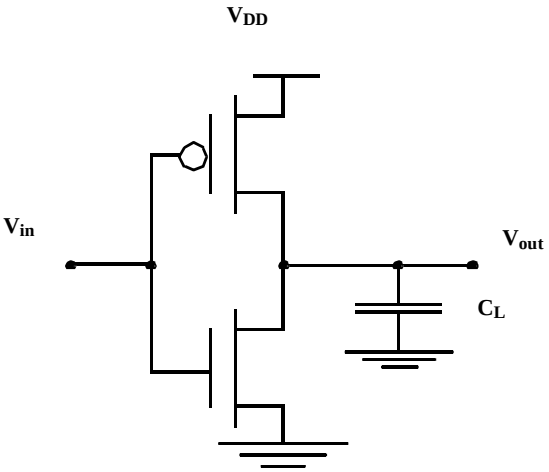
CMOS INVERTER

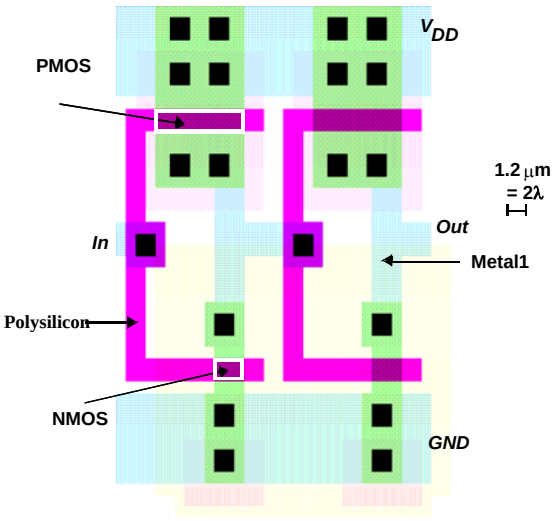
The CMOS Inverter - Outline

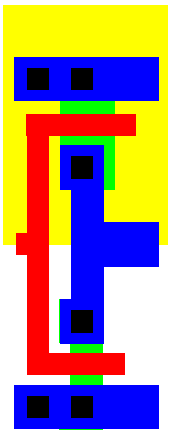
- First Glance
- Digital Gate Characterization
- Static Behavior (Robustness)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance)
  - Capacitances
  - Delay
- Power
  - Dynamic Power, Static Power, Metrics

The CMOS Inverter: A First Glance

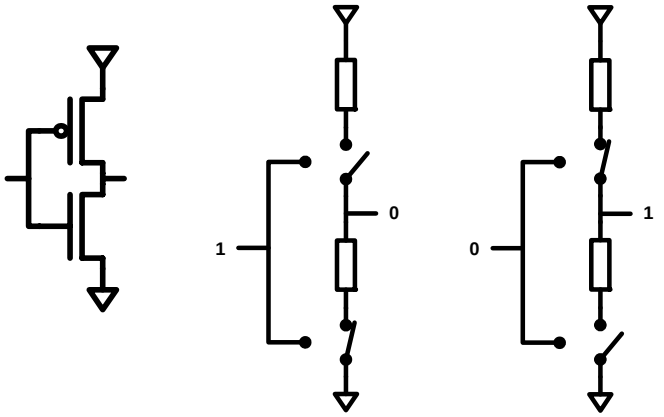


CMOS Inverters (1)





CMOS Inverter Operation Principle

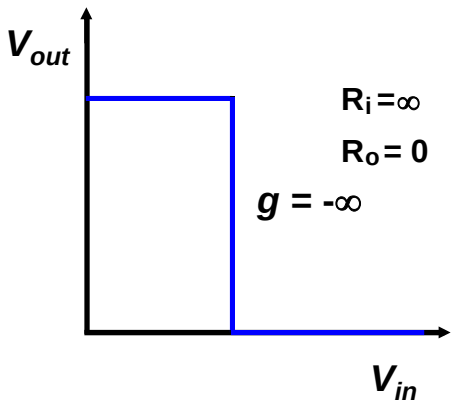


$V_{OH} = V_{DD}$ $V_{OL} = 0$

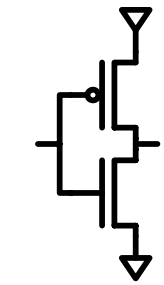
Digital Gate Fundamental Parameters

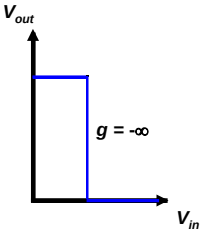
- Functionality
- Reliability, Robustness
- Area
- Performance
  - Speed (delay)
  - Power Consumption
  - Energy

The Ideal Inverter



Static CMOS Properties





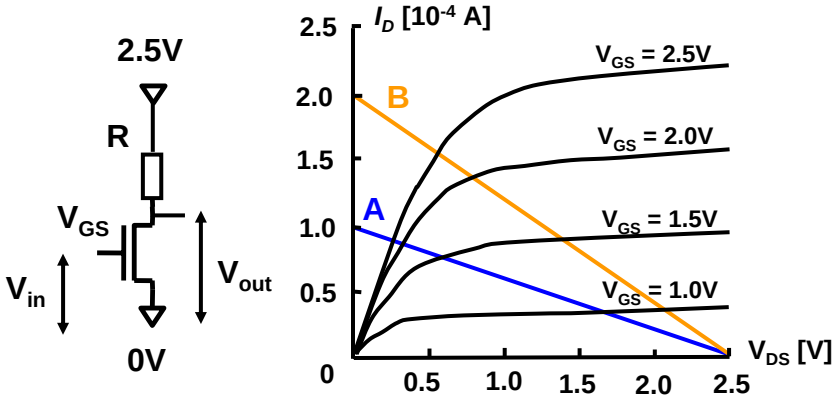
Basic inverter belongs to class of static circuits: output always connected to either V_{DD} or V_{SS}. Not ideal but:

- **Rail to rail voltage swing**
- **Ratio less design**
- **Low output impedance**
- **Extremely high input impedance**
- **No static power dissipation**
- **Good noise properties/margins**

Exercise: prioritize the list above

Voltage Transfer Characteristic (VTC)

Load Line (Ckt Theory)



Exercise:

The blue load line A corresponds to R =

The orange load line B corresponds to R =

With load line A and V_{GS} = 1V, V_{out} =

Draw a graph $V_{out}(V_{in})$ for load line A and B

PMOS Load Lines

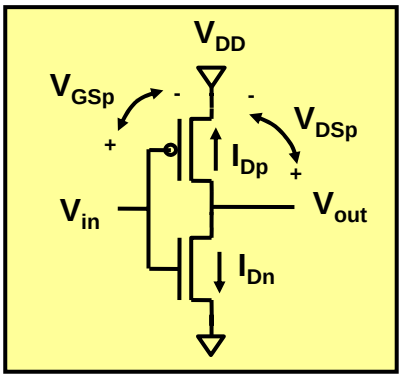
Goal: Combine I_{Dn} and I_{Dp} in one graph

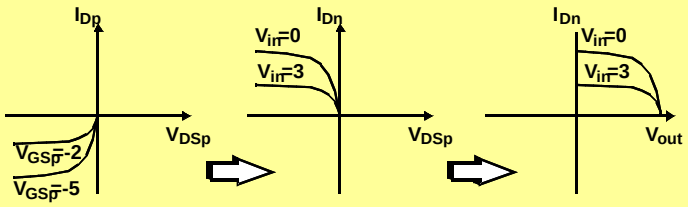
Kirchoff:

$V_{in} = V_{DD} + V_{GSp}$

$I_{Dn} = - I_{Dp}$

$V_{out} = V_{DD} + V_{DSp}$





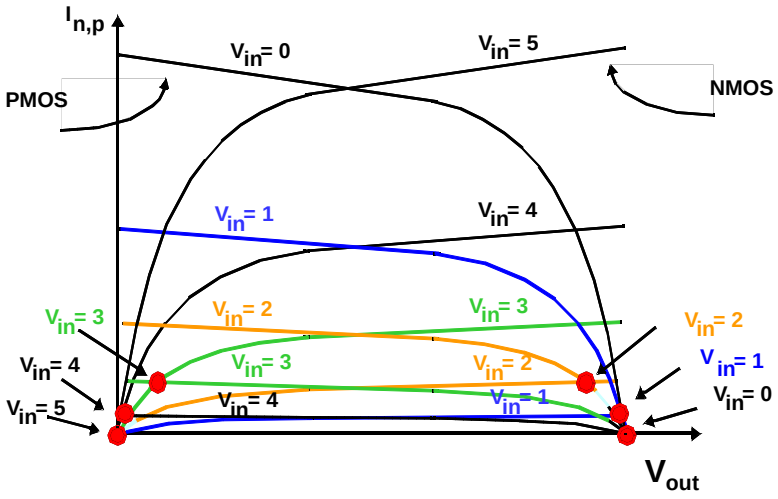
Example: V_{DD}=5V

$V_{in} = V_{DD} + V_{GSp}$

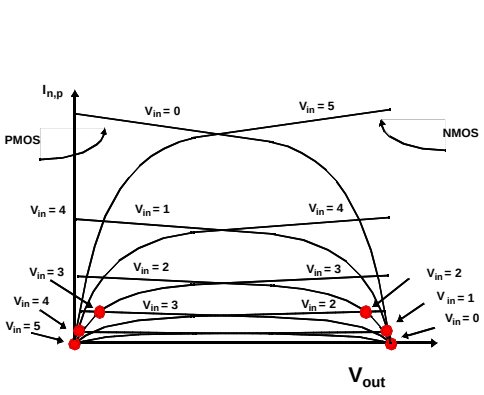
$I_{Dn} = - I_{Dp}$

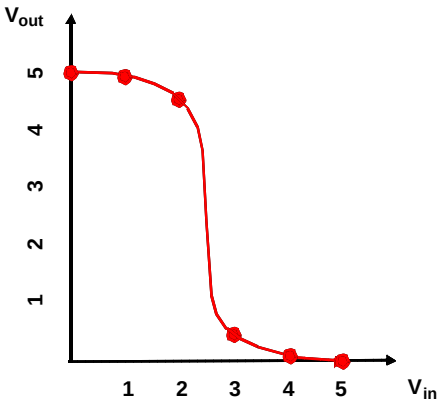
$V_{out} = V_{DD} + V_{DSp}$

CMOS Inverter Load Characteristics

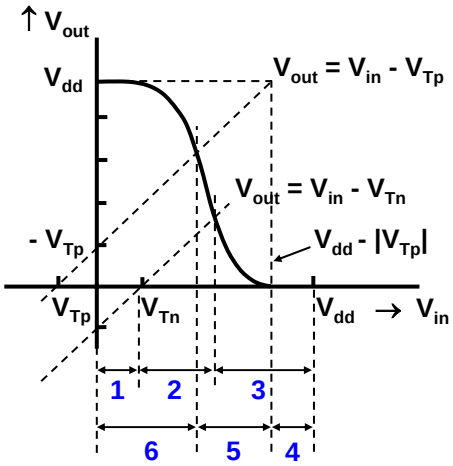


CMOS Inverter VTC





Operating Conditions



Need to know for proper dimensioning, analysis of noise margin, etc.

NMOS

1 $V_{in} = V_{GS} < V_{Tn} \Rightarrow$ **off**

2 $V_{out} > V_{in} - V_{Tn}$
$V_{DS} > V_{GS} - V_{Tn}$
$V_{GD} < V_{Tn} \Rightarrow$ **saturation**

3 $V_{out} < V_{in} - V_{Tn} \Rightarrow$ **resistive**

PMOS

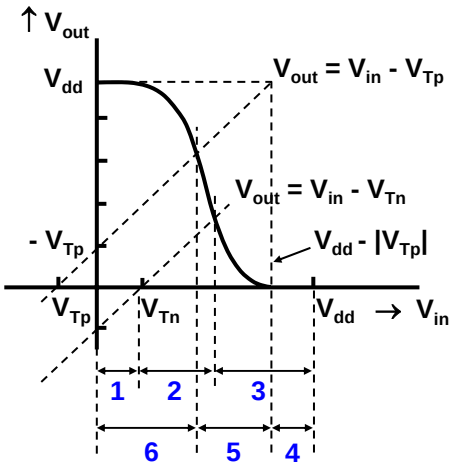
4 $V_{in} > V_{DD} + V_{Tp} \Rightarrow$ **off**

5 $V_{out} < V_{in} - V_{Tp} \Rightarrow$ **saturation**

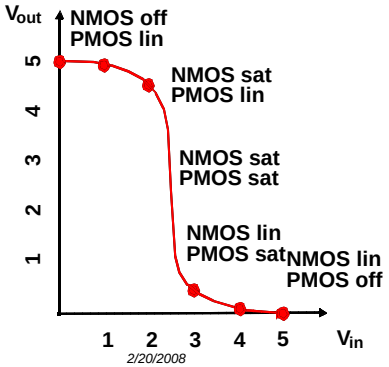
6 $V_{out} > V_{in} - V_{Tp} \Rightarrow$ **resistive**

Exercise: check results for PMOS

Operating Conditions



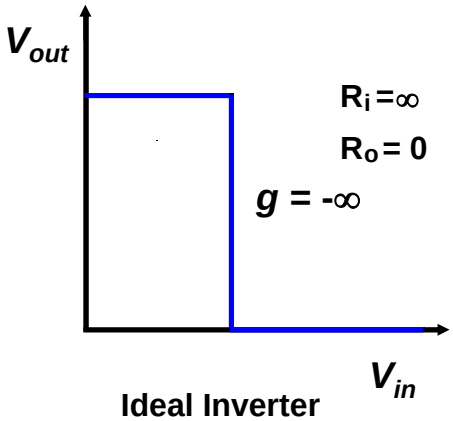
NMOS	1 off
	2 saturation
	3 resistive
PMOS	4 off
	5 saturation
	6 resistive



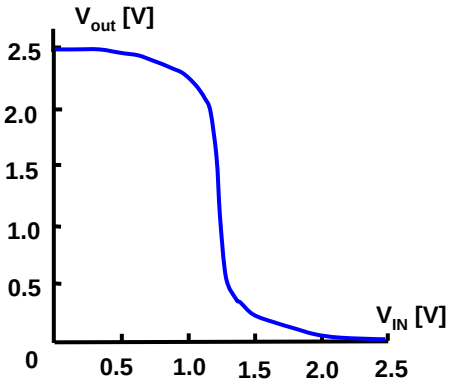
Inverter Static Behavior

- Regeneration
- Noise margins
- Delay metrics

The Realistic Inverter

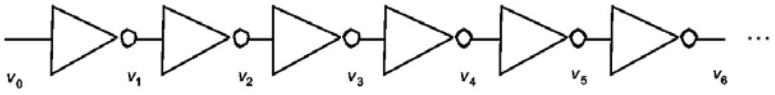


Ideal Inverter

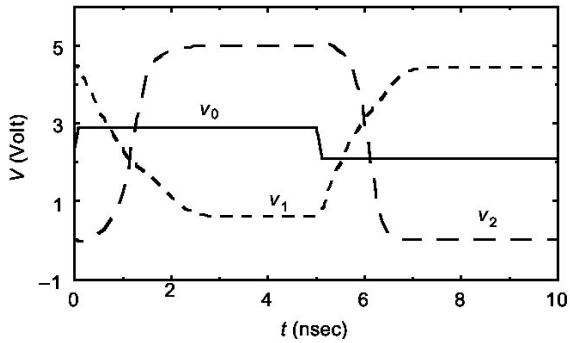


Realistic Inverter

The Regenerative Property



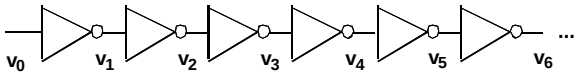
A chain of inverters



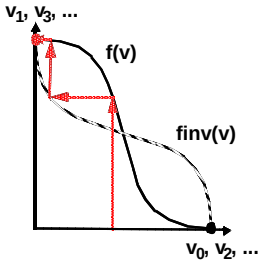
The regenerative property

- **Regenerative Property: ability to regenerate (repair) a weak signal in a chain of gates**

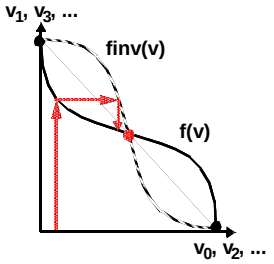
The Regenerative Property (2)



(a) A chain of inverters.

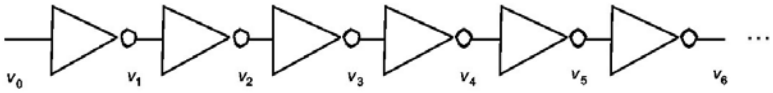


(b) Regenerative gate



(c) Non-regenerative gate

The regenerative Property (3)

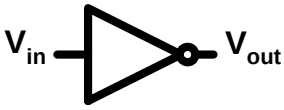


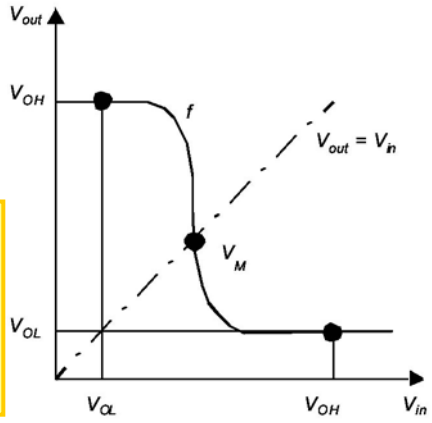
Exercise: what is the output voltage of a chain of 4 inverters with a piece-wise linear VTC passing through (0, 10), (3,7), (7,1) and (10,0) [Volt], as the result of an input voltage of 6 [Volt].

Exercise: discuss the behavior for an input of 5 [Volt]

Inverter Switching Treshold

- Not the device threshold $V_m = f(R_{onn}, R_{onp})$
- Point of $V_{in} = V_{out}$

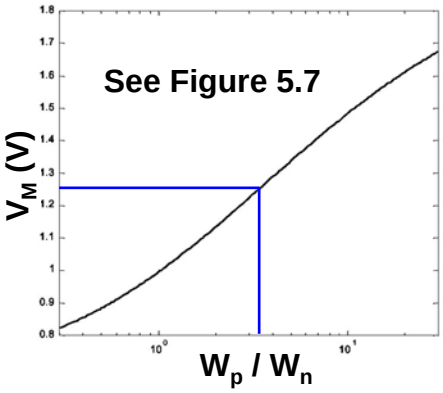




- Try to set W_n, L_n, W_p, L_p so that VTC is symmetric as this will improve noise margins

optimize NMOS-PMOS ratio

Simulated Gate Switching Threshold



Electrical Design Rule

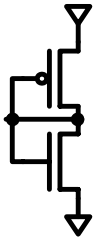
$W_p \approx 2.5\ W_n$

- Assumes $L_p = L_n$
- Should be applied consistently

- Symmetrical VTC $\Rightarrow V_m \approx \frac{1}{2} V_{DD} \Rightarrow W_p/W_n \approx$ ☐
- In practice: somewhat smaller
- Why? ☐

Inverter Switching Threshold
Analytical Derivation

- V_M is V_{in} such that $V_{in} = V_{out}$
- $V_{DS} = V_{GS} \Leftrightarrow V_{GD} = 0 \Rightarrow$ saturation
  - Assume $V_{DSAT} < V_M - V_T$
  - (velocity saturation)
  - Ignore channel length modulation
- V_M follows from
  - $I_{DSATn}(V_M) = - I_{DSATp}(V_M)$



Inverter Switching Threshold
Analytical Derivation (ctd)

$$I_{DSATn}(V_M) = - I_{DSATp}(V_M) \qquad I_D = kV_{DSAT}\left(V_{GS} - V_T - V_{DSAT}/2\right)$$

$$\Leftrightarrow k_n V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right) = -k_p V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)$$

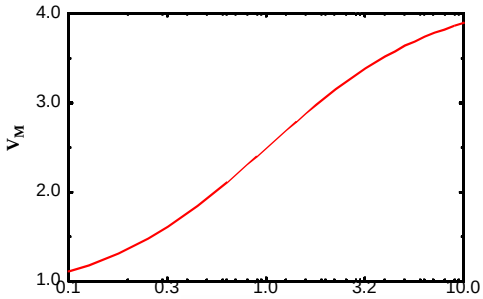
$$\Leftrightarrow \frac{k_p}{k_n} = \frac{-V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right)}{V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)} \qquad k = \frac{W}{L}k'$$

$$\Rightarrow \frac{(W/L)_p}{(W/L)_n} = \left|\frac{k'_n V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right)}{k'_p V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)}\right|$$

- See Example 5.1:
- $(W/L)_p = 3.5\,(W/L)_n$ for typical conditions and $V_M = ½\,V_{DD}$
- Usually: $L_n = L_p$

Gate Switching Threshold w/o Velocity Saturation

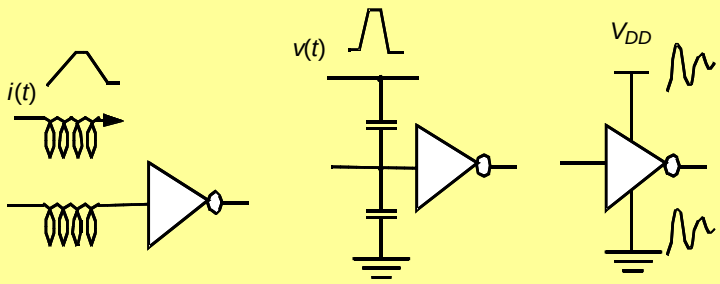
- **Long channel approximation**
- **Applicable with low V_{DD}**



Exercise (Problem 5.1): derive V_M for long-channel approximation as shown below

$$V_M = \frac{r(V_{DD} - V_{Tp} + V_{Tn})}{1+r} \quad with \quad r = \sqrt{\frac{-k_p}{k_n}}$$

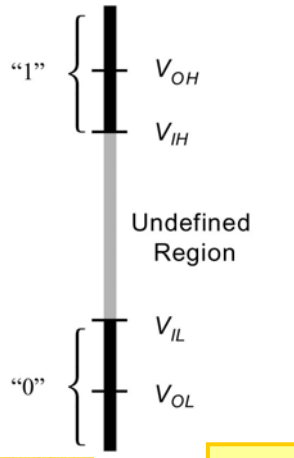
Noise in Digital Integrated Circuits

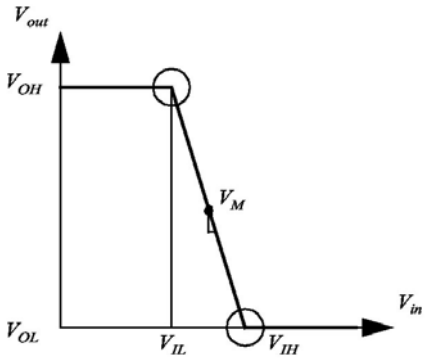


(a) Inductive coupling (b) Capacitive coupling (c) Power and ground noise

- **Study behavior of static CMOS Gates with noisy signals**

Noise Margins

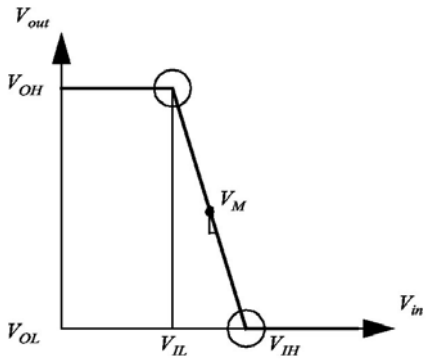


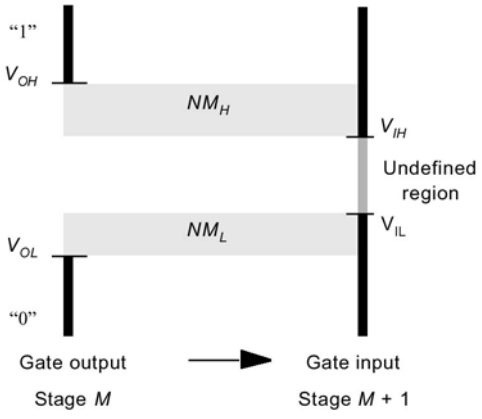



§ 1.3.2

- V_{OL} = Output Low Voltage
- V_{IL} = Input Low Voltage
- V_{OH}, V_{IH} = …

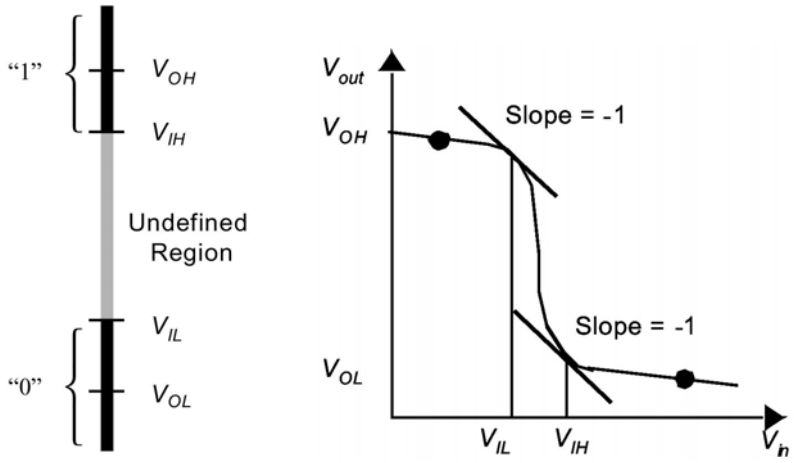
Noise Margins





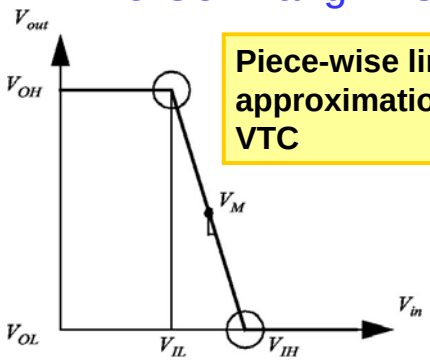
- $NM_H = V_{OH} - V_{IH}$ = High Noise Margin
- $NM_L = V_{IL} - V_{OL}$ = Low Noise Margin

Noise Margin for Realistic Gates



Exercise: explain significance of slope = -1 for noise margin

Noise Margin Calculation



Piece-wise linear approximation of VTC

g = gain factor (slope of VTC)

We know how to compute V_M

Next: how to compute g

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

§ 5.3.2

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$