Part 2: Process
Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

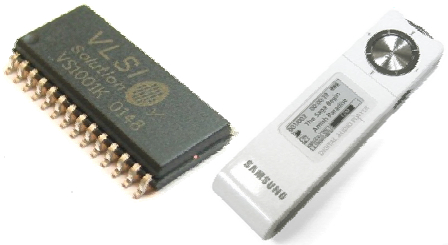
Outline

- CMOS Processing
  - Wafer Production
  - CMOS Process Outline
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Only very briefly

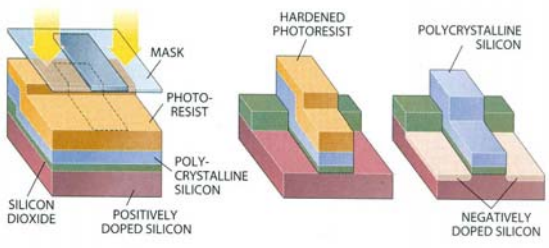
CMOS Processing

- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

IC Technology

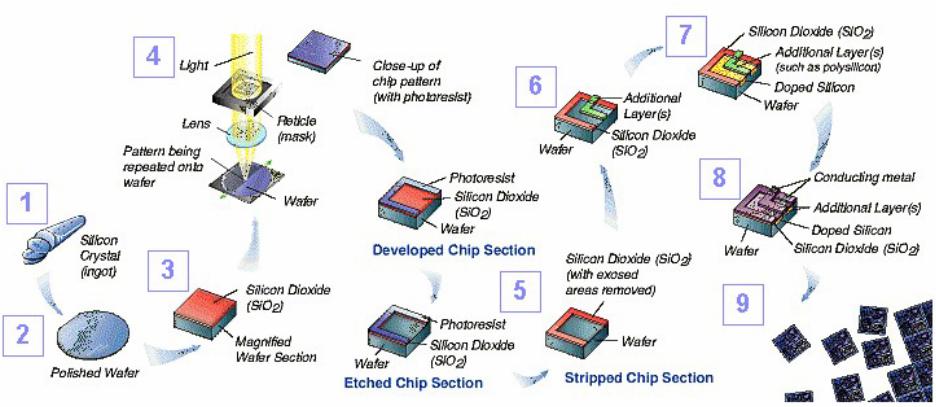


- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist



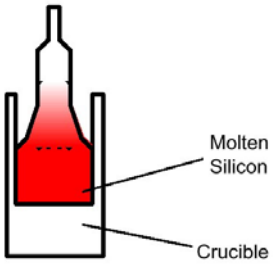
Multiple cycles, 100's STEPS in total

Another Overview of Semiconductor Processing

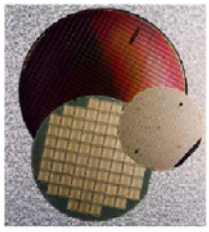


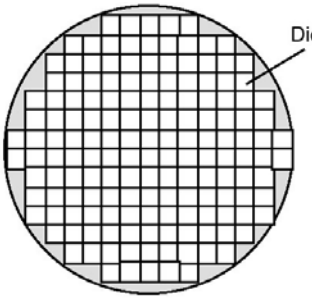
Wafer Processing – Czochralski Method

- Start with crucible of molten silicon (≈1425ºC)
- Insert crystal **seed** in melt
- Slowly rotate/raise seed to form single crystal **boule**
- After cooling, slice boule into **wafers** & polish



Wafer Structure

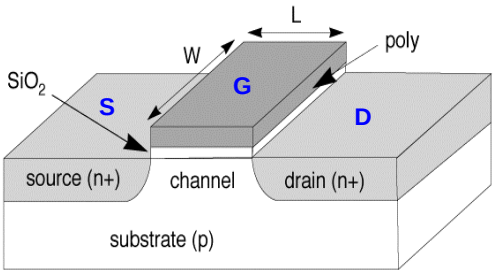


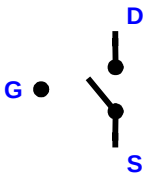


300 mm wafer (sematech)

CMOS Process Outline

MOS Transistor



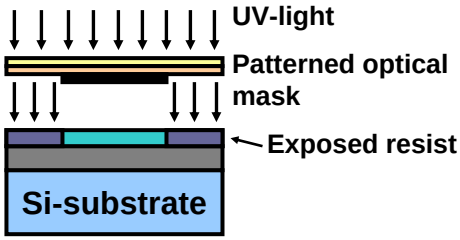


Position of switch depends on gate to source voltage

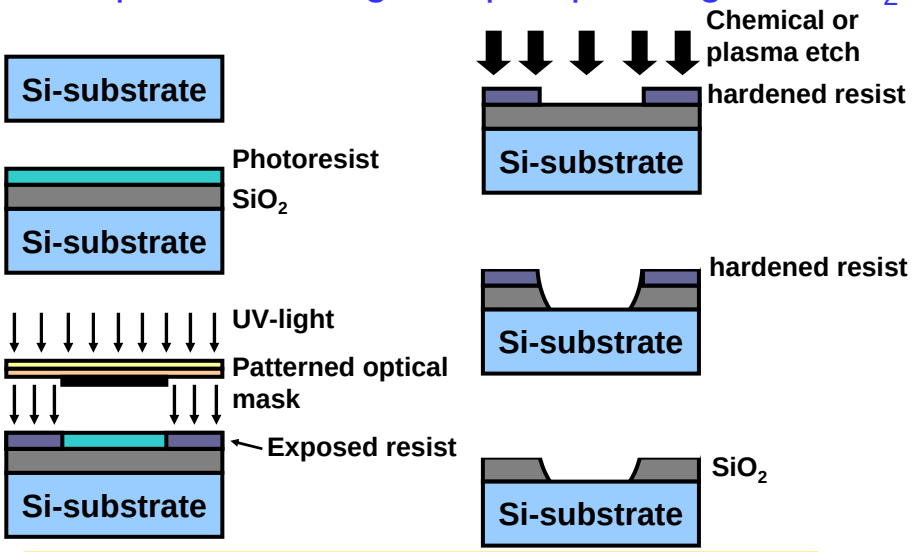
V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

How Patterns on a Chip are Created

- Basic Principle: Photolithography
  - Like projecting an image through a photographic negative (or positive)
- Coat wafer with Photoresist
- Shine UV light through glass mask
- Develop: dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")



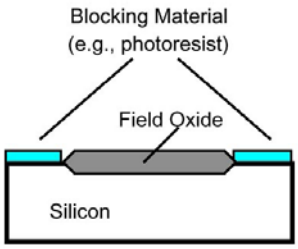
Example: Etching Step, opening of SIO_2



Etching is for removal of material, similar masking principles for deposition (adding of material)

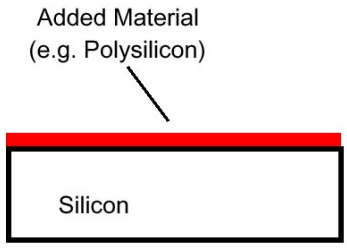
Oxidation

- SiO_2 formed by oxidation
  - Wet oxidation: heat with water (900ºC - 1200 ºC)
  - Dry oxidation:heat with pure oxygen (1200 ºC)
- Oxide occupies more volume
- Alternative: deposition



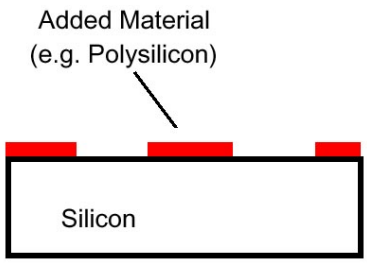
Adding Materials

- Add materials on top of silicon
  - Polysilicon
  - Metal
  - SiO_2
- Methods
  - Vapor deposition
  - Sputtering (Metal ions)



Patterning Added Materials

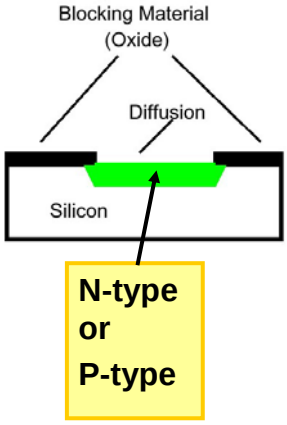
- Add material to wafer
- Coat with photoresist
- Selectively remove photo resist (PR), after exposure through mask
- Remove unprotected (by PR) material
- Remove remaining PR



Diffusion

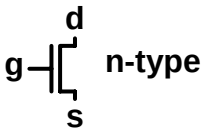
- Modify electrical properties of Si:
  - N-type (extra electrons)
  - or p-type

  (fewer electrons ⇔ extra holes)
- Introduce dopant via epitaxy or ion implant e.g. Arsenic (N), Boron (P)
- Allow dopants to diffuse
- Block diffusion in selective areas using oxide or PR (photo-resist)
- Diffusion spreads both vertically, horizontally

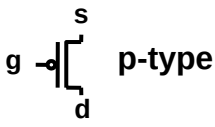


CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



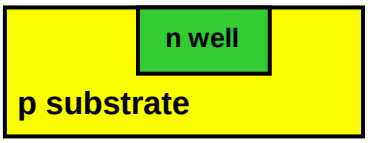
n-type



p-type

- "on" when V_g is high
- With n-type s/d
- Electrons (n) as carrier
- Built in p-type Si

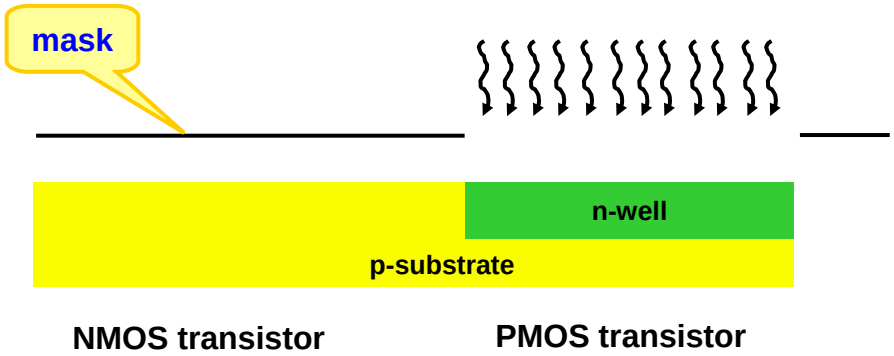
- "on" when V_g is low
- With p-type s/d
- Holes (p) as carrier
- Built in n-type Si



n-well (for PMOS) in p-type substrate (for NMOS)

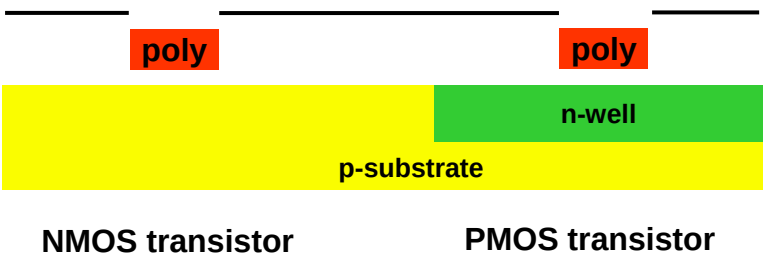
Outline of Process Flow

First place n-well to provide properly-doped substrate for n-type, p-type transistors :



Outline of Process Flow, cont'd

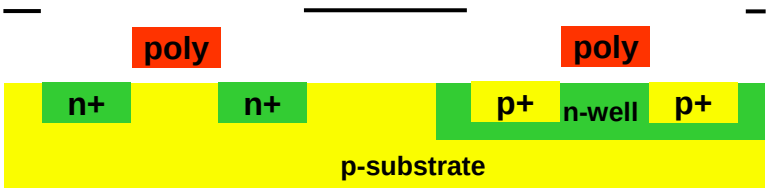
Pattern gate next, to later act as a mask for source and drain diffusions:



Outline of Process Flow, cont'd

Add s/d diffusions, performing self-masking by poly gate:

Poly also works as a mask, ensuring good alignment of s/d to gate

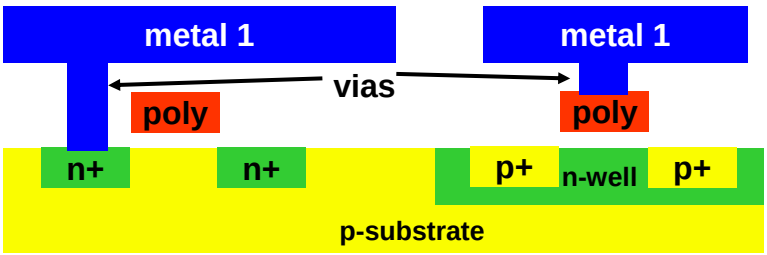


NMOS transistor PMOS transistor

Outline of Process Flow, cont'd

Start adding metal layers:

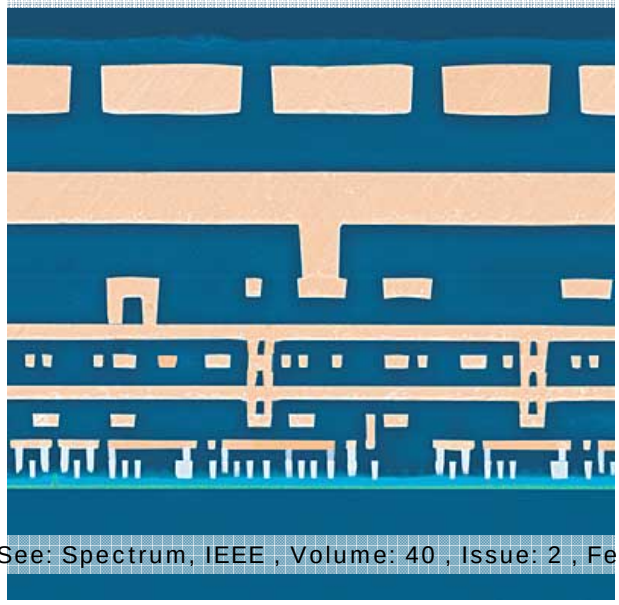
Via: contact hole between metal layers



NMOS transistor PMOS transistor

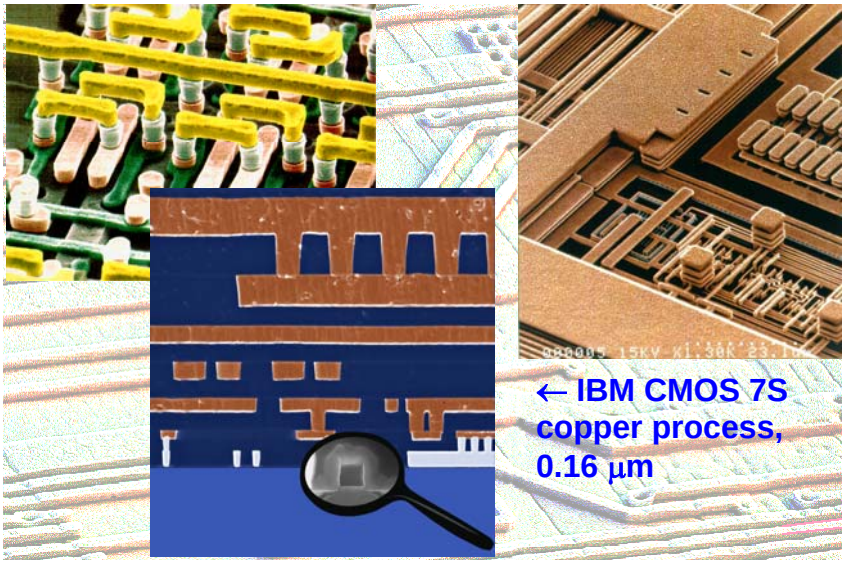
Similar for subsequent metal layers

Cross-section of advanced IBM process



See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

Interconnect Examples (motorola, ibm)



← IBM CMOS 7S copper process, 0.16 μm

IC Recipe Precisely Fixed

- Process conditions (temperature, time, concentration, ...) very critical
- Many strong compatibility issues of materials and processes
- Very expensive and difficult to tune
- Very expensive equipment and facilities
- Need Billions of turnover for break-even

Complex Lithographic Process

- Example: ASML TWINSCAN™ XT:1250
- Sub wave length Lithography
  193 nm KrF Laser (Deep UV)
- 65 nm resolution
- < 8 nm overlay
- > 85 WpH (300 mm)
- DOF ~ 0.50 μm (1: 600.000)
- price around 5M€
- www.asml.com
- Intel Fab 32 (2007)
  3B$ investment, class 10

Compare Stepper Wafer Size and Resolution to NL scale

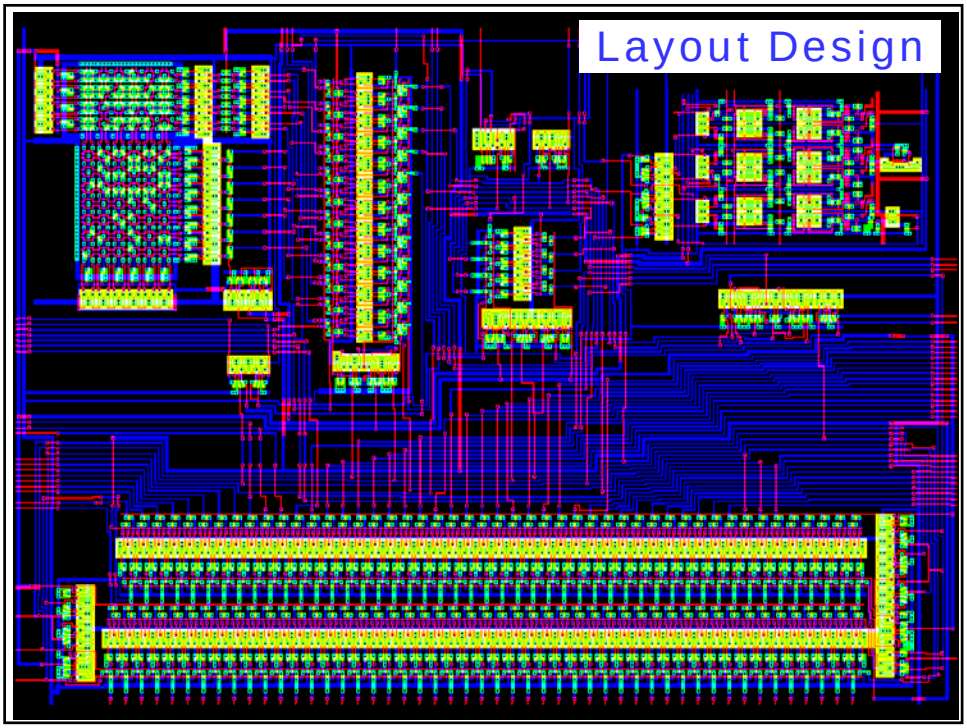
- **Wafer size: ∅ 300mm**
- **Resolution: 65nm**
- **Netherlands: 40.000 km^2 ~ 200km x 200km**

300mm	**1**	**65nm**
200km	**667x10^3**	**4.3cm**

A 'magnified' waferstepper could 'print' the Netherlands with a resolution of 4.3 cm in 42 sec.

Equivalent to a 52.5 terabit camera

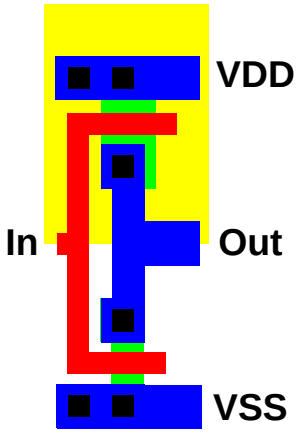
Layout Design



Layout Design

Layout Design Concepts

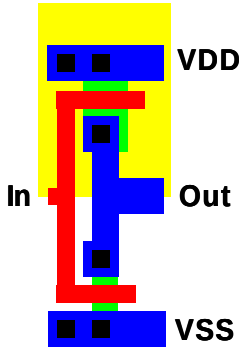
- Layer map
- Layout examples
- Stick diagrams



You should be able to understand such a drawing as well as simpler drawings called 'stick diagram'

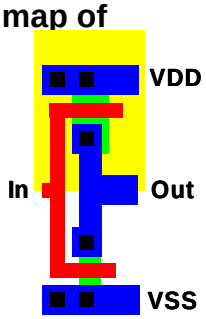
Layout Design

- Layout is design of fabrication masks
- Each mask is drawn in different color
- Layout is not a free-form drawing
  - Most often: Manhattan Layout (rectangular)
  - Sometimes 45-degree angles
  - Curved geometry only for special applications
- Layout should obey Design Rules



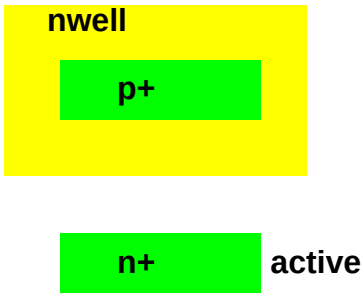
Layer Map

- Layers are assigned colors and/or patterns, not always 1 to 1
- Is a matter of convention
- Site-dependent, process dependent, tool dependent
- Be prepared to reverse-engineer layer map of unknown layouts

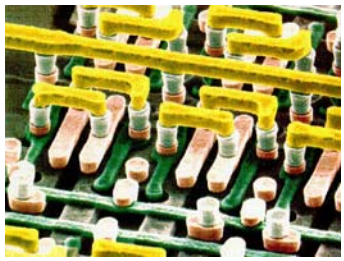


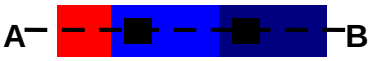
Polarity of Active Area

- Active layer or active area is the source/drain implant layer (area). Usually abbreviated as 'active' only.
- Normally, a so-called select mask determines polarity of active
- See color plate 5
- Many simplified drawings only show subset of the masks
- Rest should be clear from context

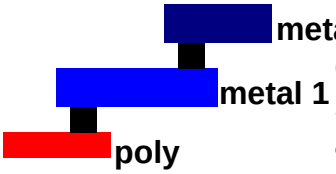


Contact Holes and Vias





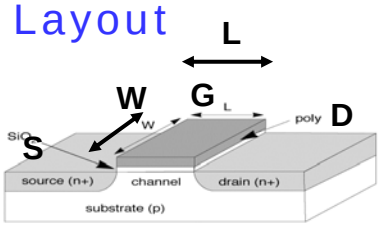
Layout (top view)



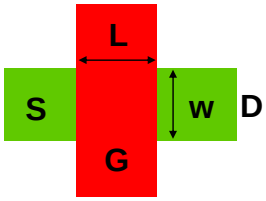
Cross-section along A-B

Transistor Layout

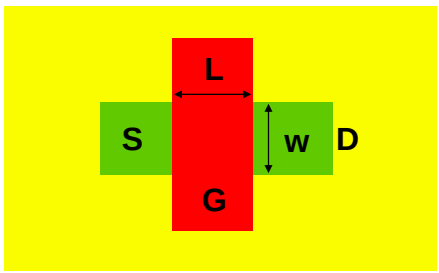
n-well (p-sub)



n-type



p-type



Simplified CMOS Layer Map

- **Compare to / instead of colorplate 1.**

yellow		nwell – place for P-transistors
pink		select – invert p
green		active – source and drain regions
red		polysilicon – gate material
blue		metal 1 – first interconnect metal
dark blue		metal 2 – second interconnect metal
magenta		metal 3 – third interconnect metal
black		contact, via – hole in interlayer oxide

- Lab won't use 'select' mask

- **Note: active = active area = diff = diffusion, well ≈ tub**

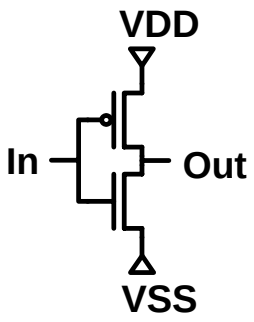
Further Simplified CMOS Layer Map

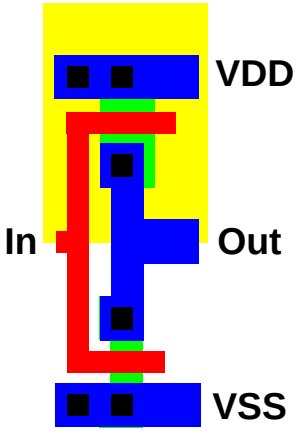
- **Compare to / instead of colorplate 1.**

yellow		nwell – place for P-transistors
green		active – source and drain regions
red		polysilicon – gate material
		metal 1 – first interconnect metal
black		contact, via – hole in interlayer oxide

- **Or equivalent B/W patterns**

Invertor Layout

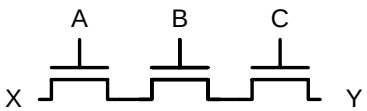




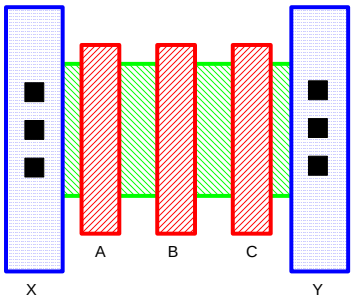
Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

Be able to draw such layouts (but more complex) (coming weeks) and reverse engineer (decode) them

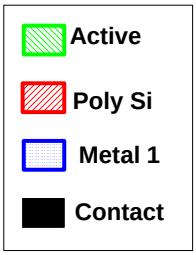
From Schematic to Layout



Transistor schematic



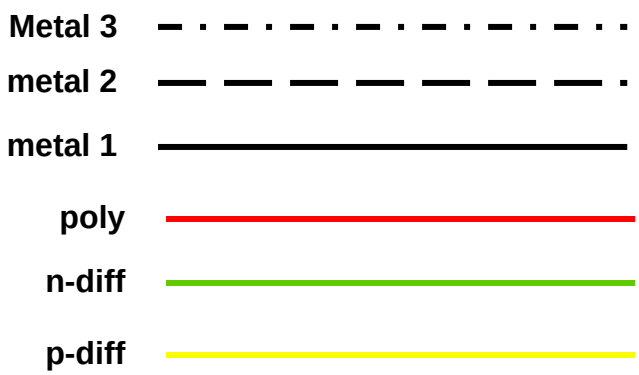
Layout



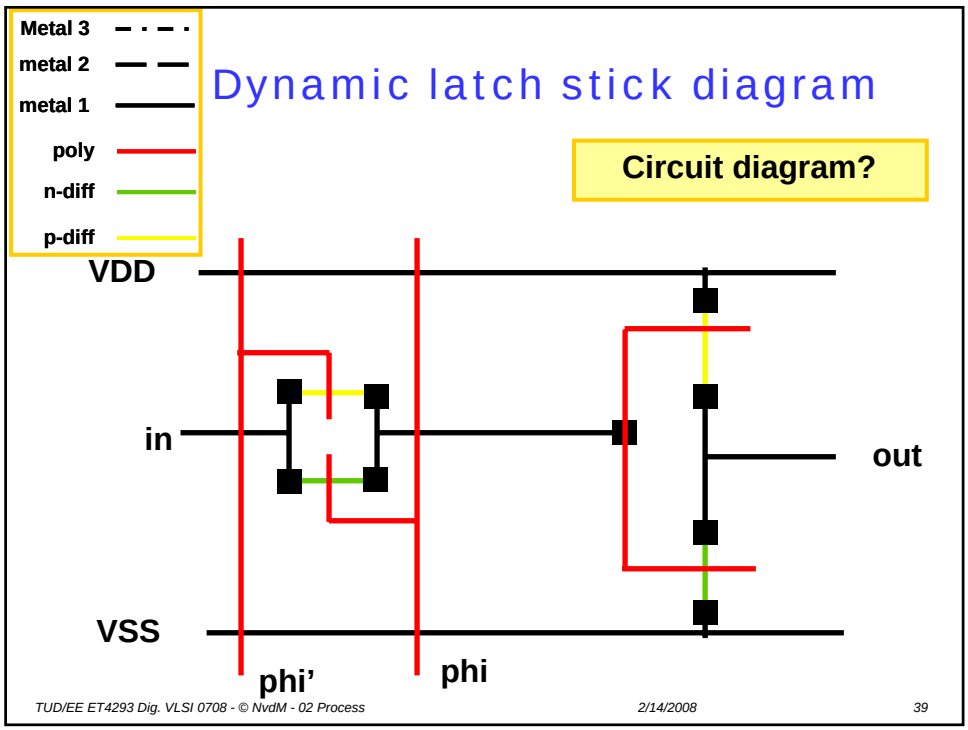
Stick diagrams

- A stick diagram is a cartoon of a layout.
- Does show components/vias but only relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.

Stick layers



- Caution: stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff


Metal 3
metal 2
metal 1
poly
n-diff
p-diff
Dynamic latch stick diagram
Circuit diagram?
VDD
in
out
VSS
phi'
phi
TUD/EE ET4293 Dig. VLSI 0708 - © NvdM - 02 Process
2/14/2008
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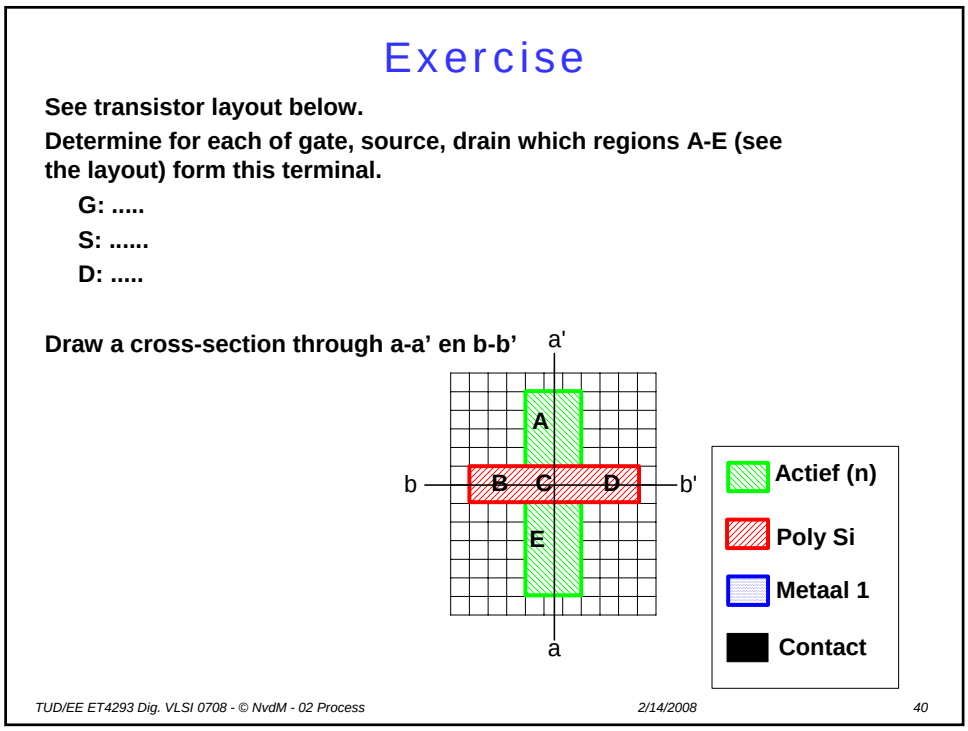
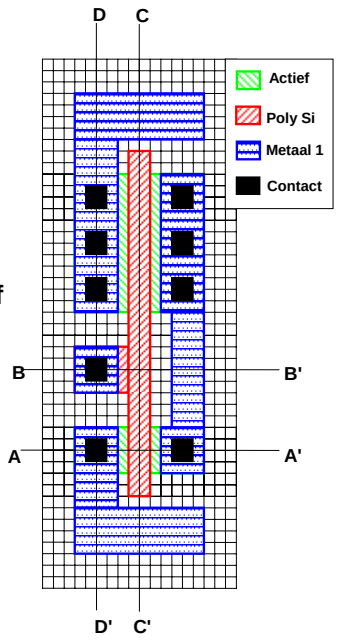

Exercise
See transistor layout below.
Determine for each of gate, source, drain which regions A-E (see the layout) form this terminal.
G: .....
S: .....
D: .....
Draw a cross-section through a-a' en b-b'
a'
A
b
B
C
D
b'
E
a
Actief (n)
Poly Si
Metaal 1
Contact
TUD/EE ET4293 Dig. VLSI 0708 - © NvdM - 02 Process
2/14/2008
40

See the CMOS inverter layout on the right

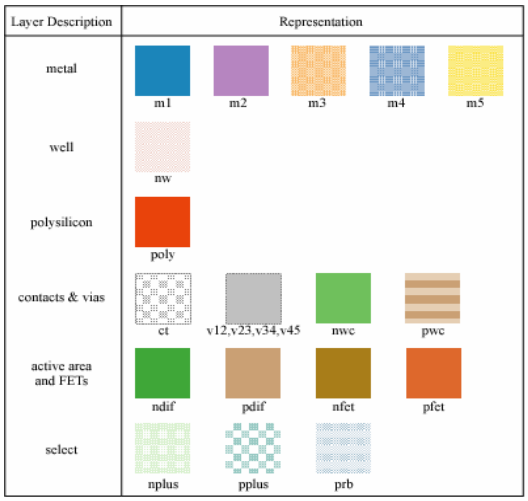
- Draw cross-sections A-A', B-B' and C-C'
- Which of the 2 transistors must be the P-transistor? Why?
- Draw the corresponding N-well.
- Annotate in the layout the location of the VDD and VSS terminals.
- Draw the schematic, including L and W ratios.



Design Rules

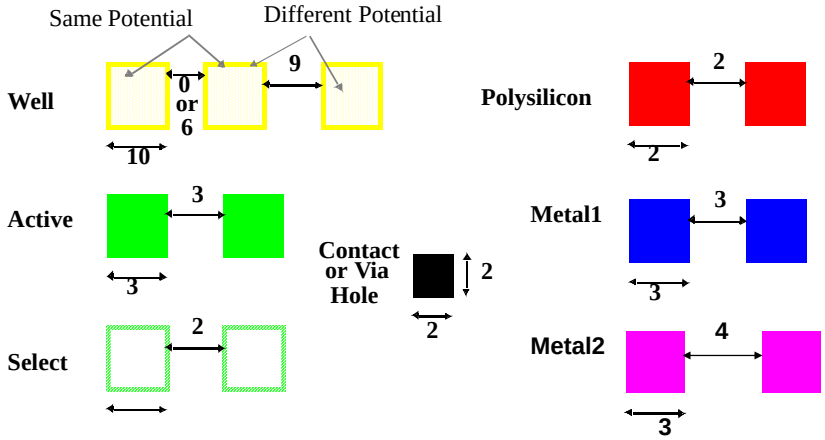
- The fabrication process will suffer from tolerances
- Chip features will have a practical minimum size to allow them to be fabricated reliably enough (with high enough yield)
- This is captured into a set of precise Design Rules
- Modern processes have terribly complex set of design rules as a compromise between flexibility and manufacterability
- Need to work with those rules during cell layout.

Layers in 0.25 μm CMOS process

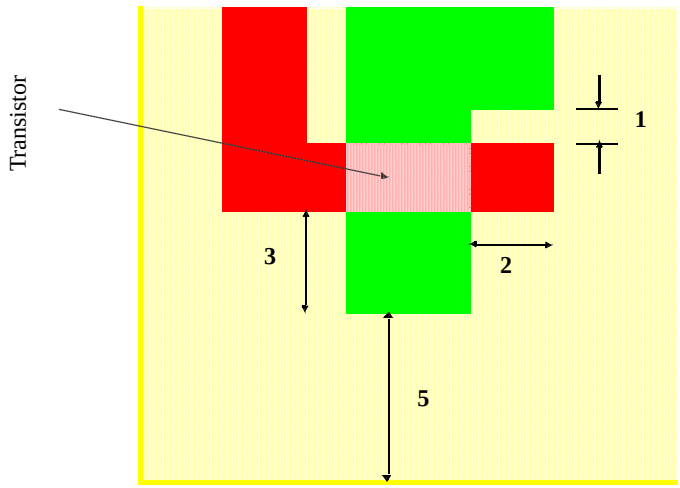


Intra-Layer Design Rules

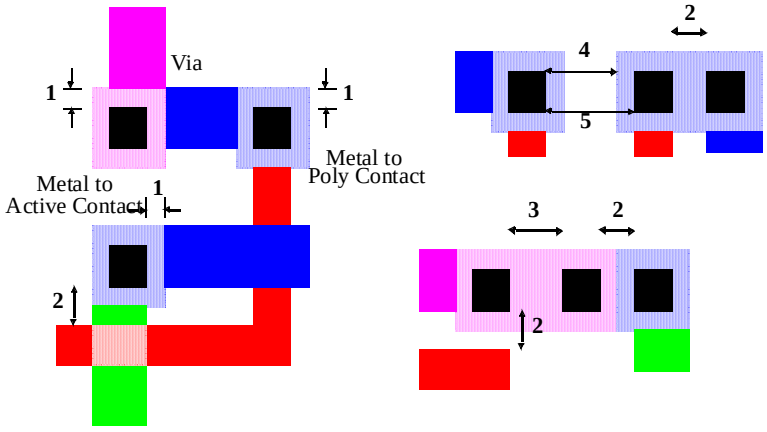
Example Rules



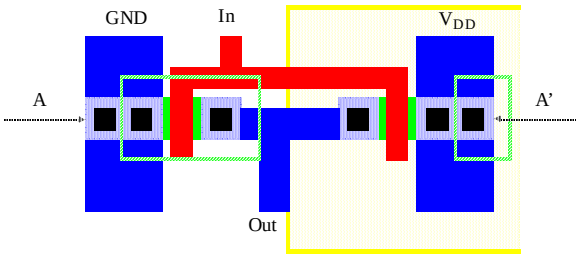
Transistor Layout



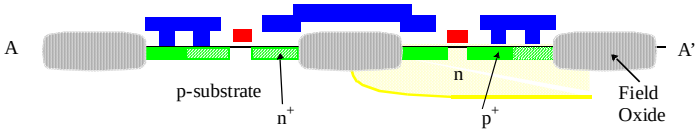
Vias and Contacts



CMOS Inverter Layout

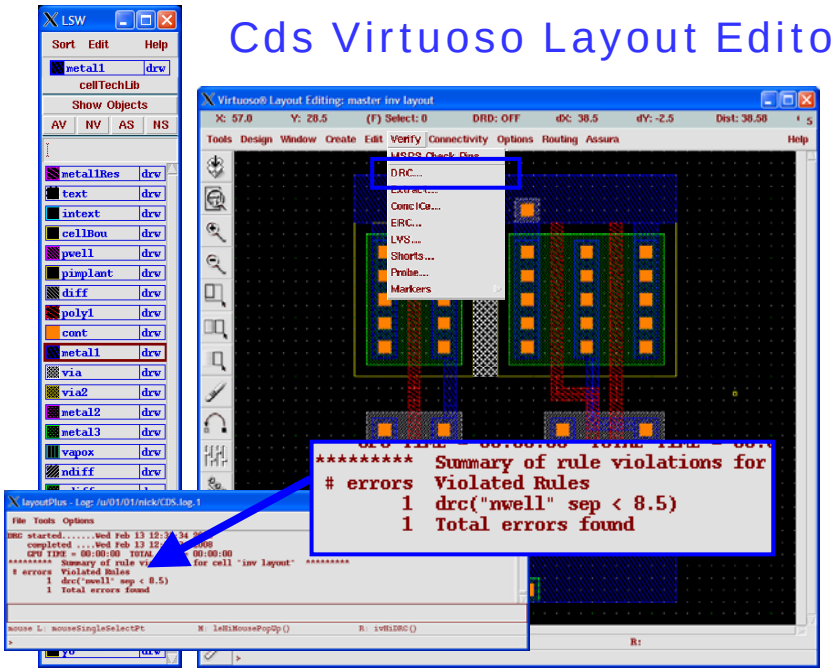


(a) Layout



(b) Cross-Section along A-A'

Cds Virtuoso Layout Editor



Summary

- CMOS Processing
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- CMOS Process Outline
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Why we need design rules