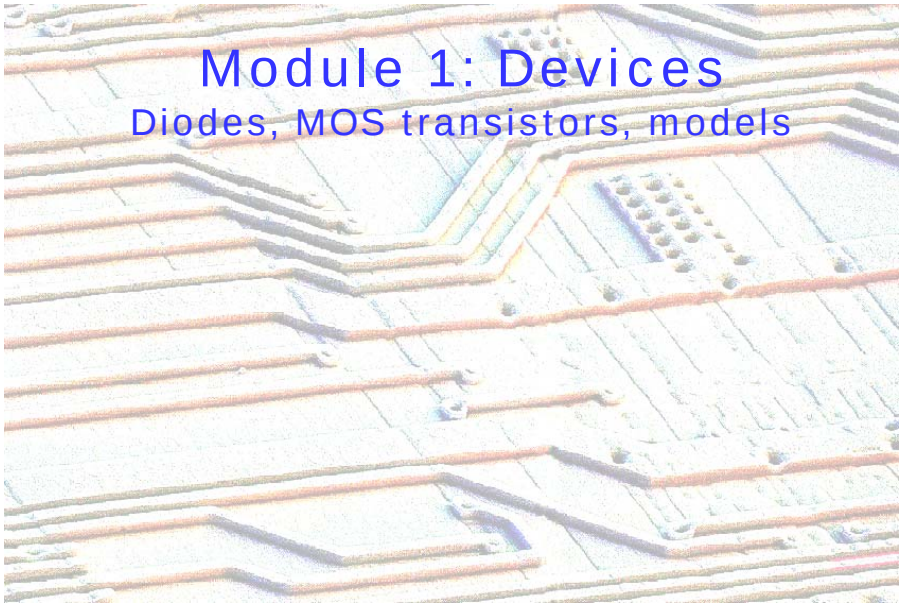




Module 1: Devices

Diodes, MOS transistors, models

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1

Goal of this chapter

- Present intuitive understanding of device operation
- Review of basic device equations
- Introduction of models for manual analysis
- Review of models for SPICE simulation
- Analysis of secondary and deep-sub-micron effects
- Future trends

■ In depth:

- ET4296 - Advanced Device Physics – 0/0/2/0 (René van Swaaij)
- Neamen: *Semiconductor Physics and Devices, basic principles*, 2003, McGraw Hill
- Taur and Ning: *Fundamentals of Modern VLSI Devices* 1998, Cambridge University Press

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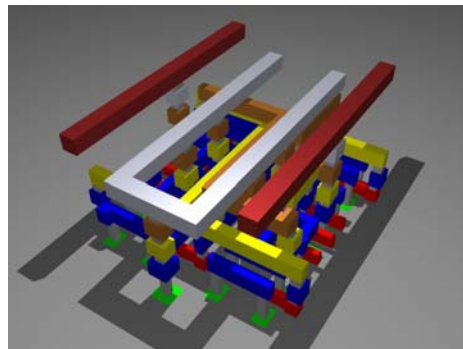
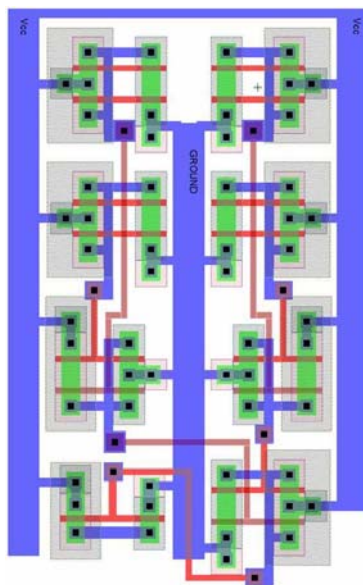
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Outline

- Semiconductor Physics
- The diode
 - Depletion, I-V relations, capacitance,
- The MOS transistor
 - First glance, threshold, I-V relations, models
 - Dynamic behavior (capacitances), resistances,
- Process variations

Chip Anatomy

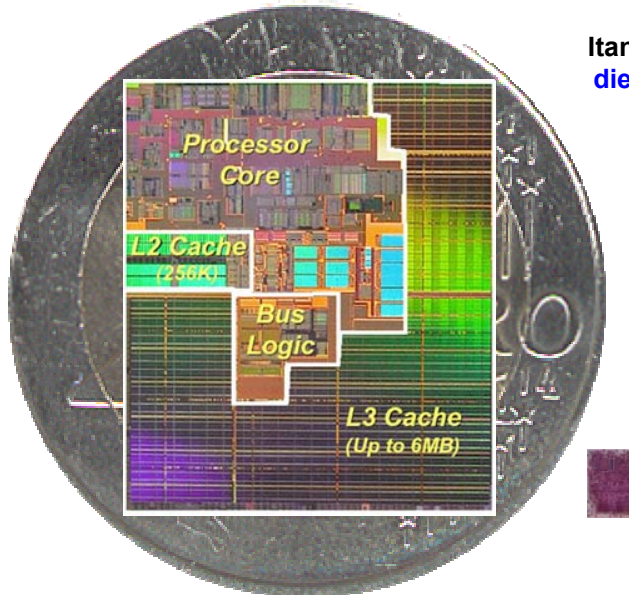


Not 1-to-1, sorry
(Rendering of) result after fabrication

Layout of chip, final design result

Evolution

Intel 4004 (1971) and
Itanium (McKinley, 2002)
die compared to 2€ coin

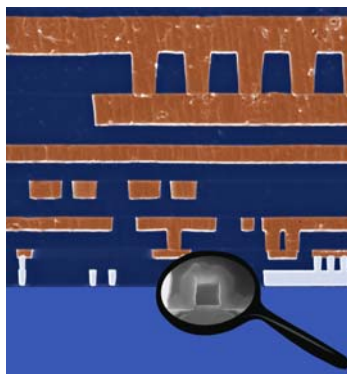


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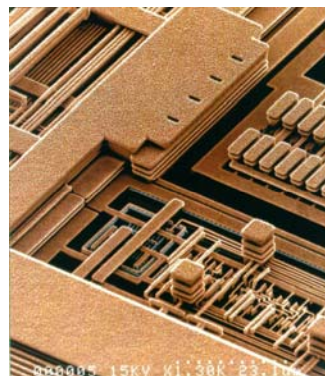
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5

SEM Images



Cross-section



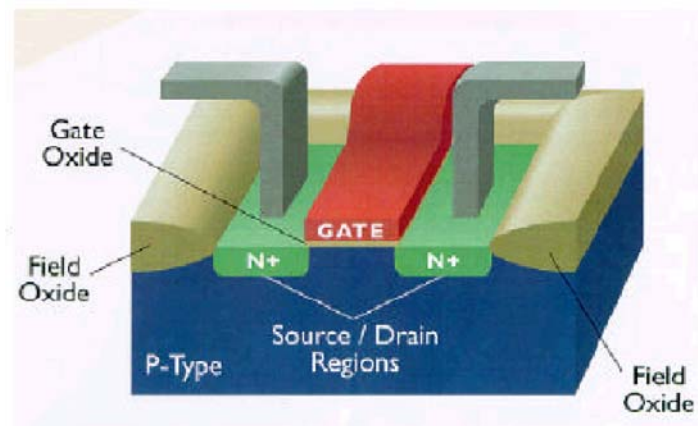
3d perspective

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MOS Transistor 3D Structure

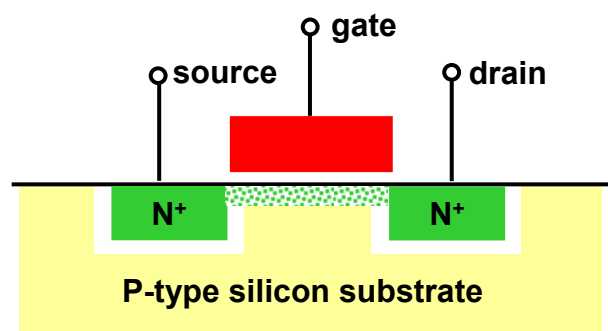


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NMOS Cross-section



- 3 types of conductors
 - Good conductors (metallic)
 - N-type semi-conductors
 - P-type semi-conductors



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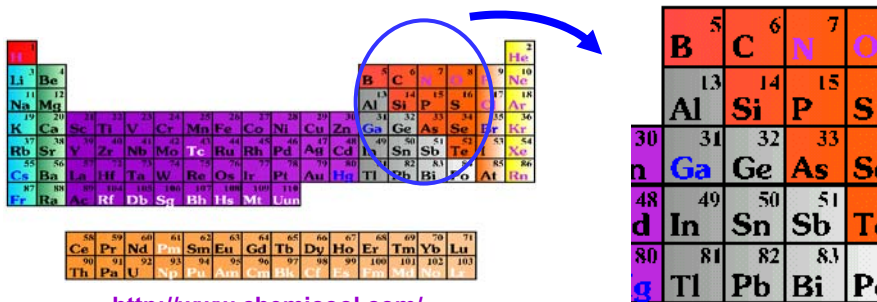
8

What is a Semiconductor?

Material whose **conductivity**, due to **charges of both signs**, is normally in the range between that of metals and insulators and in which the **electric charge carrier density can be changed by external means**.

[<http://goldbook.iupac.org/S05591.html>]

Periodic System

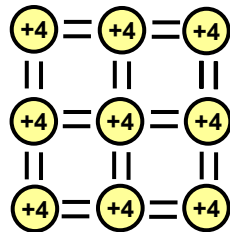


B	C	N	O
13	14	15	
Al	Si	P	S
30	31	32	33
Ga	Ge	As	Se
48	49	50	51
In	Sn	Sb	Te
80	81	82	83
Tl	Pb	Bi	Po

<http://www.chemicool.com/>

Name	Symbol	#	Valence
Silicon	Si	14	4
Boron	B	5	3
Phosphor	P	15	5
Arsenic	As	33	5
Germanium	Ge	32	4

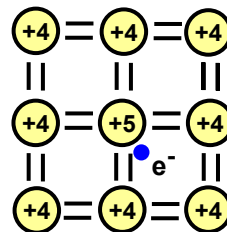
Semiconductor Physics



- Intrinsic Si
- Ideal crystal structure
- Valence 4
- almost no free carriers
- almost no conduction

$$[n] = [p] = n_i = 1,5 \cdot 10^{10} / \text{cm}^3$$

at 300 K for silicon



- doping with valence 5 atoms (Phosphor, Arsenic) introduces "loose electrons"
- electron donor
- conductivity depends on doping level

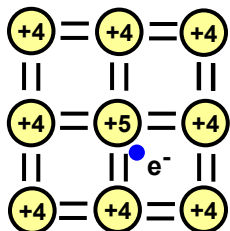
$$n \cdot p = n_i^2 \text{ (in equilibrium)}$$

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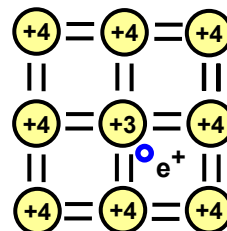
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Semiconductor Physics



- doping with valence 5 atoms (Phosphor, Arsenic) introduces "loose electrons"
- electron donor
- conductivity depends on doping level



- doping with valence 3 atoms (Boron) introduces "loose holes"
- electron acceptors
- hole conductivity lower than electron conductivity

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Semiconductor Physics

Si in equilibrium : $n \cdot p = n_i^2 = 2.25 \times 10^{20}$ at 300K
 Intrinsic Si : $n = p = n_i$

$$N_D \gg N_A$$

Electron donors: As, P
 n-type Si

$$n \approx N_D, p = n_i^2 / n$$

Electrons: majority carriers

Holes: minority carriers

Resistive material

Conductivity depends
 on N_D

$$N_A \gg N_D$$

Electron acceptors: B
 p-type Si

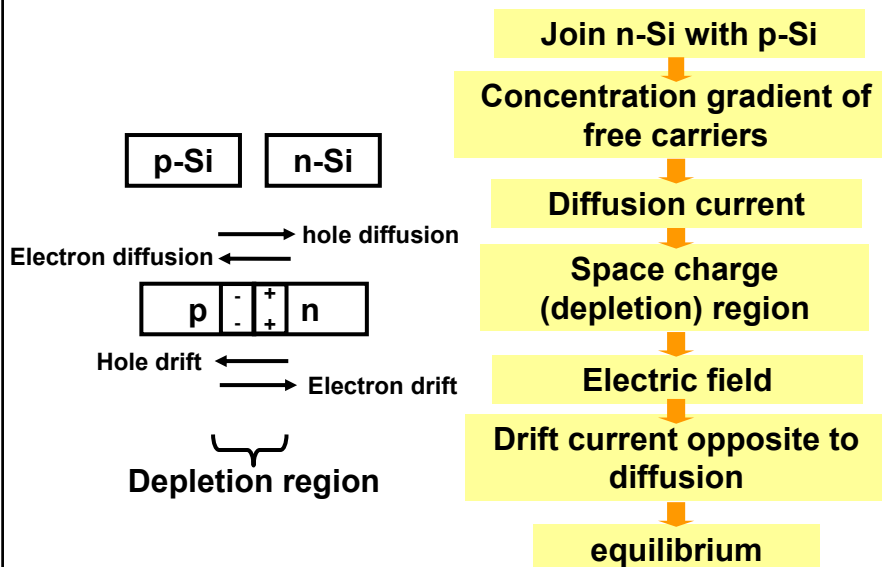
$$p \approx N_A, n = n_i^2 / p$$

Holes: majority carriers

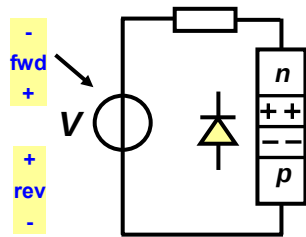
Electrons: minority carriers

Hole conductivity lower
 than electron conductivity

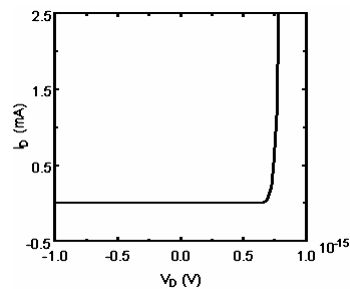
PN junction



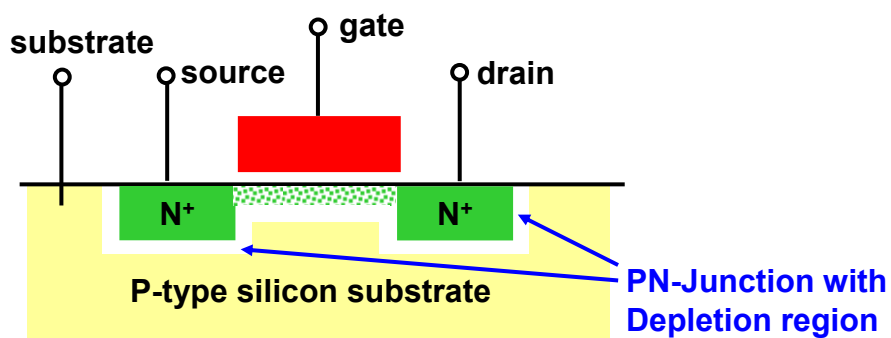
Diode Conduction



- By applying an external voltage, width of depletion region can be changed
- Forward: becomes smaller and smaller, finally **conduction**
- Reverse: becomes wider and wider => **no conduction**

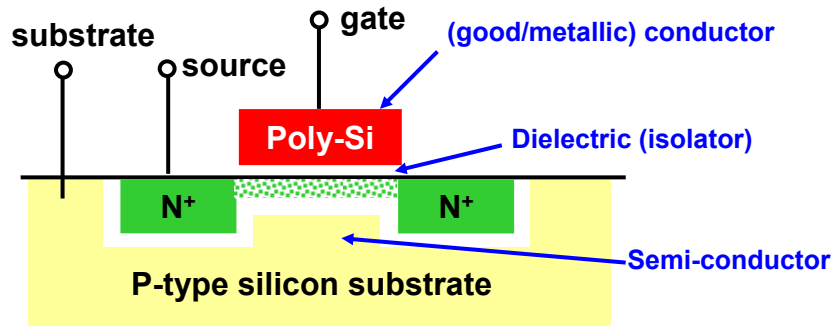


$$I_D = I_S (e^{V_D/\phi_T} - 1)$$



- Drain and source voltage relative to substrate voltage should maintain isolation!
Substrate = Bulk = B, Source = S, Drain = D
 $V_{SB} > 0, V_{DB} > 0$
- Normally the case

MOS Capacitor

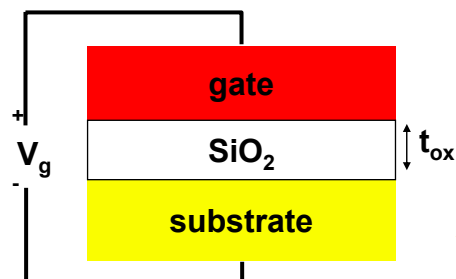


Inversion layer

- Presence of inversion layer depends on voltages relative to substrate
- If present: **conduction** between source and drain

MOSFET gate as capacitor

- Gate capacitance helps determine charge in channel which forms **inversion region**.
- Basic structure of gate is **parallel-plate capacitor**:



$$C_{ox} = \epsilon_{ox} / t_{ox}$$

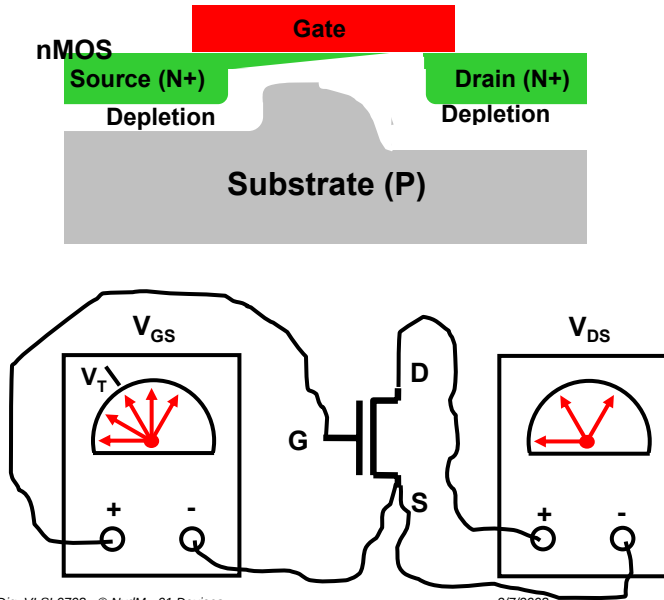
$$\epsilon_{ox} = \epsilon_0 \epsilon_r$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$$

$$\epsilon_r = 3.9 \text{ (SiO}_2\text{)}$$

Note: [F] vs. [F/m²]

nMOS Transistor Operation

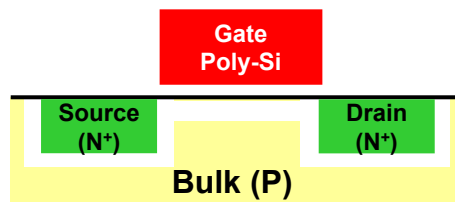


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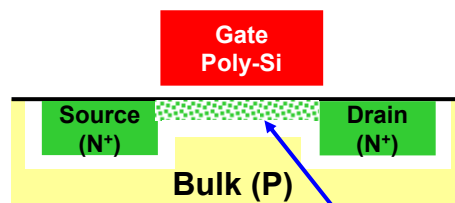
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MOS Summary



- Low gate voltage
- Transistor off



- High gate voltage
- Conduction between source and drain

Channel

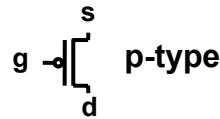
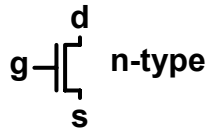
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CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



- | | |
|-----------------------------------|-------------------------------|
| ■ “on” when V_g is high | ■ “on” when V_g is low |
| ■ With n-type s/d | ■ With p-type s/d |
| ■ Electrons (n) as carrier | ■ Holes (p) as carrier |
| ■ Built in p-type Si | ■ Built in n-type Si |



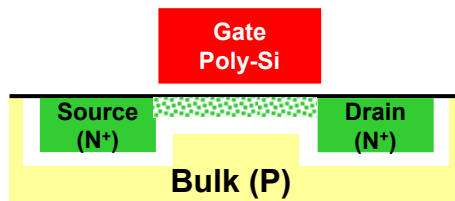
n-well (for PMOS) in p-type substrate (for NMOS)

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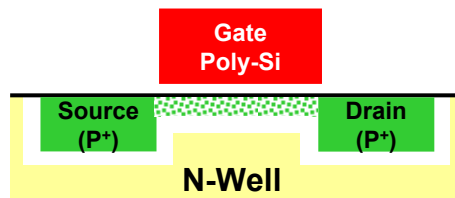
21

NMOS vs PMOS



NMOS

- On when gate voltage is high
- Off when gate voltage is low



PMOS

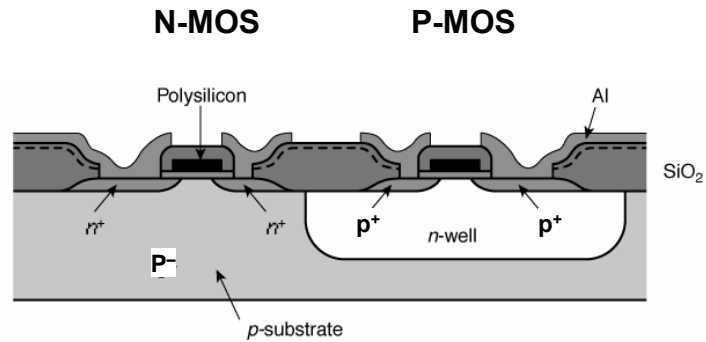
- N and P regions opposite of NMOS
- On when gate voltage is low
- Off when gate voltage is high

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Cross-Section of CMOS Technology

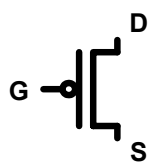
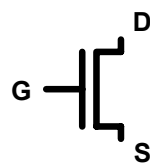


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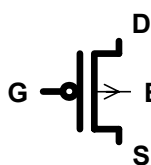
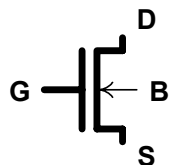
23

MOS Transistors



3-terminal model

bulk assumed to be connected to appropriate supply



4-terminal model

B = bulk (substrate)

NMOS

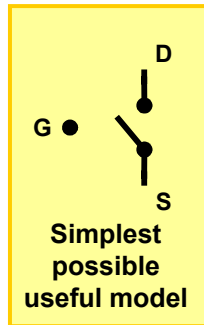
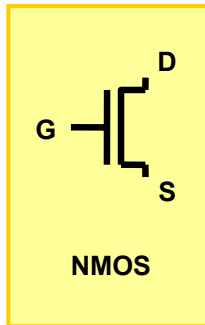
PMOS

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MOS Transistor Switch Level Models



Position of switch depends on gate voltage

V_G	NMOS	PMOS
hi	closed	open
lo	open	closed

- Connection between source and drain depends on gate voltage, current can flow from **source to drain and vice versa** if closed
- No **static** current flows into gate terminal

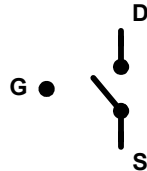
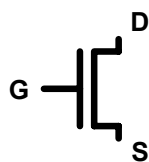
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MOS Transistor Threshold Voltage

Threshold voltage V_T : point at which transistor turns on



Position of switch depends on gate voltage (**relative to source**)

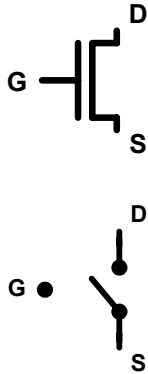
V_{GS}	NMOS	PMOS
$V_{GS} > V_T$	closed	open
$V_{GS} < V_T$	open	closed

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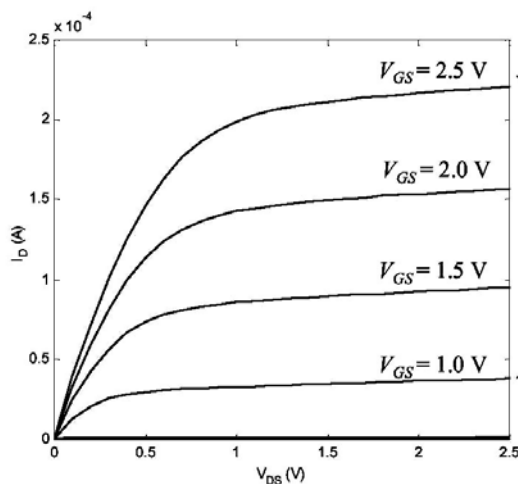
26

Is this all there is?



- You don't believe that (CMOS) life can be so **simple**, do you?
- Discuss some of the things that you would expect to be **non-idealities** of CMOS as a switch
- Since we want to design CMOS circuits, we need a **deeper understanding** of CMOS circuit

Drain Current I_D

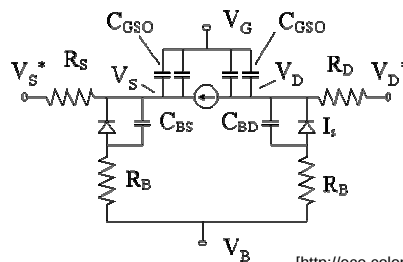


(b) Short-channel transistor ($L_d = 0.25 \mu\text{m}$)

- You might remember quadratic dependence
- Not true anymore for short-channel devices (velocity saturation)

SPICE Model

- Some very advanced models to describe MOS devices over all combinations of terminal voltage
 - Includes dynamic behavior, thermal, ...
 - BSIM3, BSIM4, HICUPS, PSP, **MEXTRAM**, ...
 - Can be used for Circuit Simulation
 - >10k lines of C-code



[<http://ece.colorado.edu/~bart/book/book/index.html>]

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MOS Operating Regimes

- Off
- Saturation
- Linear – Triode – Resistive
- Velocity Saturation
- (Sub-threshold)
- Different formulas for drain current I_D in each region
- You need to understand these principles

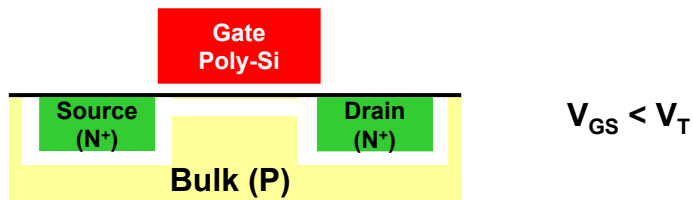


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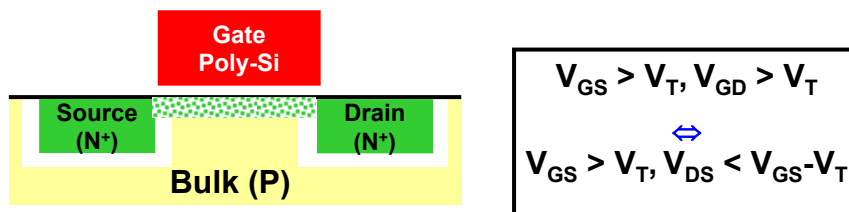
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Off-regime (NMOS)



- Easiest – current I_D is essentially zero
- When V_{GS} approaches V_T , a small current starts to flow (**sub-threshold current**)
Important phenomenon for small, low-voltage devices

Triode-regime (NMOS)



- Inversion both at source-side and drain-side of channel
- I_D depends on V_{DS} : triode behavior
- I_D depends on $V_{GS} - V_T$
- Inversion not completely symmetric if $V_{DS} > 0$

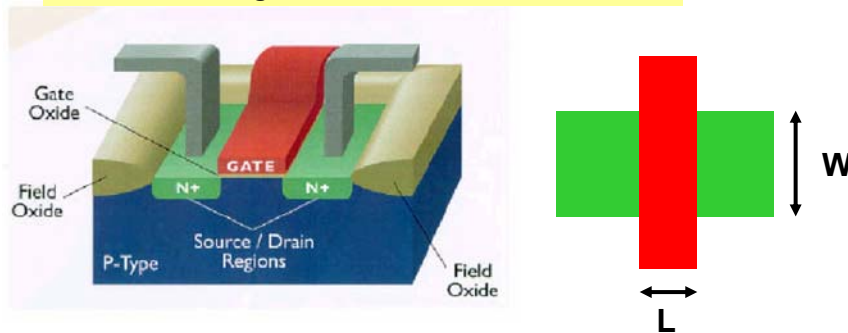
$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

k, V_T : device parameters

Device Sizing

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad k = k' \frac{W}{L}$$

k	Device transconductance
k'	Process transconductance
W	Device width
L	Device length

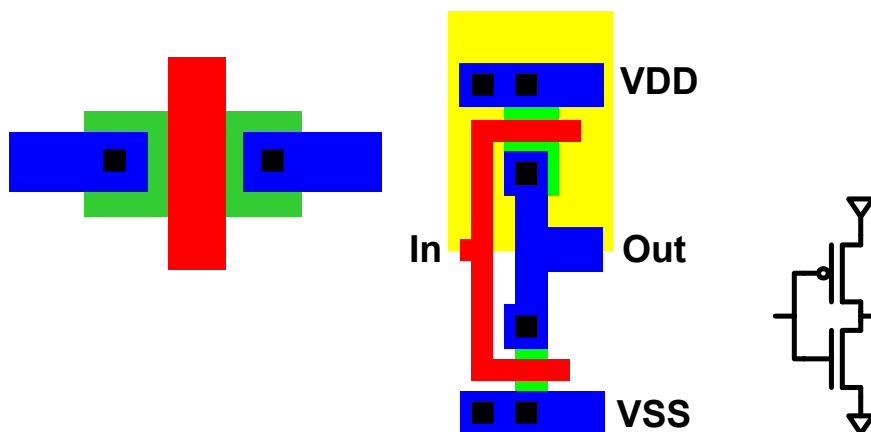


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Device Layout

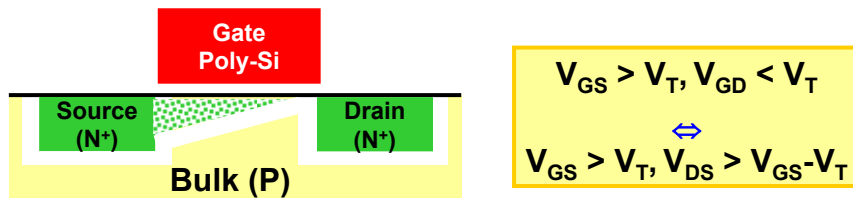


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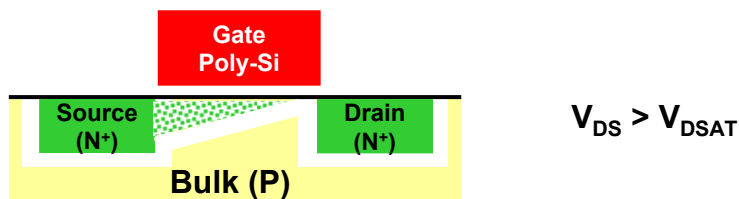
Saturation (NMOS)



- Inversion only at source-side of channel
- Still, current will be flowing between S and D
- Current is (more) independent of V_{DS} : current source behavior

$$I_D = \frac{1}{2} k (V_{GS} - V_T)^2$$

Velocity Saturation



- When V_{DS} large enough – current doesn't increase anymore since carrier velocity is limited by scattering to lattice
- Visible in (advanced) short-channel devices
- Can happen in (otherwise) saturation conditions, but also in triode conditions

$$I_D = k \left[(V_{GS} - V_T) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 \right] \quad (k, V_T, V_{DSAT}: \text{device data})$$

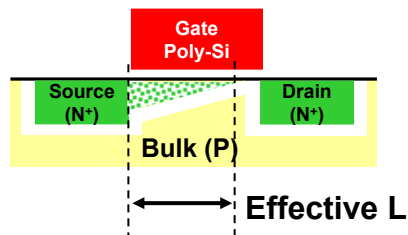
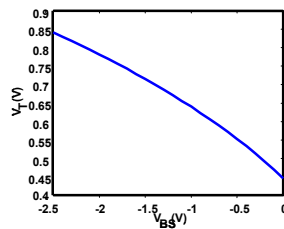
More Effects

- **Body Effect:** V_T depends on V_{SB}

$$V_T = V_{T0} + \gamma \left(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right)$$

- **Channel length Modulation:**
 I_D depends on V_{DS} also in saturation

$$I_D = I_{D0} \times (1 + \lambda V_{DS})$$



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Summary

$$I_D = \begin{cases} k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\ \frac{1}{2} k (V_{GS} - V_T)^2 & V_{GS} > V_T, V_{DS} > V_{GS} - V_T \\ k \left[(V_{GS} - V_T) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 \right] & V_{DS} > V_{DSAT} \end{cases}$$

$$I_D = I_{D0} \times (1 + \lambda V_{DS})$$

$$V_T = V_{T0} + \gamma \left(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right)$$

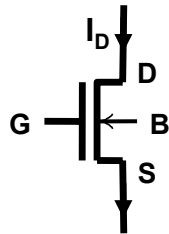
Next slide presents alternative formulation

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MOS Models for Manual Analysis



determined by circuit

$$V_{DS}, V_{GS}, V_{SB}$$

determined by designer

$$W, L$$

determined by technology

$$k', \lambda, V_{DSAT}, V_{T0}, \gamma, \phi_F$$

MOS model for manual analysis

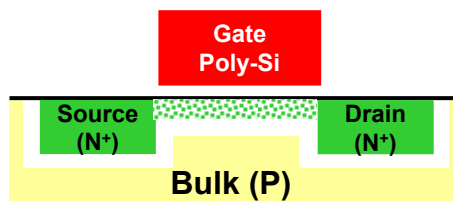
$$I_D = k(V_{GT}V_{MIN} - 0.5V_{MIN}^2)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$

$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = \min(V_{DS}, V_{GT}, V_{DSAT}) \quad k = k' \frac{W}{L}$$

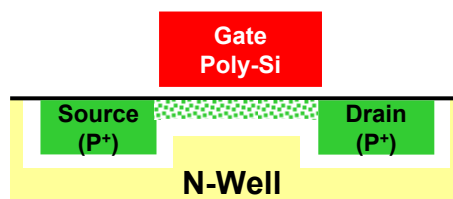
$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F})$$

NMOS vs PMOS



NMOS

- On when gate voltage is high
- Off when gate voltage is low

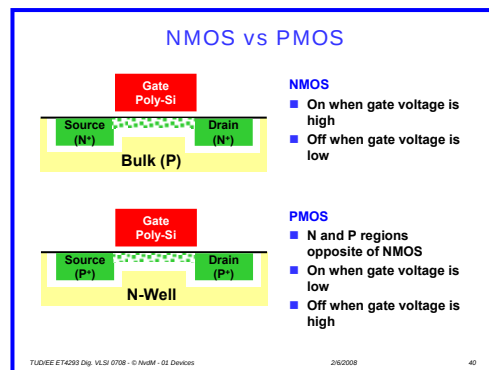


PMOS

- N and P regions opposite of NMOS
- On when gate voltage is low
- Off when gate voltage is high

NMOS vs PMOS

- PMOS: all polarities reversed for same operation region
- Hole-mobility < Electron-mobility
- $|k'_{\text{PMOS}}| < k'_{\text{NMOS}}$



NMOS Regions of Operation

Triode	$\Leftrightarrow$	$V_{gs} > V_t$ and $V_{ds} < V_{gs} - V_t$
Saturation	$\Leftrightarrow$	$V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$
Cut-off	$\Leftrightarrow$	$V_{gs} \leq V_t$

PMOS Regions of Operation

Triode	$\Leftrightarrow$	$V_{gs} < V_t$ and $V_{ds} > V_{gs} - V_t$
Saturation	$\Leftrightarrow$	$V_{gs} < V_t$ and $V_{ds} < V_{gs} - V_t$
Cut-off	$\Leftrightarrow$	$V_{gs} \geq V_t$

Universal

Triode	$\Leftrightarrow$	$ V_{gs} > V_t $ and $ V_{ds} < V_{gs} - V_t $
Saturation	$\Leftrightarrow$	$ V_{gs} > V_t $ and $ V_{ds} > V_{gs} - V_t $
Cut-off	$\Leftrightarrow$	$ V_{gs} \leq V_t $

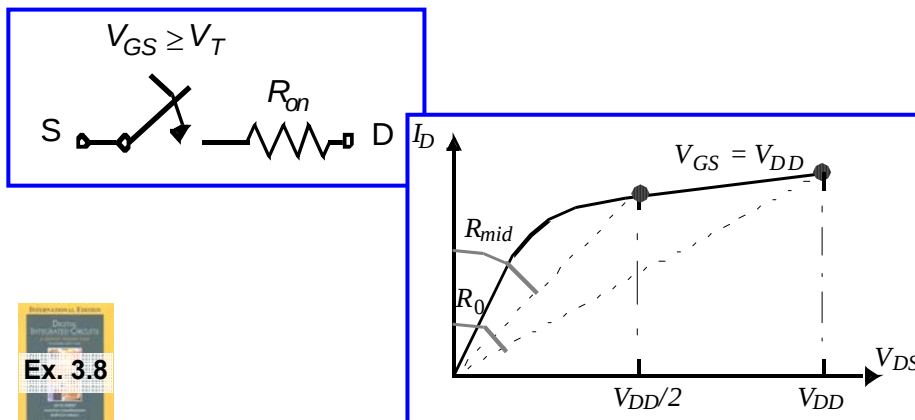
Unified Model Parameters

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($\text{V}^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

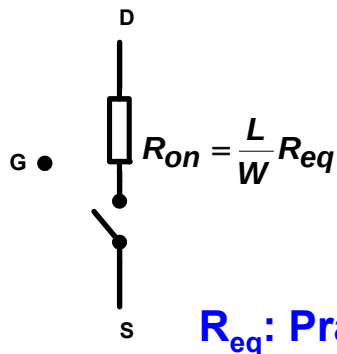
- Parameters depend on **technology**
- See tables in **front and back cover** of book

The Transistor as a Switch



$$R_{eq} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

MOS Transistor Switch Level Model (Empirical).



Position of switch depends on gate to source voltage

V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

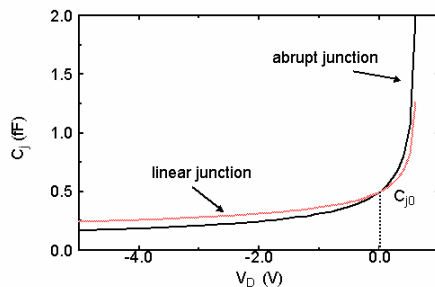
$R_{eq} \setminus V_{dd} (V)$	1	1.5	2	2.5
NMOS ($k\Omega$)	35	19	15	13
PMOS ($k\Omega$)	115	55	38	31

Dynamic Behavior

- (Solely) governed by **time needed to (dis)charge** (intrinsic, parasitic) **capacitances** associated with device and interconnect
- **Essential knowledge** for designing high-quality ckts.
- Many caps are **non-linear**
- **Spice models** can accurately take C into account
- Need **simplification** and insight for *design*
 - Linearization
 - Lumping/merging

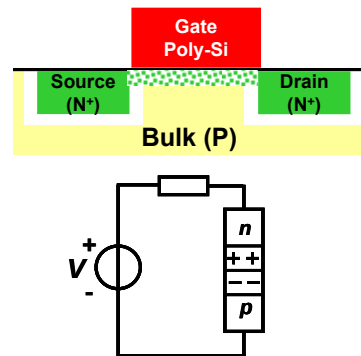


Junction Capacitance



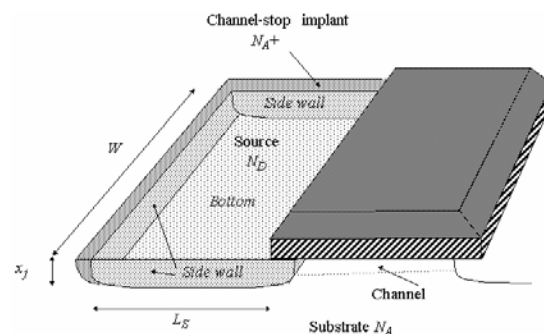
$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction



- Space-charge / depletion region creates electric field
- Electric field energy works like capacitor (energy is $\frac{1}{2}CV^2$)
- Width of depletion region depends on voltage: non-linear C

MOS S/D Capacitance



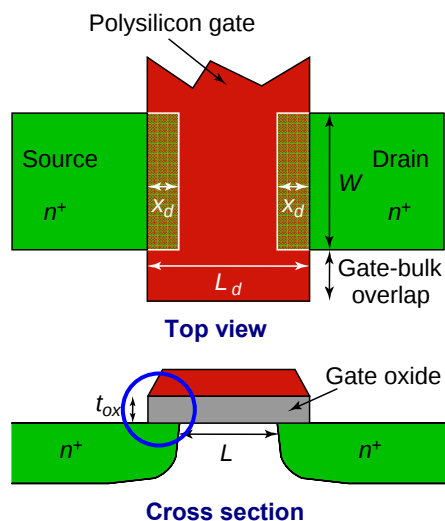
$$\begin{aligned}
 C_{diff} &= C_{bottom} + C_{sidewall} \\
 &= C_j \times AREA + C_{jsw} \times PERIMETER \\
 &= C_j L_s W + C_{jsw} (2L_s + W)
 \end{aligned}$$

Diode capacitances $\Rightarrow$ use linearized values

Gate Capacitance

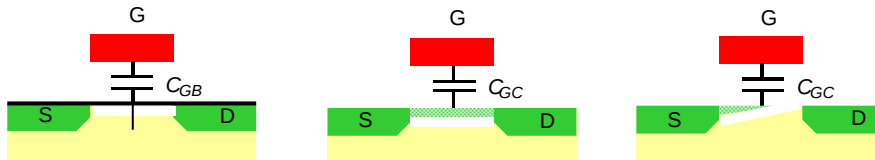
- **Gate-to-channel**
 - Complex function of operating voltages
 - Because channel charge depends on voltages
- **Gate-source** and **gate-drain** overlap capacitance
 - Just (almost) linear capacitances depending only on geometry

Gate-Overlap Capacitance



$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} WL$$

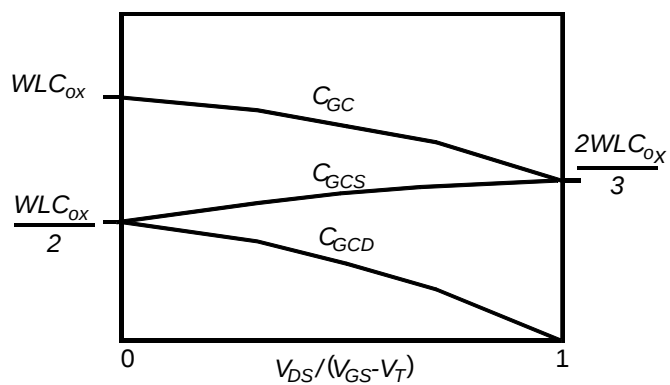
Gate-Channel Capacitance



Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

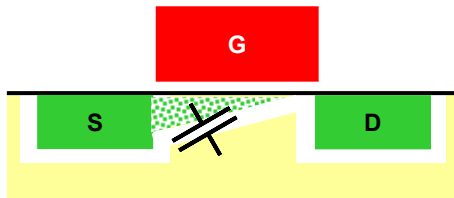
**Most important regions in digital design:
saturation and cut-off**

Gate-Channel Capacitance



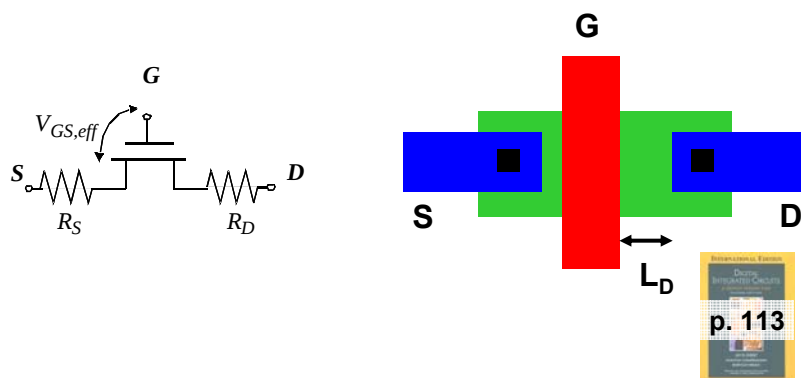
Degree of saturation

Channel-Bulk Capacitance

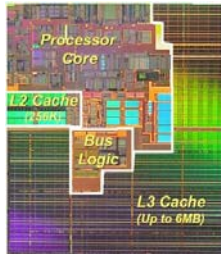


- Channel-bulk cap C_{CB}
- Only when transistor is on
- Parallel to C_{SB}

Device Parasitic Resistance

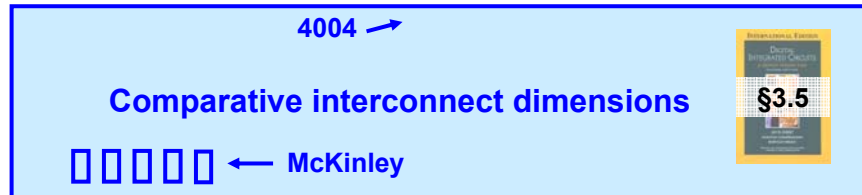


Technology Scaling



McKinley 4004

Processor	4004	McKinley	Montecito
Year	1971	2002	2005
Feat. size	10 μ m	0.18 μ m	90nm
Die size	12mm ²	421mm ²	596mm ²
Transistors	2300	221x10 ⁶	1.7x10 ⁹ 91% in L3 cache
Clock	108 kHz	1GHz	1.8GHz
Perform. (spec2000)	0.01	810	~1600

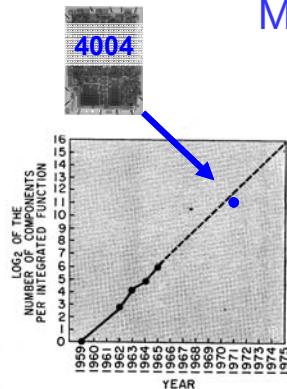


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Moore's Law



The number of transistors that can be integrated on a single chip will double every 18 months

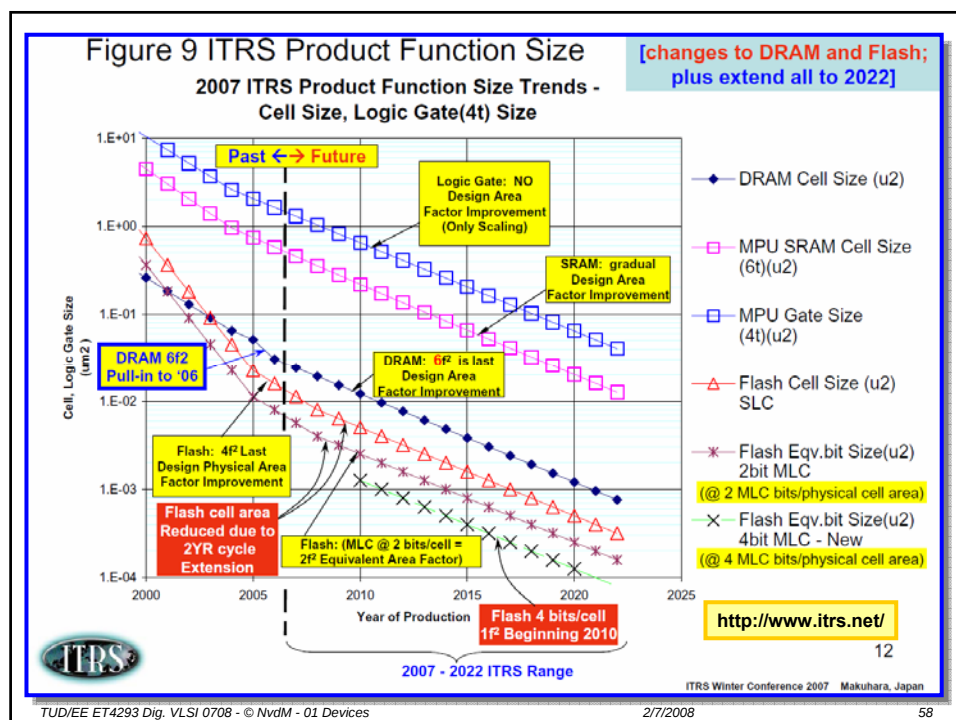
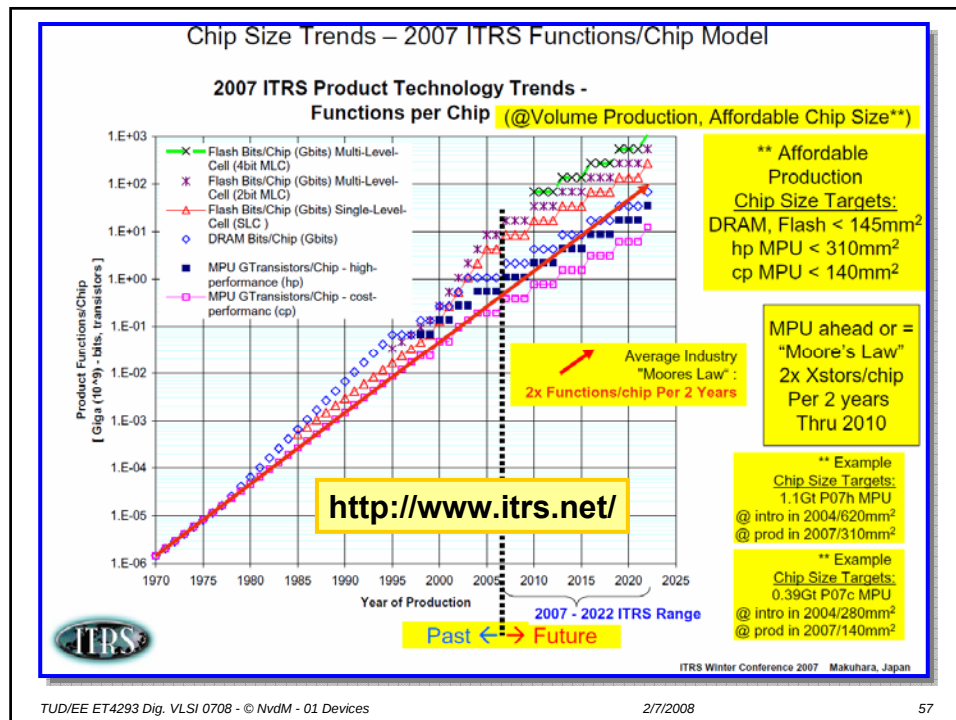
Gordon Moore, co-founder of Intel
[Electronics, Vol 38, No. 8, 1965]



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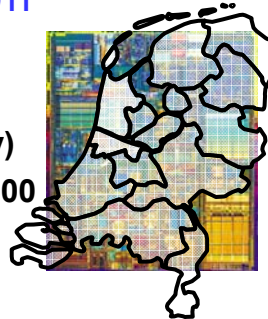
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IC Technology—Comparison

Chip: 4 cm^2
 Netherlands: $40,000 \text{ km}^2$ (approximately)
 Scale: $2 \text{ cm} / 200 \text{ km} = 1:10,000,000$



A chip compares to
 Netherlands full of roads:

0.9 meters wide
 0.9 meters apart
 8 layers



IC Technology Scaling

Scaling improves density and **performance**

■ First order **scaling theory**

		<u>2000 / 1971</u>
■	dimensions, voltage	$1/S$ 0.02
■	intrinsic delay	$1/S$ 0.02
■	power per transistor	$1/S^2$ 0.0004
■	power-delay product	$1/S^3$ 0.000008

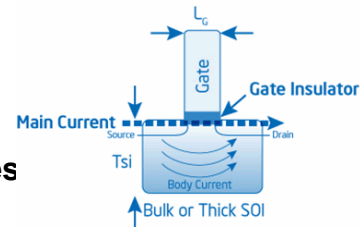
■ **Scaling trend**



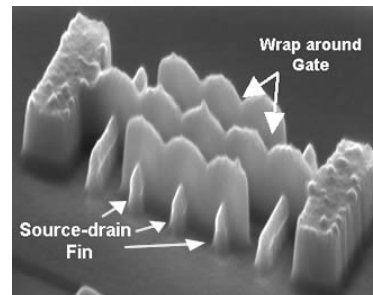
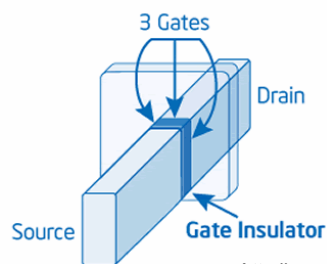
Advanced Issues

- Variability, manufacturing tolerances
- Scaling
- Reliability
- Advanced device architectures

Power Leakage on a Planar Transistor



Tri-Gate: Surrounding the Channel



<http://www.intel.com/technology/silicon/tri-gate-demonstrated.htm>

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Devices – Summary

- Intuitive understanding of device operation
- Static behavior
 - Models for manual analysis
 - Switch model
 - Spice model
- Dynamic behavior (capacitances)
- Parasitic resistances
- Scaling
- Advanced issues

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