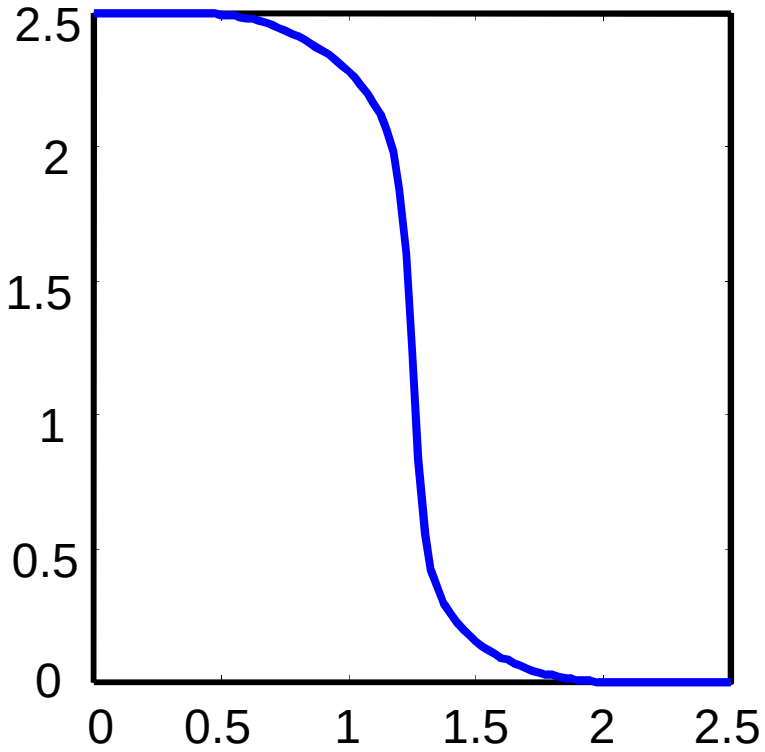
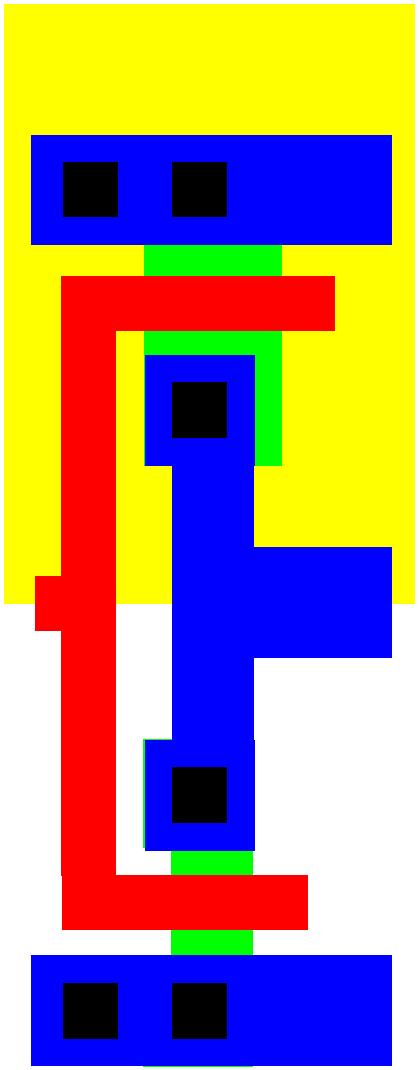
Module 4

CMOS INVERTER





Course Material for Inverter

Chapter 5, 2nd ed.

P = primair, I = Illustratie, O = overslaan

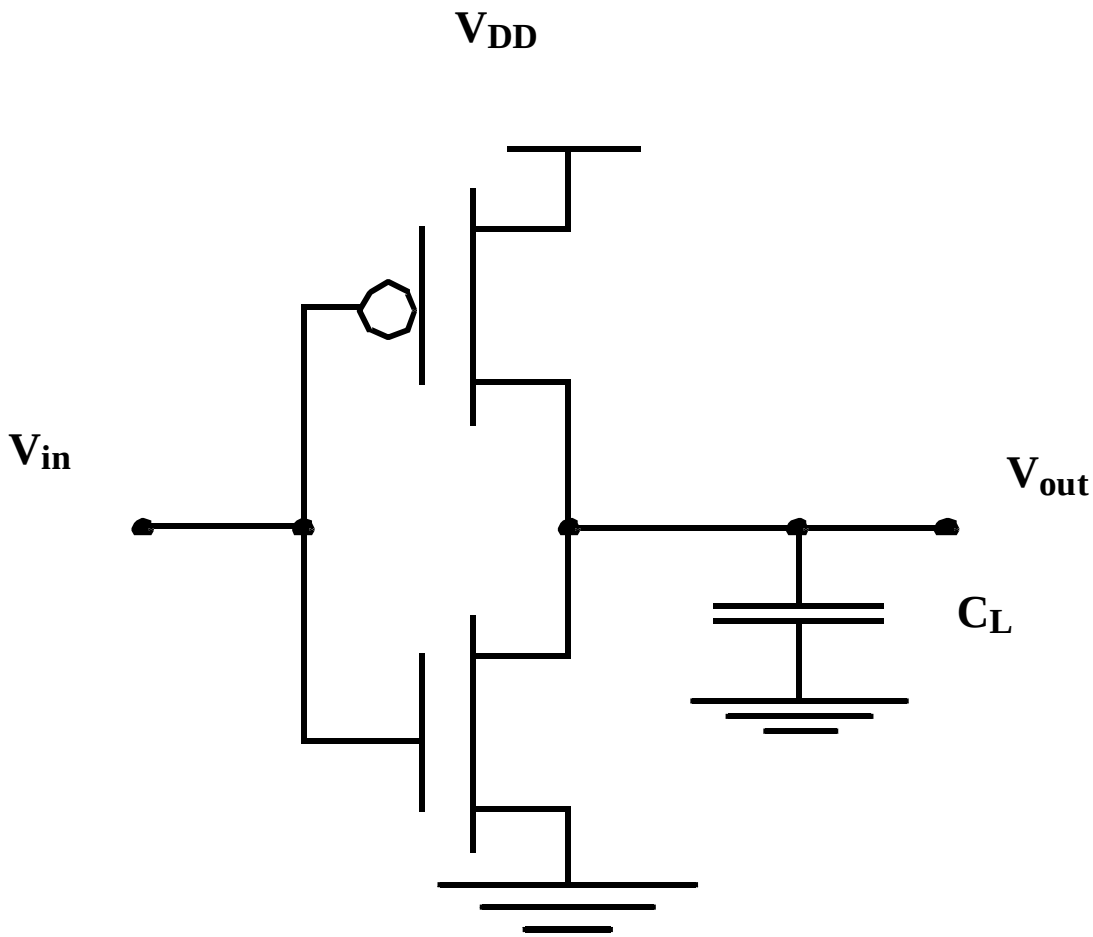
P	5.1	Introduction	180
P	5.2	The Static CMOS inverter - intuitive	181 – 184
P	1.3.2	Functionality and Robustness	18 – 27
P	5.3	Evaluating the Robustness ...	184 – 191
I	5.3.3	Robustness Revisited	191 – 193
P	1.3.3	Performance	27 – 30
I	5.4	Performance of the CMOS inverter	193 – 213
P	1.3.4	Power and Energy Consumption	30 – 31
I	5.5	Power, Energy, and Energy-Delay	213 – 223
O	5.5.2	Static Consumpti	223 – 225
O	5.5.3	Putting it All Toge	225 – 227
O	5.5.4	Analyzing Power Consumption using SPICE	227 – 229.
O	5.6	Perspective: Technology scaling…	229 – 231
P	5.7	Summary	232 – 233

+Primair: pp. 214-215

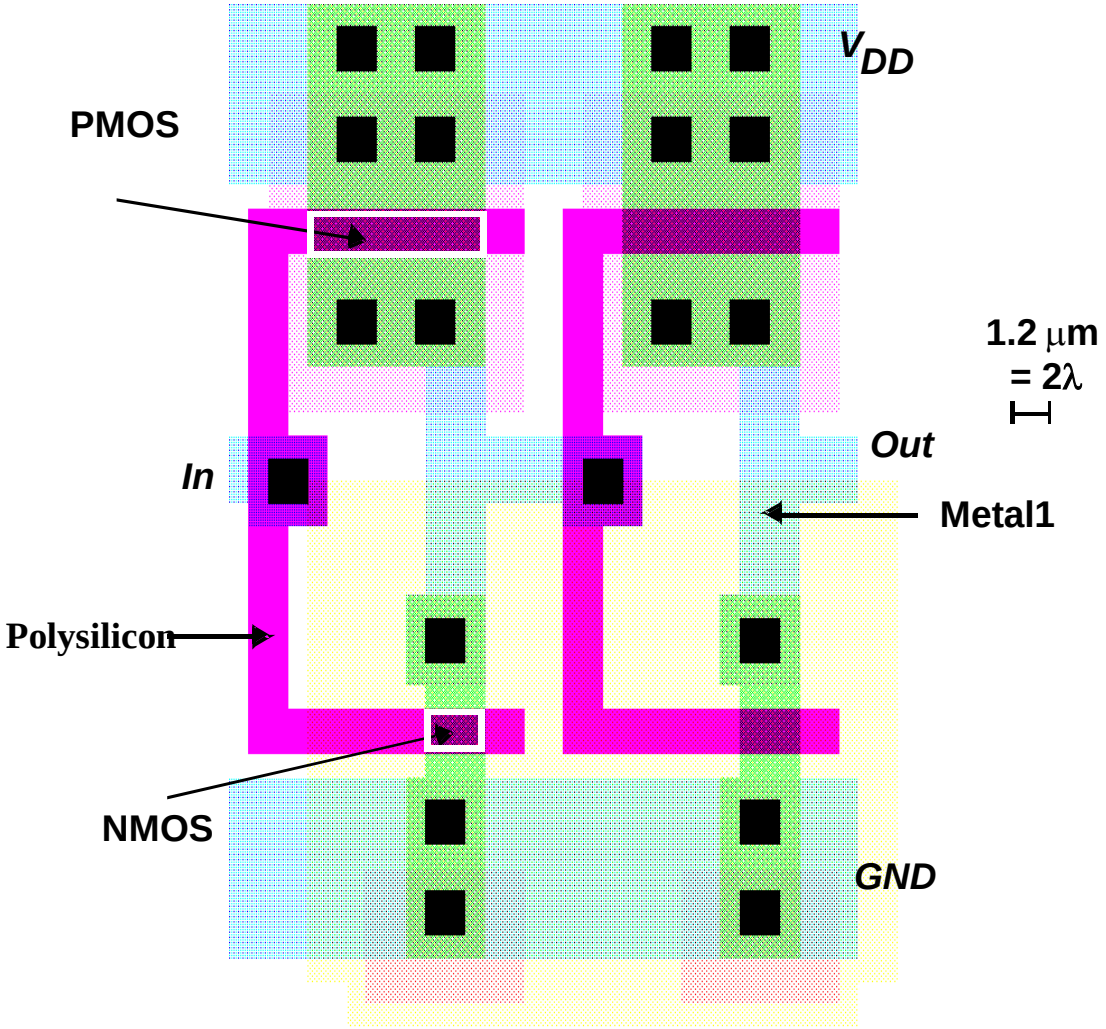
The CMOS Inverter - Outline

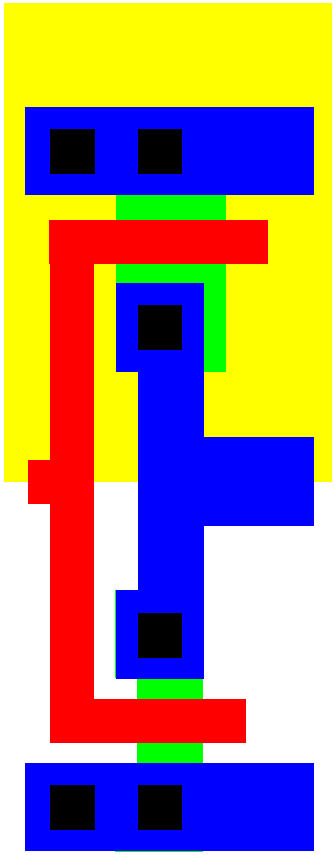
- First Glance
- Digital Gate Characterization
- Static Behavior (Robustness)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance)
  - Capacitances
  - Delay
- Power
  - Dynamic Power, Static Power, Metrics

The CMOS Inverter: A First Glance

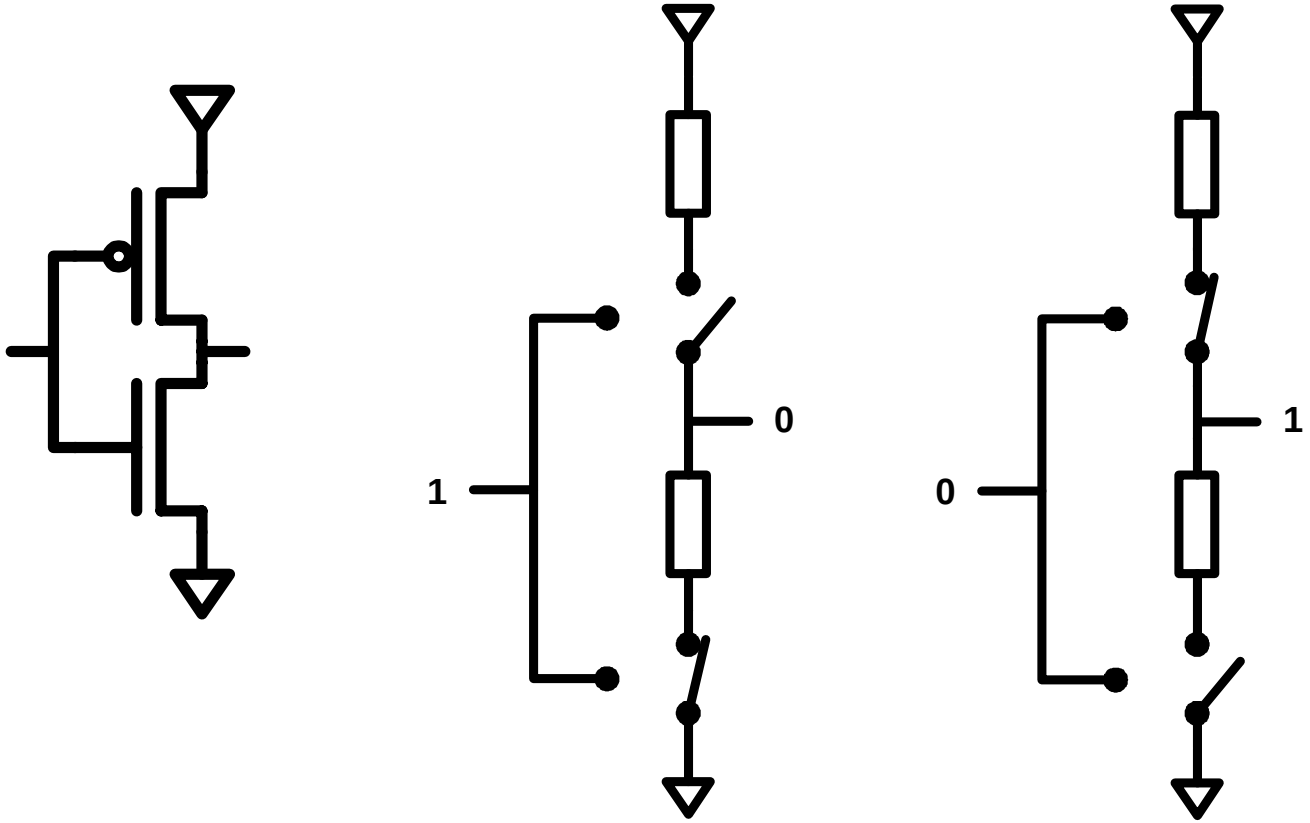


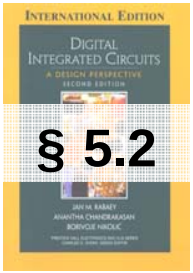
CMOS Inverters (1)





CMOS Inverter Operation Principle



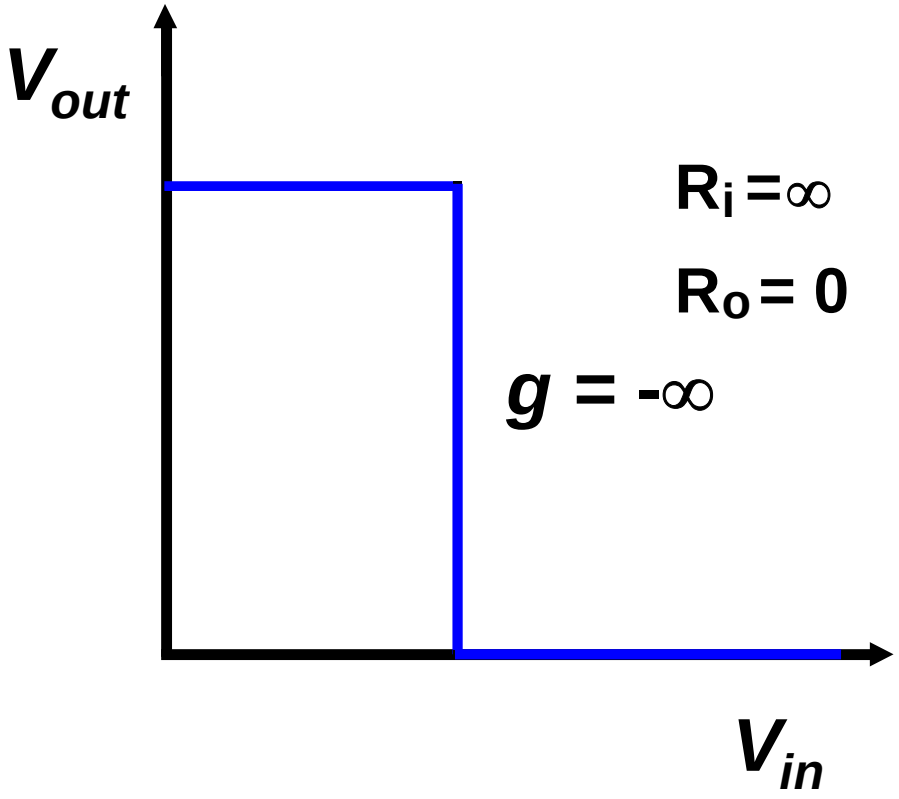


$V_{OH} = V_{DD}$ $V_{OL} = 0$

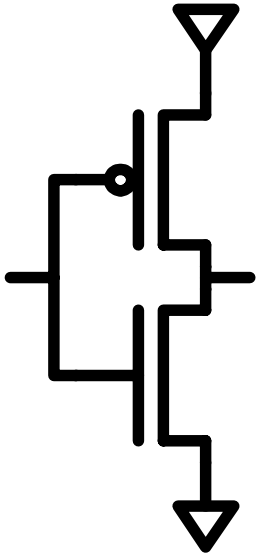
Digital Gate Fundamental Parameters

- **Functionality**
- **Reliability, Robustness**
- **Area**
- **Performance**
  - **Speed (delay)**
  - **Power Consumption**
  - **Energy**

The Ideal Inverter

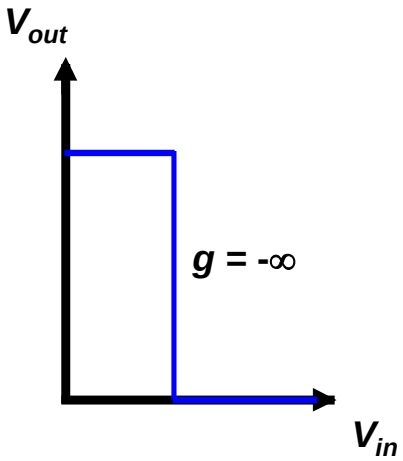


Static CMOS Properties.



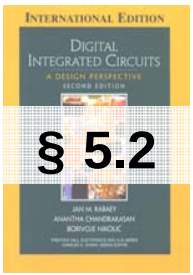
Basic inverter belongs to class of static circuits: output always connected to either V_{DD} or V_{SS}. Not ideal but:

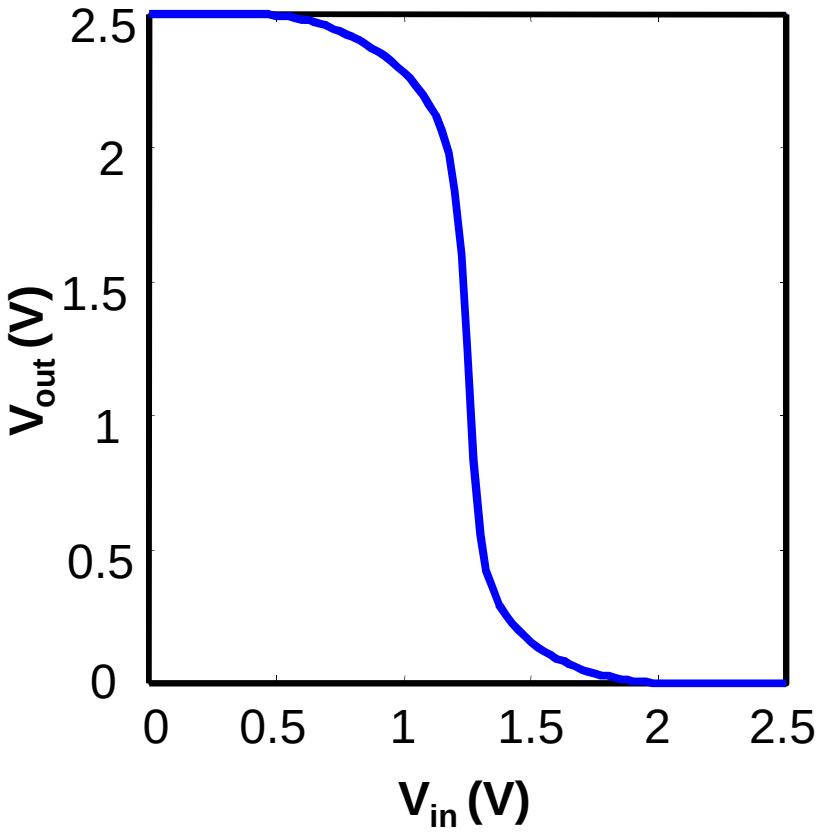
- **Rail to rail voltage swing**
- **Ratio less design**
- **Low output impedance**
- **Extremely high input impedance**
- **No static power dissipation**
- **Good noise properties/margins**



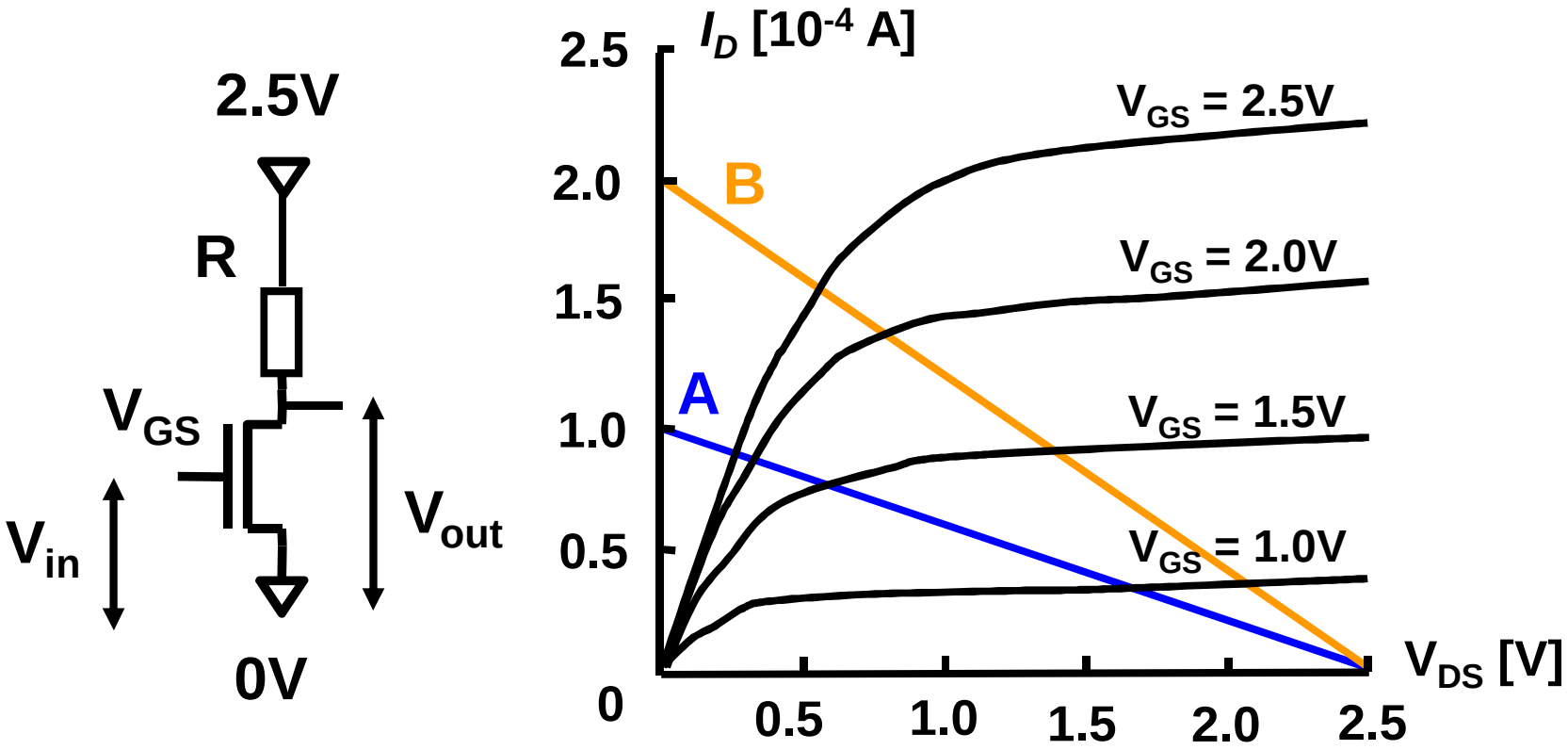
Exercise: prioritize the list above

Voltage Transfer Characteristic (VTC)





Load Line (Ckt Theory)



Exercise:

The blue load line A corresponds to R =

The orange load line B corresponds to R =

With load line A and V_{GS} = 1V, V_{out} =

Draw a graph $V_{out}(V_{in})$ for load line A and B

PMOS Load Lines

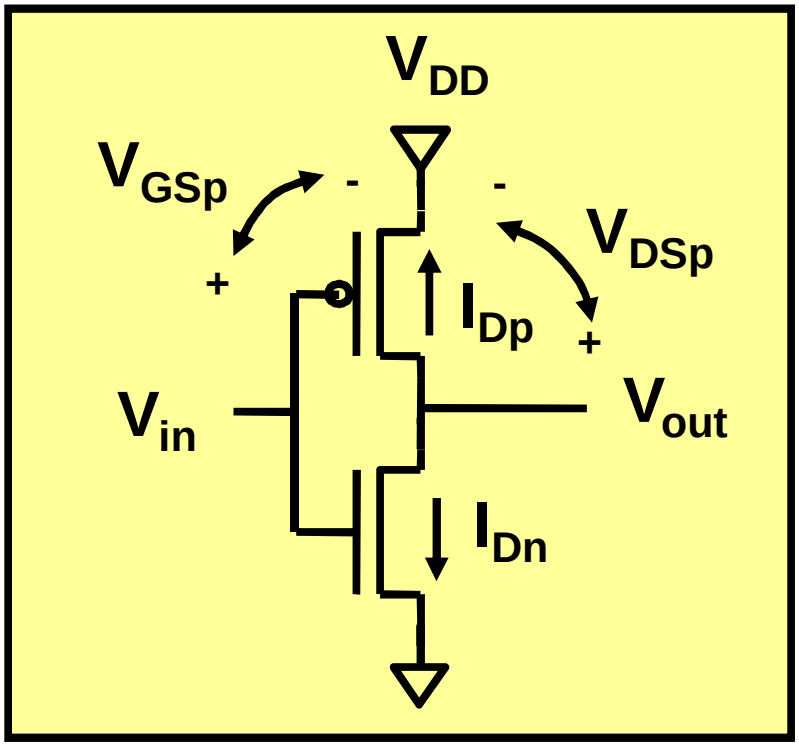
Goal: Combine I_{Dn} and I_{Dp} in one graph

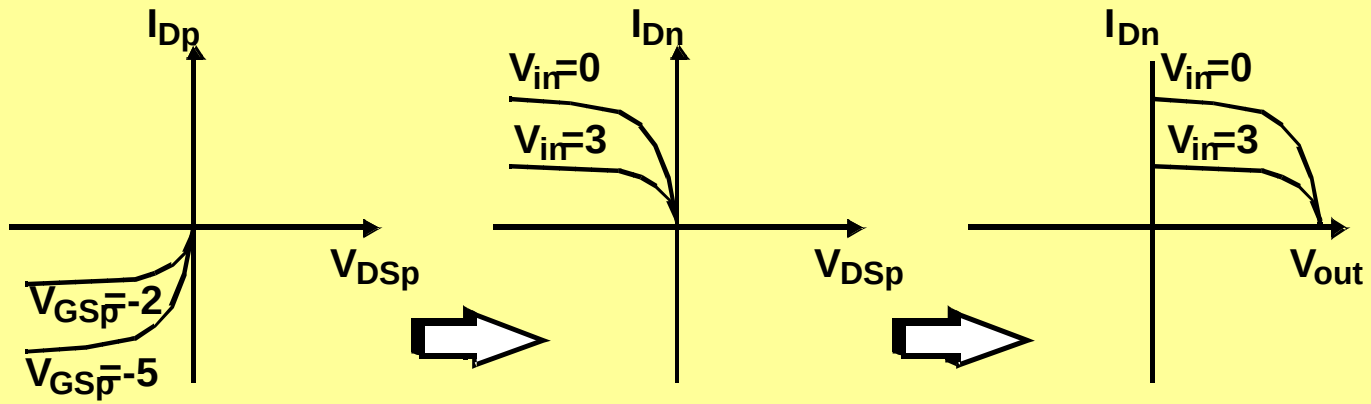
Kirchoff:

$V_{in} = V_{DD} + V_{GSp}$

$I_{Dn} = - I_{Dp}$

$V_{out} = V_{DD} + V_{DSp}$





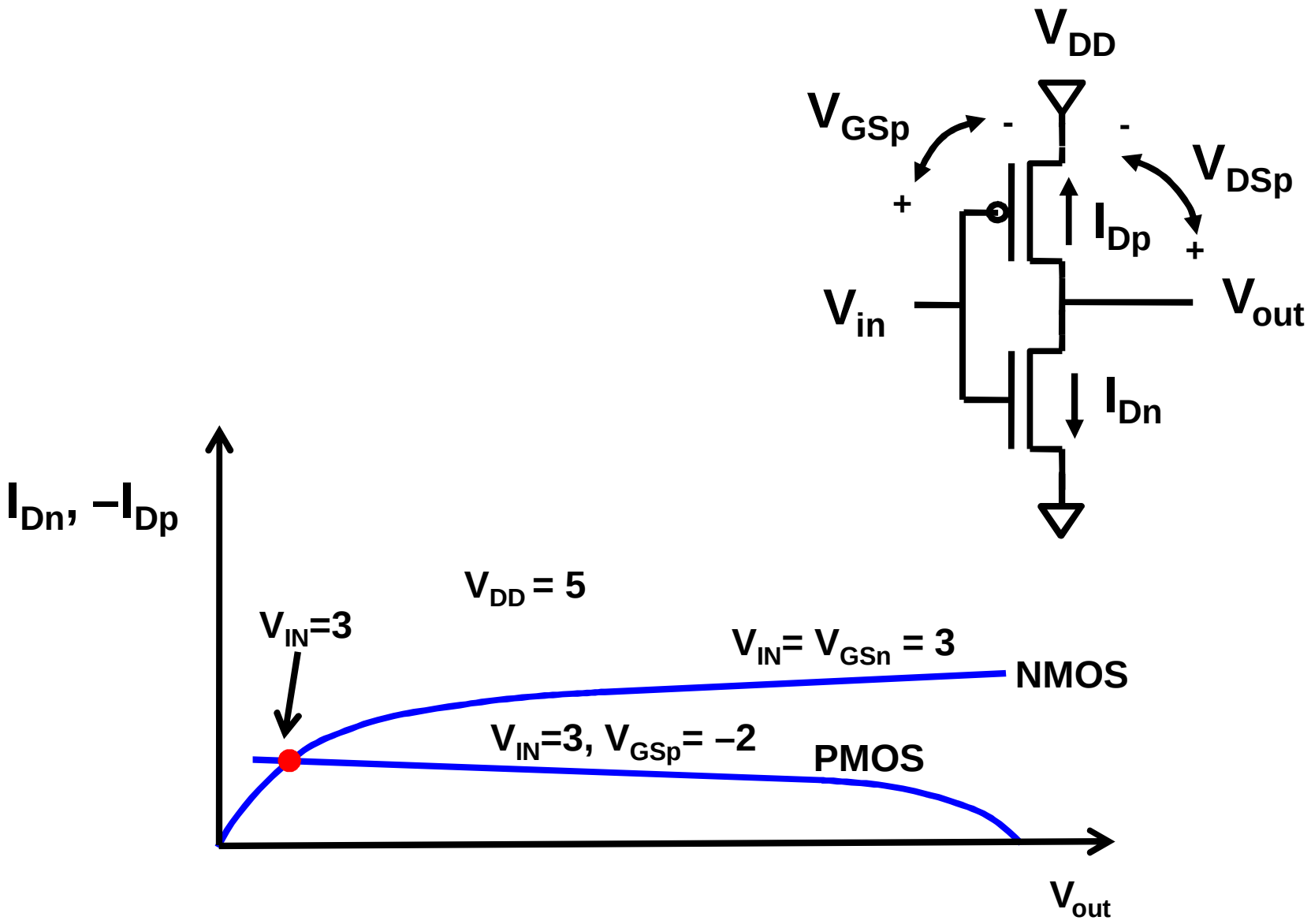
Example: V_{DD}=5V

$V_{in} = V_{DD} + V_{GSp}$

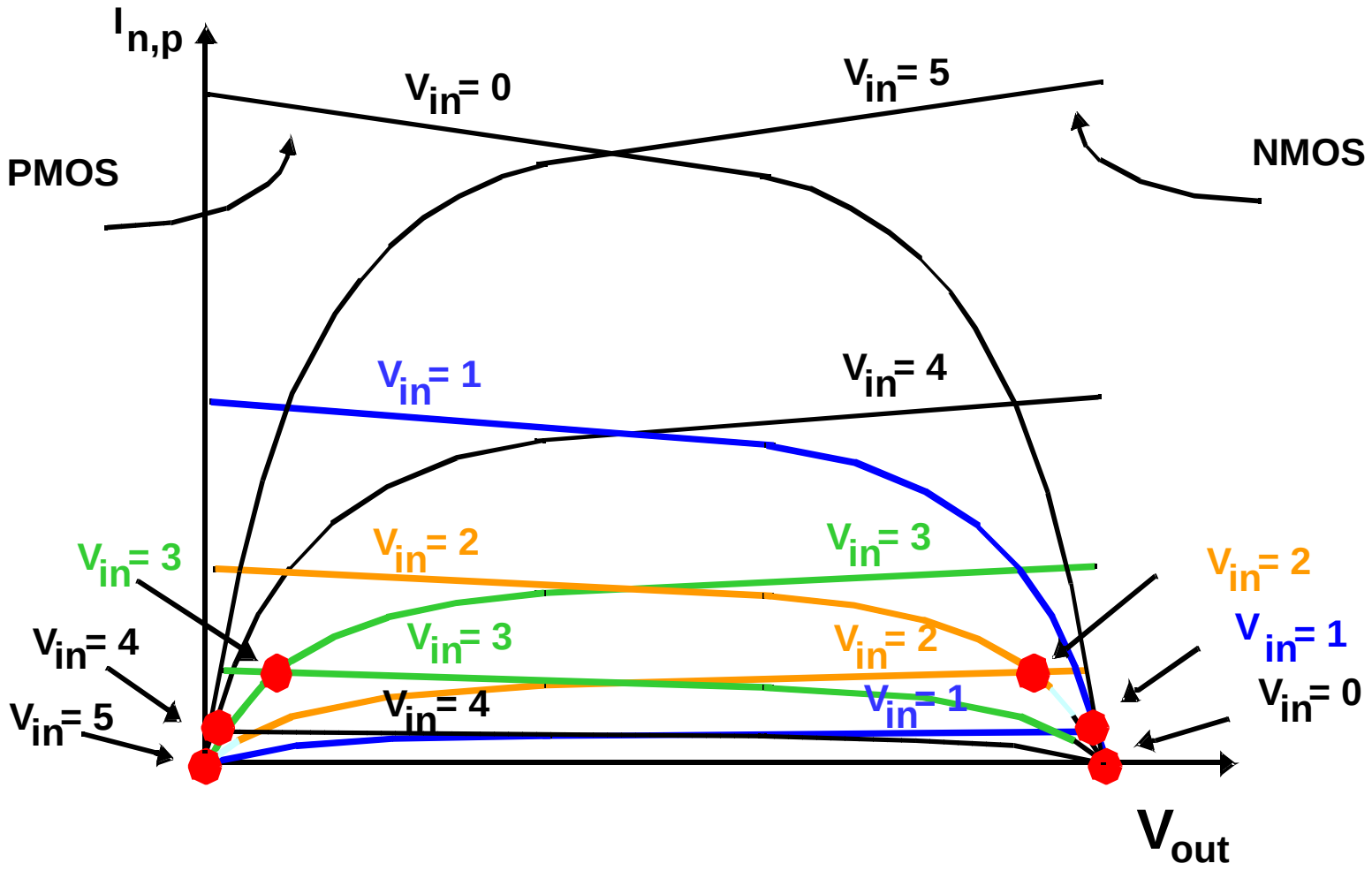
$I_{Dn} = - I_{Dp}$

$V_{out} = V_{DD} + V_{DSp}$

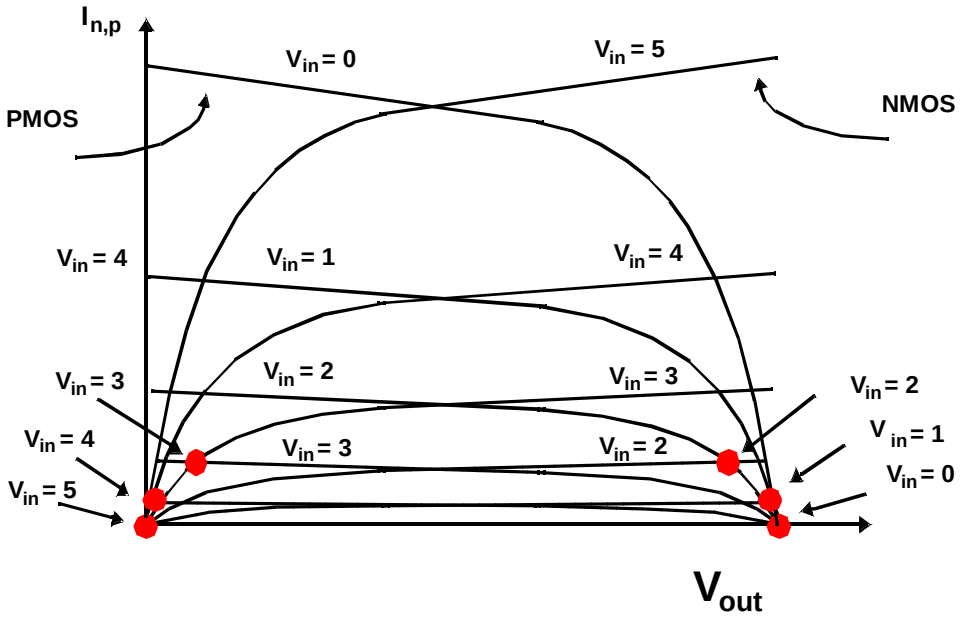
CMOS Inverter Load Characteristics

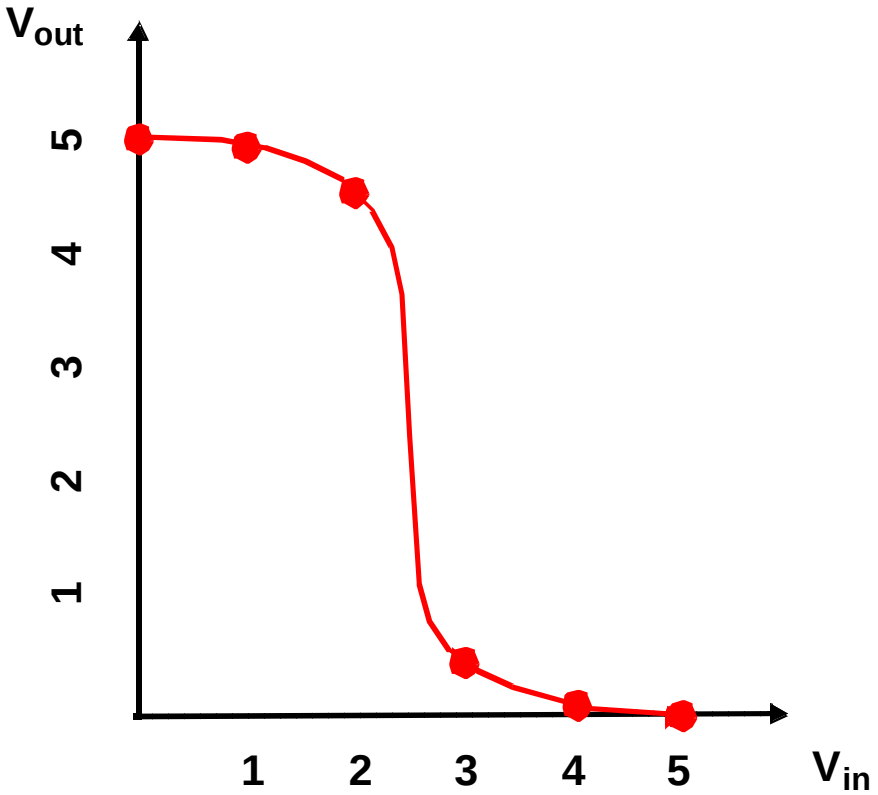


CMOS Inverter Load Characteristics



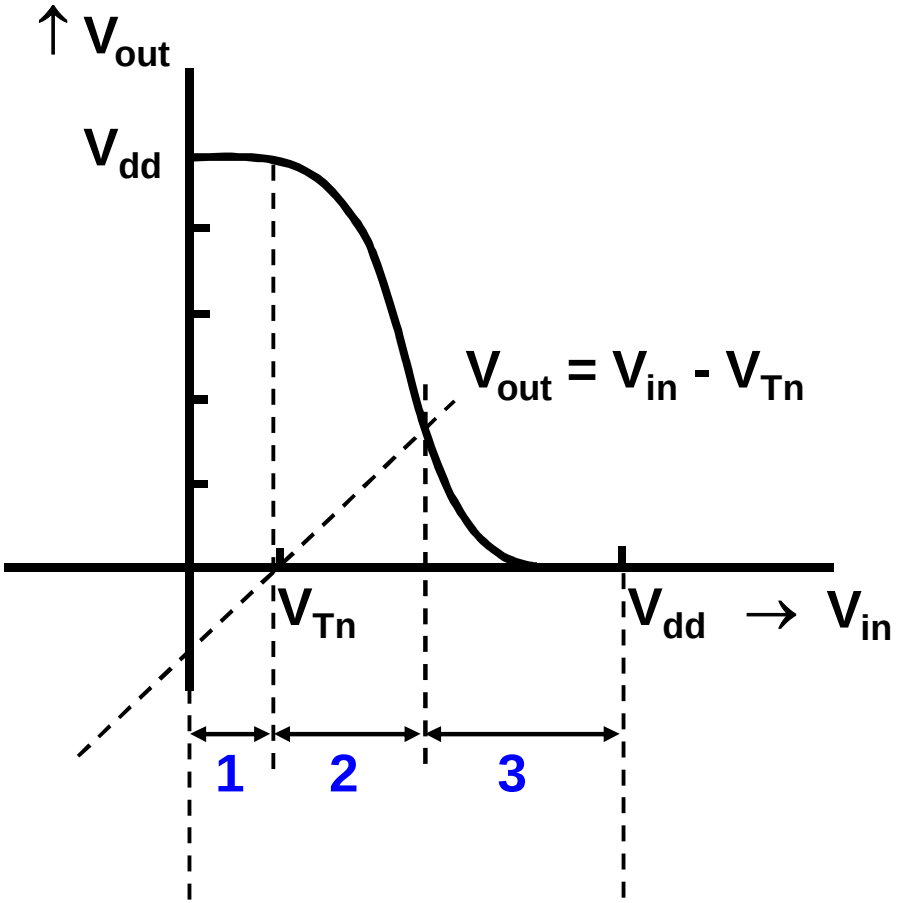
CMOS Inverter VTC.





NMOS Operating Conditions

Need to know for proper dimensioning, analysis of noise margin, etc.



NMOS

1 $V_{in} = V_{GS} < V_{Tn} \Rightarrow$ **off**

2 $V_{out} > V_{in} - V_{Tn}$

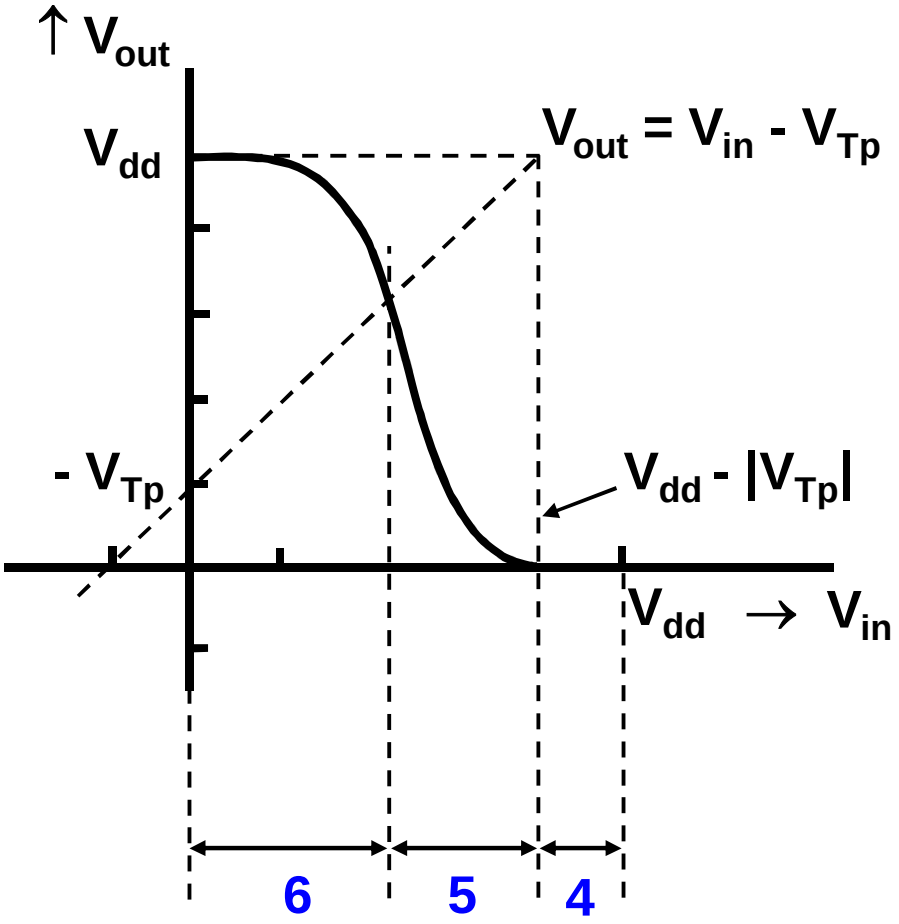
$V_{DS} > V_{GS} - V_{Tn}$

$V_{GD} < V_{Tn} \Rightarrow$ **saturation**

3 $V_{out} < V_{in} - V_{Tn} \Rightarrow$ **resistive**

PMOS Operating Conditions

Need to know for proper dimensioning, analysis of noise margin, etc.



PMOS

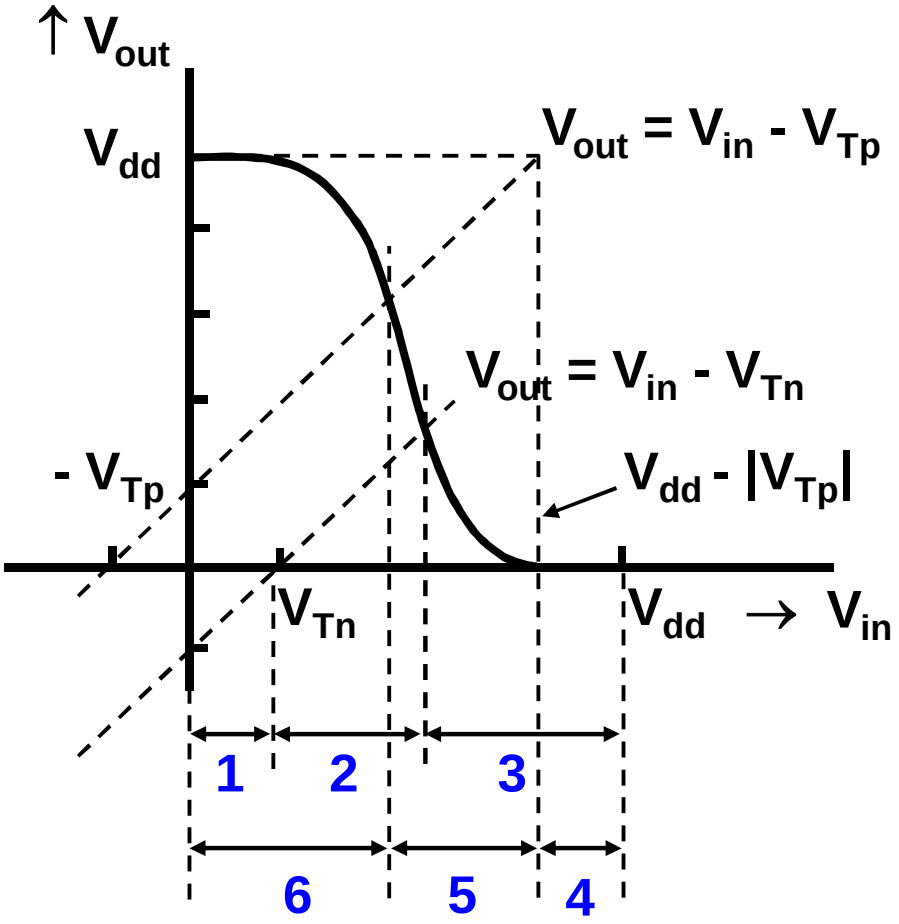
4 $V_{in} > V_{DD} + V_{Tp} \Rightarrow$ **off**

5 $V_{out} < V_{in} - V_{Tp} \Rightarrow$ **saturation**

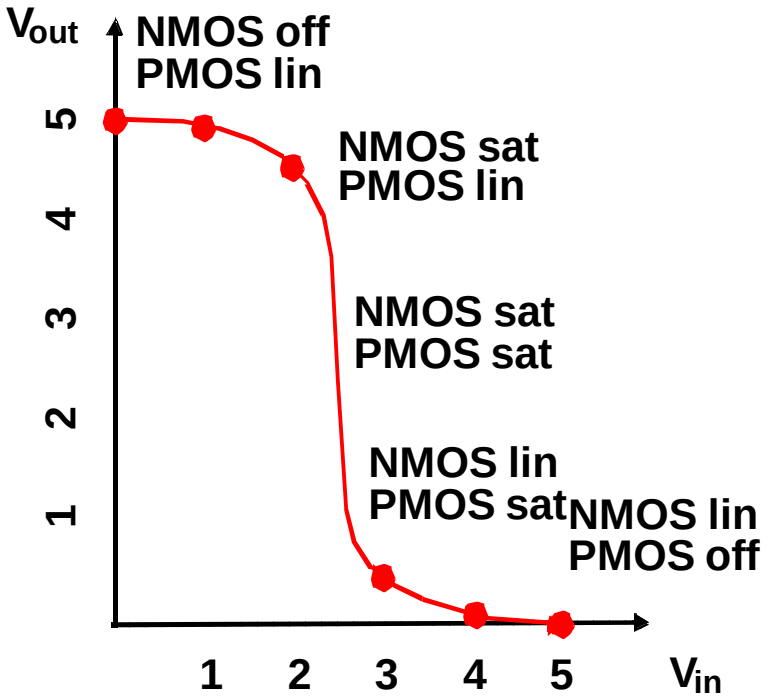
6 $V_{out} > V_{in} - V_{Tp} \Rightarrow$ **resistive**

Exercise: check results for PMOS

Operating Conditions.

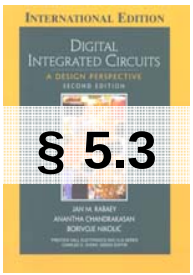


NMOS	1 off
	2 saturation
	3 resistive
PMOS	4 off
	5 saturation
	6 resistive

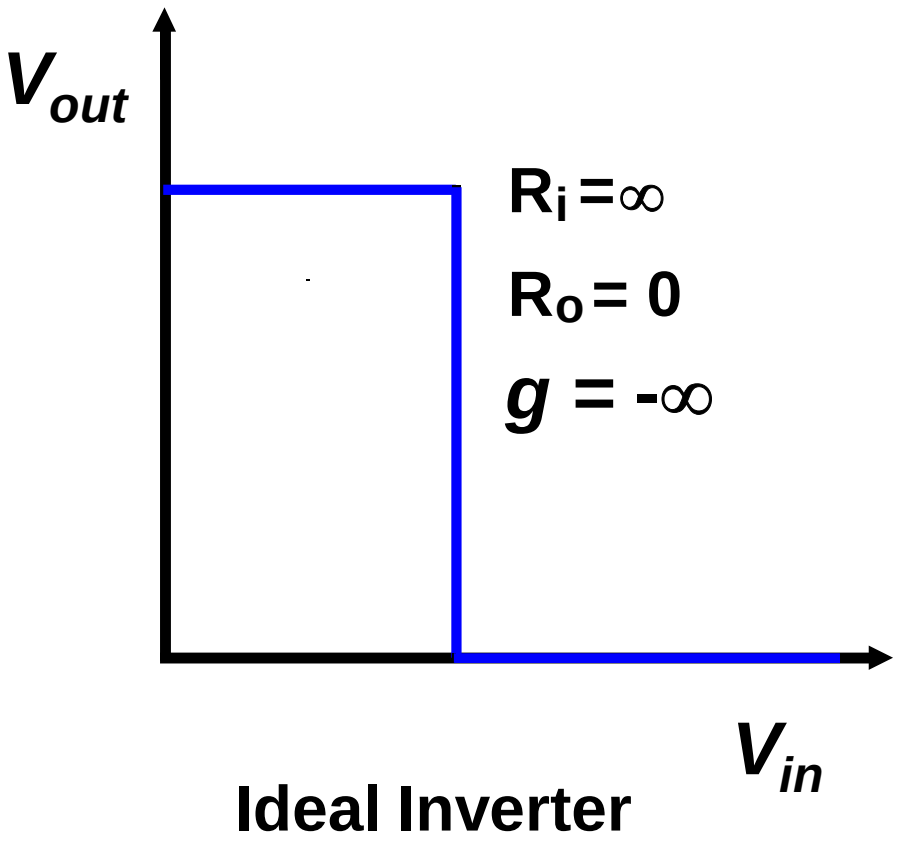


Inverter Static Behavior

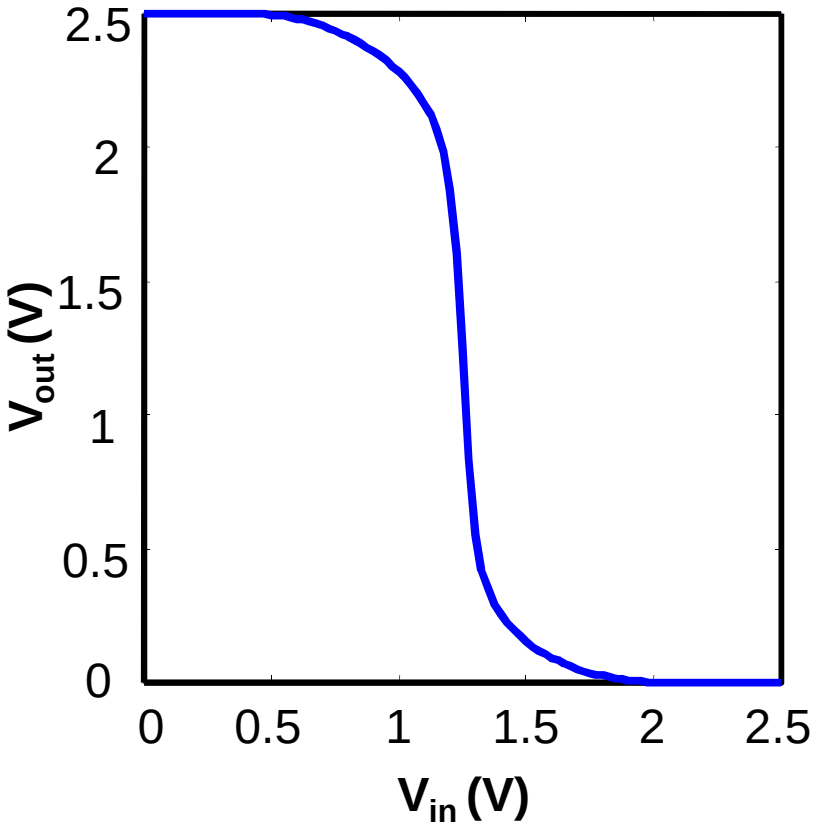
- Regeneration
- Noise margins
- Delay metrics



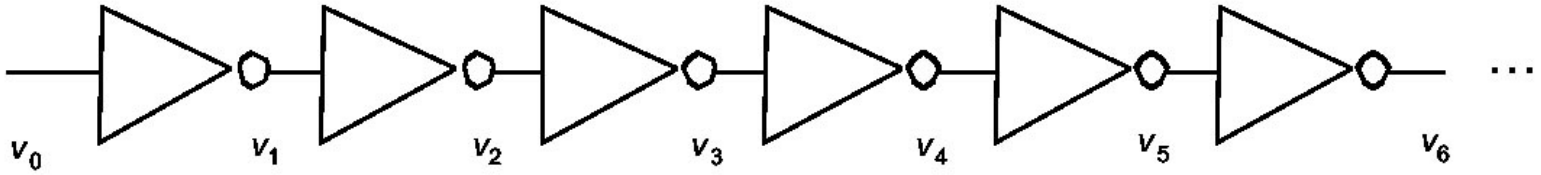
The Realistic Inverter



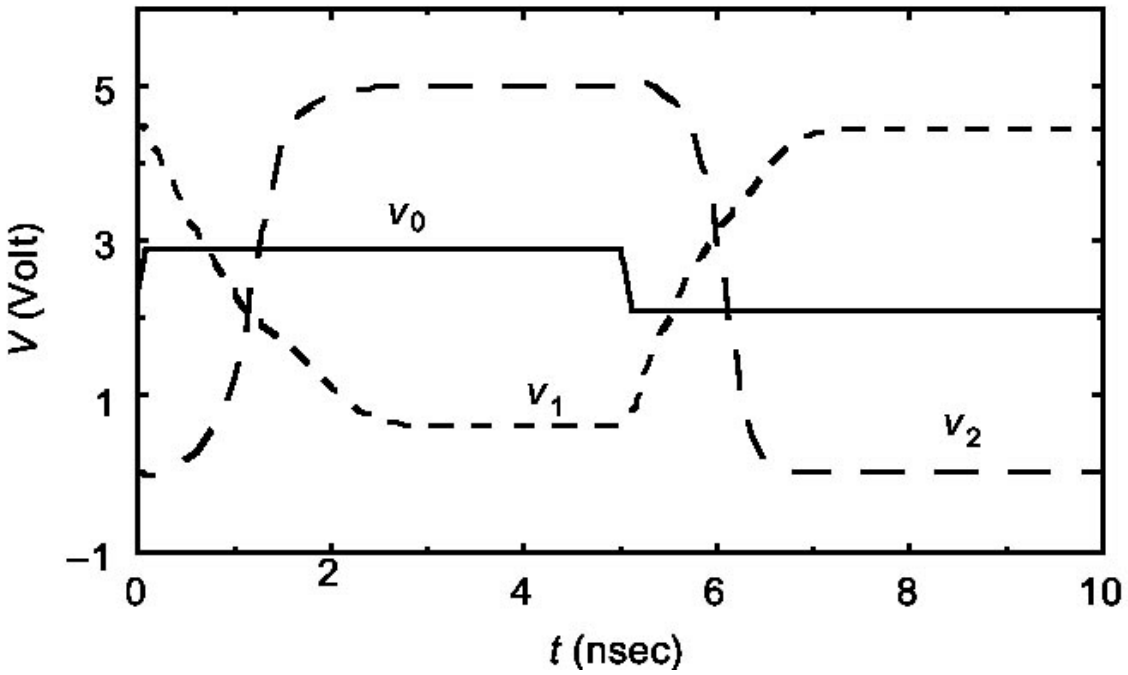
Ideal Inverter



The Regenerative Property

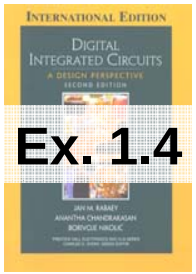


A chain of inverters

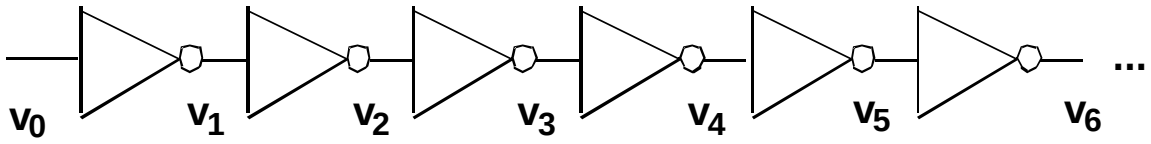


The regenerative property

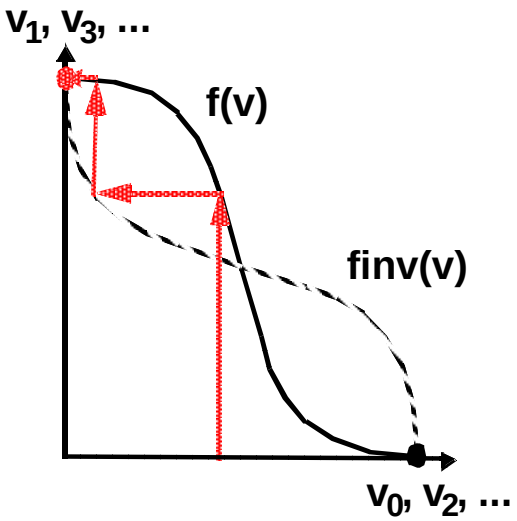
- **Regenerative Property:** ability to regenerate (repair) a weak signal in a chain of gates



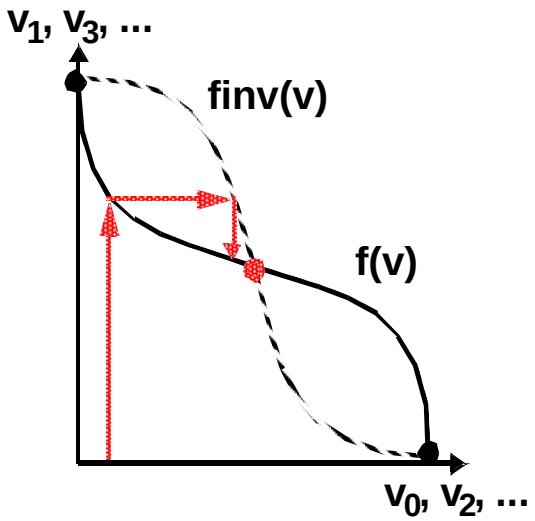
The Regenerative Property (2)



(a) A chain of inverters.

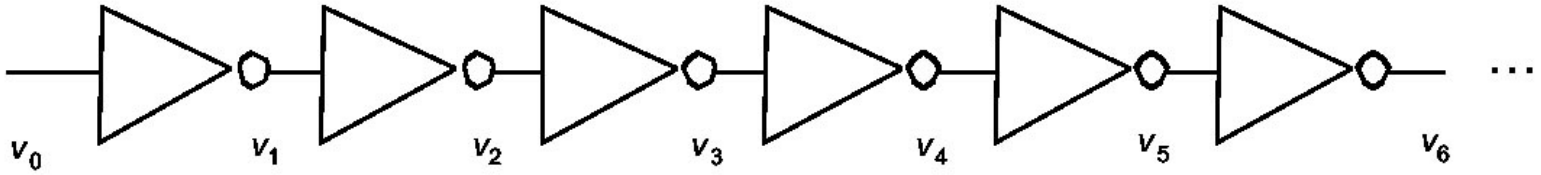


(b) Regenerative gate



(c) Non-regenerative gate

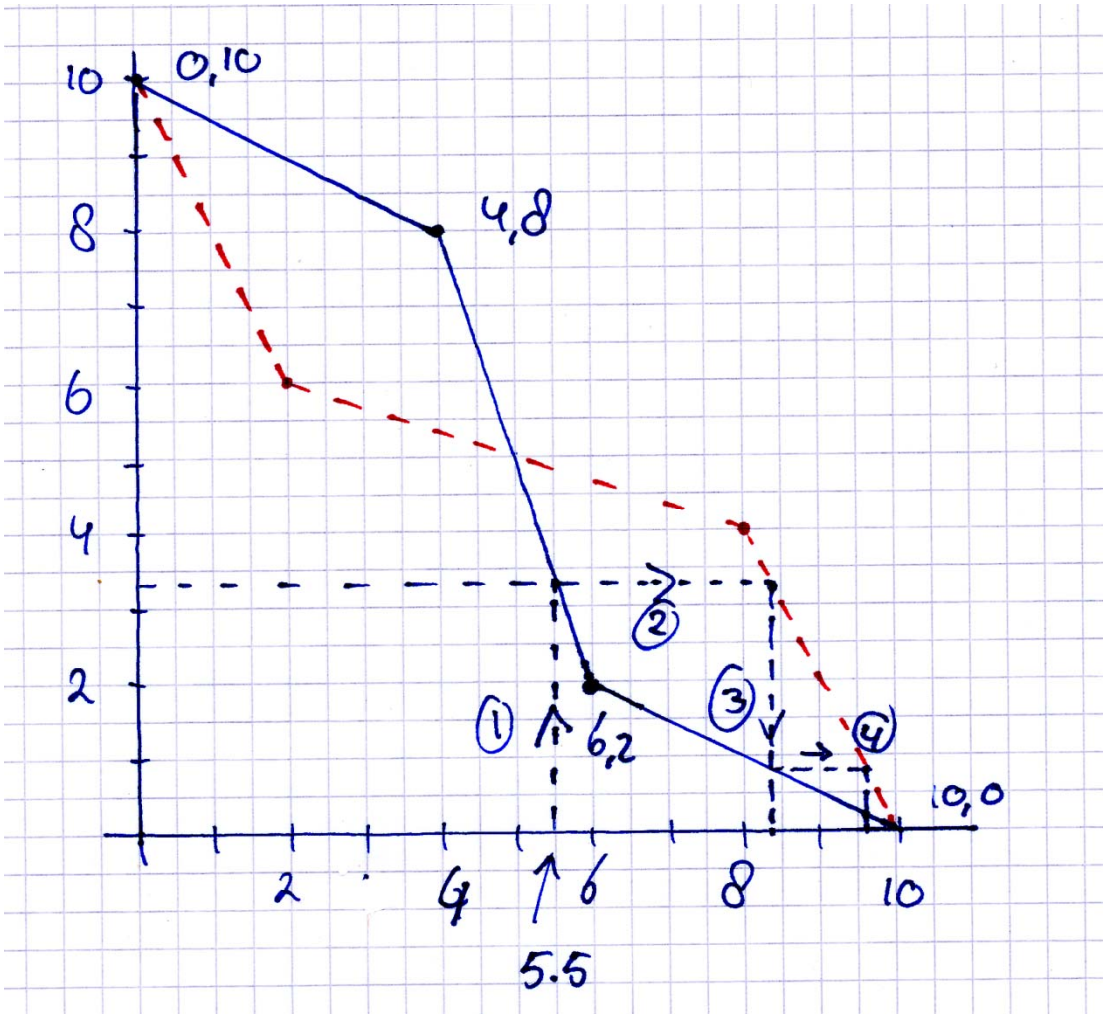
The regenerative Property (3)



Exercise: **what is the output voltage of a chain of 4 inverters with a piece-wise linear VTC passing through (0, 10), (4,8), (6,2) and (10,0) [Volt], as the result of an input voltage of 5.5 [Volt].**

Exercise: **discuss the behavior for an input of 5 [Volt]**

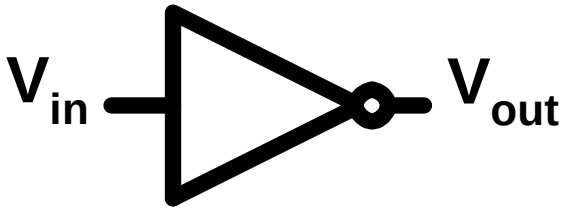
Exercise Answer

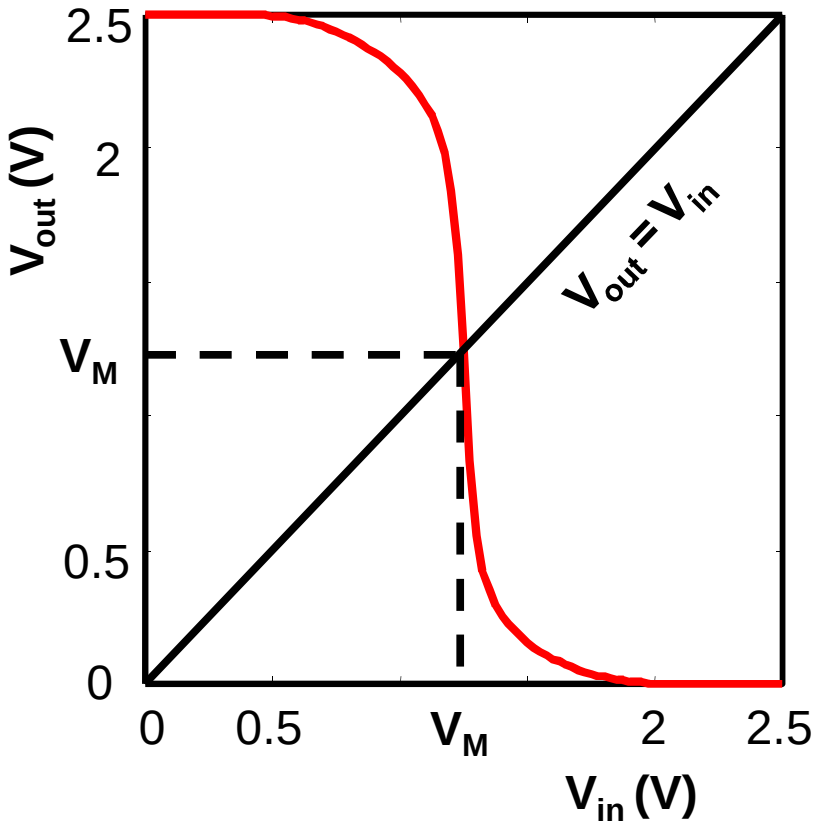


Ongeveer: 5.5 → 3.5 → 8.5 → 0.75 → 9.75

Inverter Switching Treshold

- **Not the device threshold** $V_m = f(R_{onn}, R_{onp})$
- **Point of $V_{in} = V_{out}$**

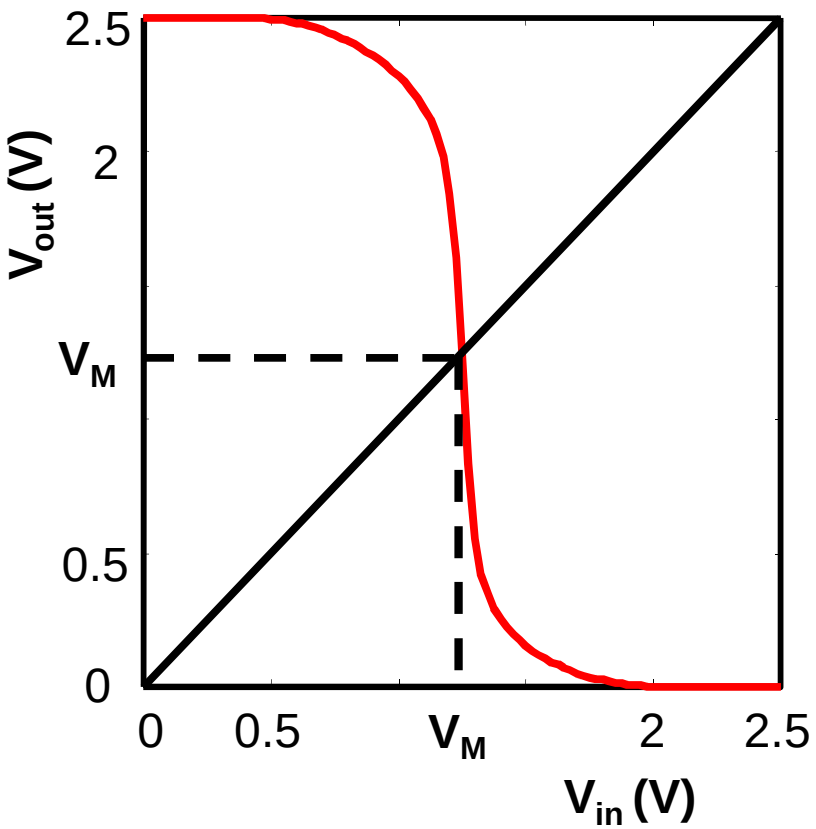




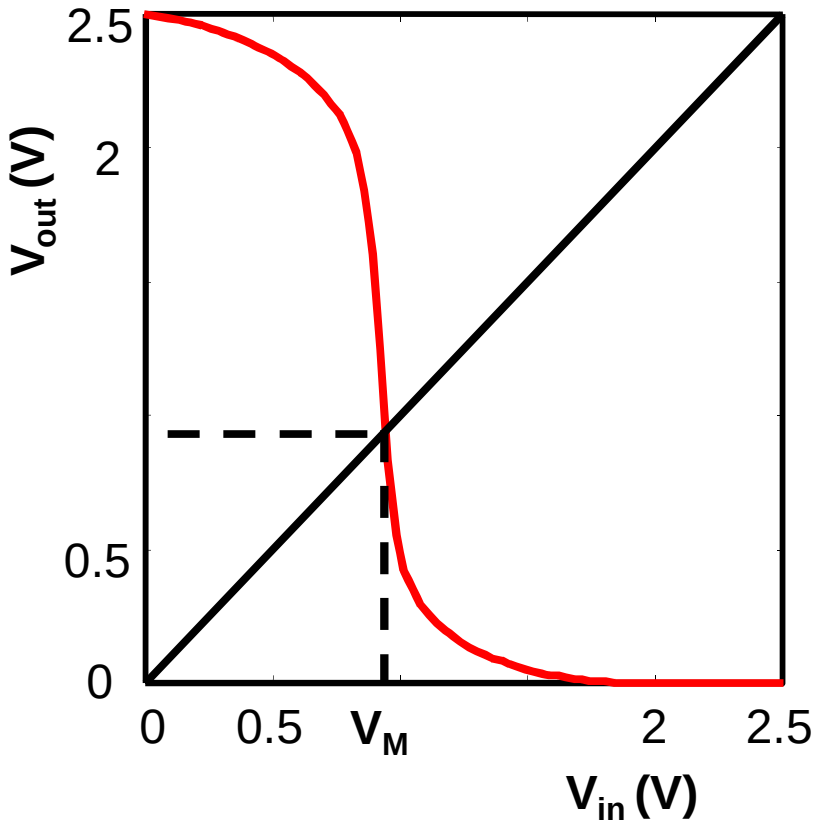
- **Try to set W_n, L_n, W_p, L_p so that VTC is symmetric as this will improve noise margins**

optimize NMOS-PMOS ratio

Inverter Switching Threshold



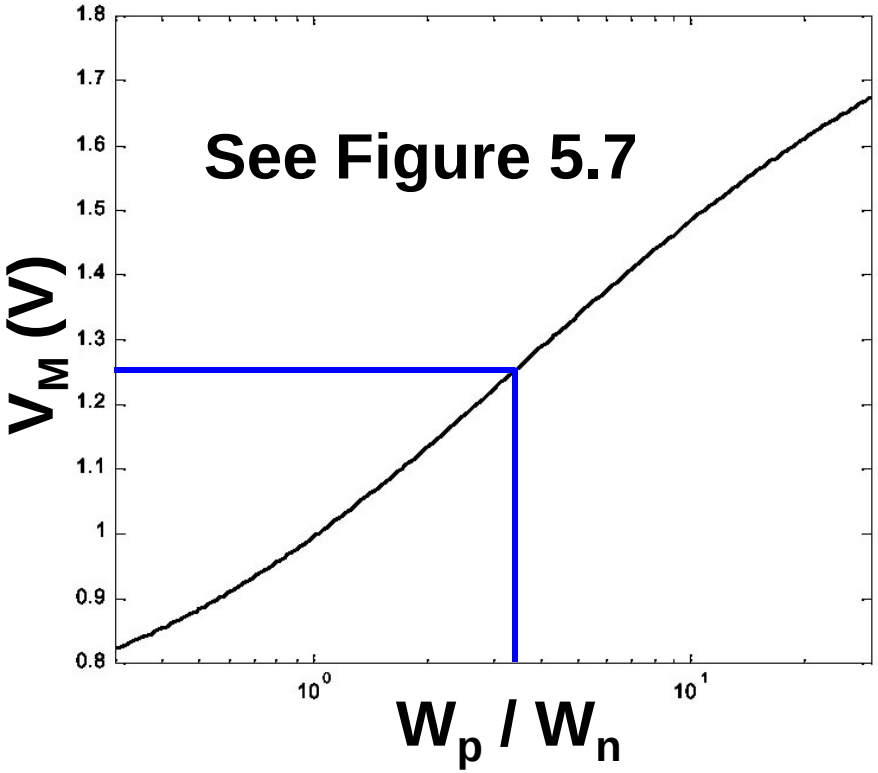
Balanced NMOS and PMOS sizes



Strong NMOS, Weak PMOS

$$V_M = f\,(W_n/W_p)$$

Simulated Inverter Switching Threshold



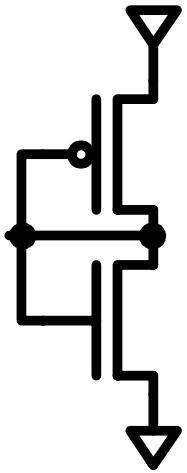
Electrical Design Rule

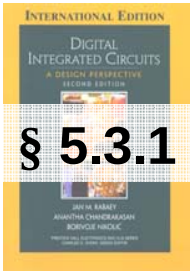
$W_p \approx 2.5\, W_n$

- Assumes $L_p = L_n$
- Should be applied consistently

- Symmetrical VTC $\Rightarrow V_m \approx \frac{1}{2} V_{DD} \Rightarrow W_p/W_n \approx$ [ ]
- In practice: choose somewhat smaller value of W_p/W_n
- Why? [ ]

Inverter Switching Threshold
Analytical Derivation





- V_M is V_{in} such that $V_{in} = V_{out}$
- $V_{DS} = V_{GS} \Leftrightarrow V_{GD} = 0 \Rightarrow$ saturation
  - Assume $V_{DSAT} < V_M - V_T$

    (velocity saturation)
  - Ignore channel length modulation (for simplicity – is it allowed?)
- V_M follows from
  - $I_{DSATn}(V_M) = - I_{DSATp}(V_M)$
- Q: Given desired value of V_M, what is the required W/L ratio?

Inverter Switching Threshold

Analytical Derivation (ctd)

$$I_{DSATn}(V_M) = -\, I_{DSATp}(V_M)$$

$$I_D = kV_{DSAT}\left(V_{GS} - V_T - V_{DSAT}/2\right)$$

$$\Leftrightarrow\ k_n V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right) = -k_p V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)$$

$$\Leftrightarrow\ \frac{k_p}{k_n} = \frac{-V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right)}{V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)}$$

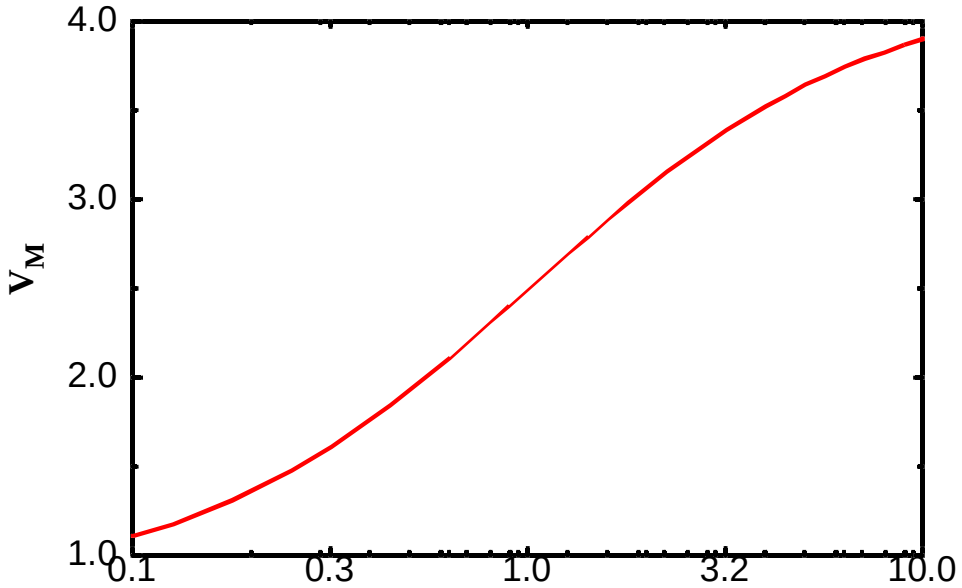
$$k = \frac{W}{L}k'$$

$$\Rightarrow\ \frac{(W/L)_p}{(W/L)_n} = \left|\frac{k'_n V_{DSAT_n}\left(V_M - V_{Tn} - V_{DSATn}/2\right)}{k'_p V_{DSAT_P}\left(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2\right)}\right|$$

- **See Example 5.1:**
- **$(W/L)_p = 3.5\,(W/L)_n$ for typical conditions and $V_M = ½\ V_{DD}$**
- **Usually: $L_n = L_p$**

Inverter Switching Threshold w/o Velocity Saturation.

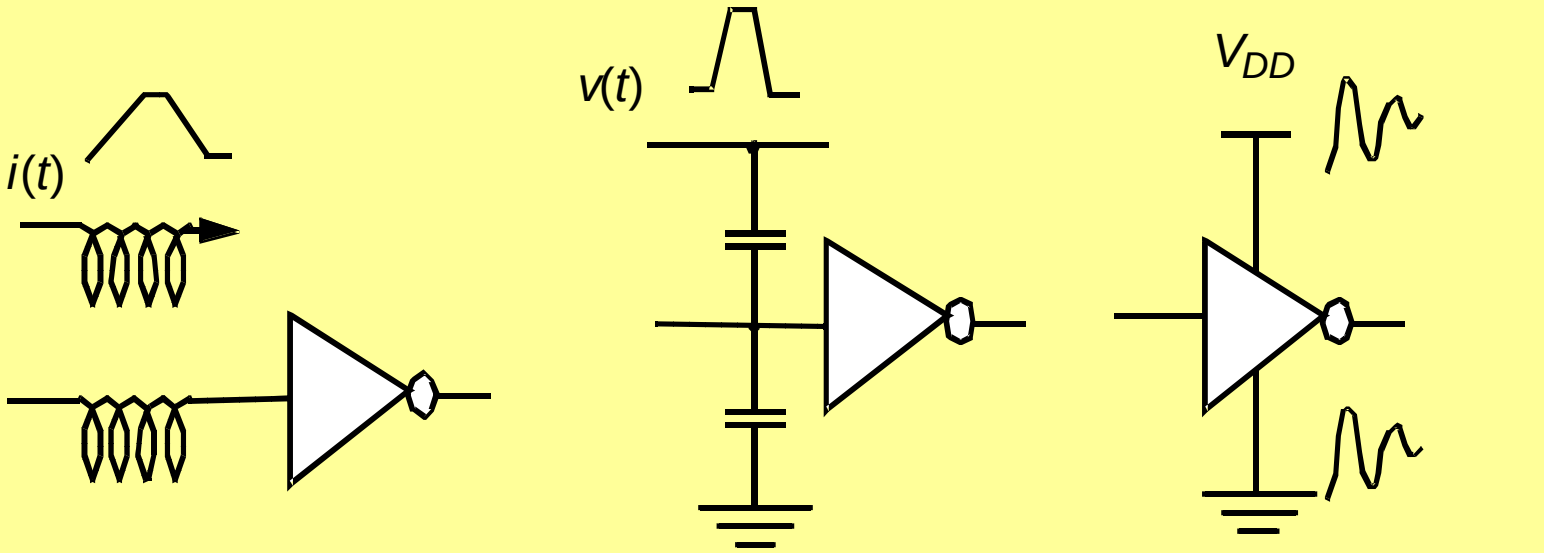
- **Long channel approximation**
- **Applicable with low V_{DD}**



Exercise (Problem 5.1): derive V_M for long-channel approximation as shown below

$$V_M = \frac{r(V_{DD} - V_{Tp} + V_{Tn})}{1 + r} \quad with \quad r = \sqrt{\frac{-k_p}{k_n}}$$

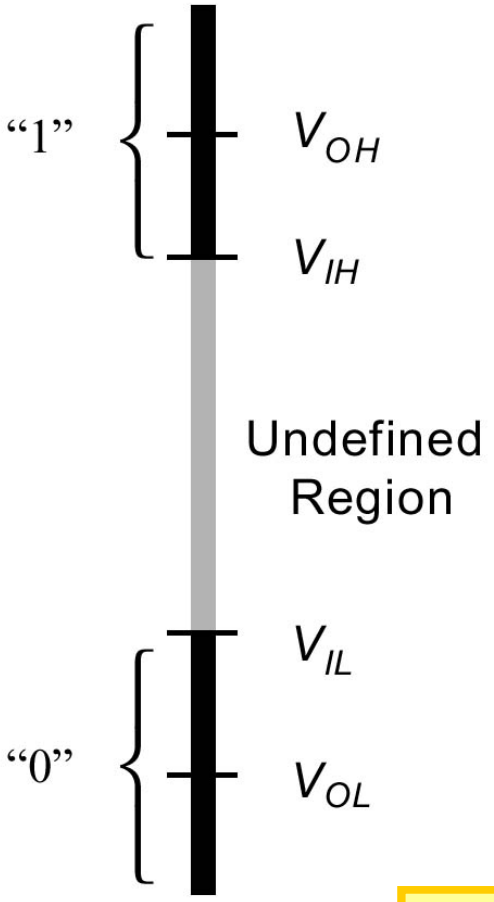
Noise in Digital Integrated Circuits

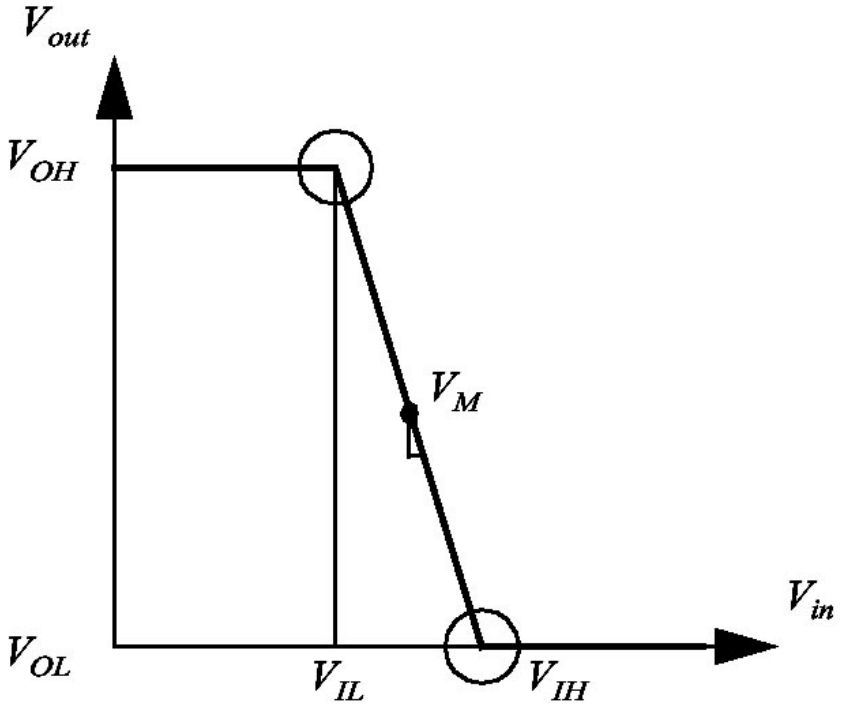


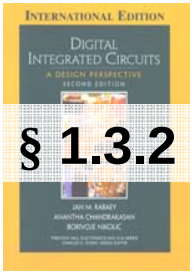
(a) Inductive coupling (b) Capacitive coupling (c) Power and ground noise

- **Study behavior of static CMOS Gates with noisy signals**

Noise Margins

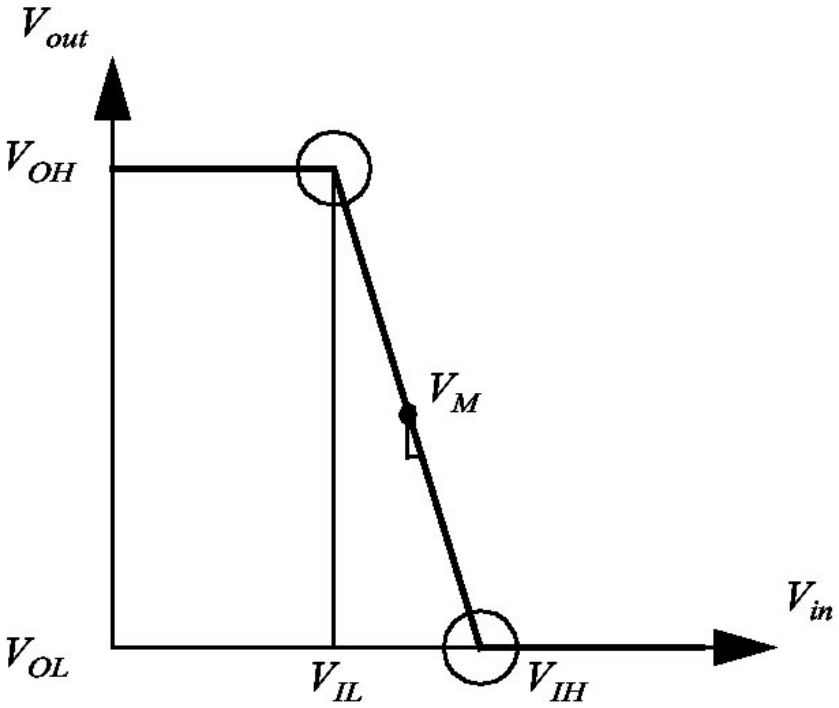


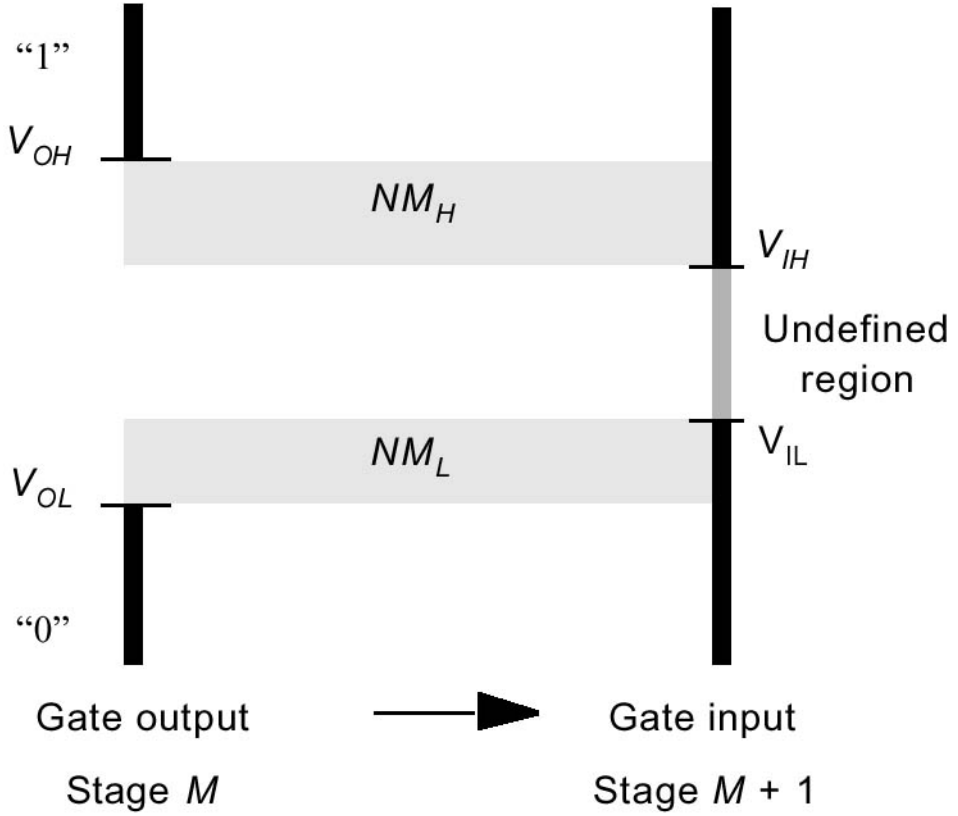




- **V_{OL} = Output Low Voltage**
- **V_{IL} = Input Low Voltage**
- **V_{OH}, V_{IH} = …**

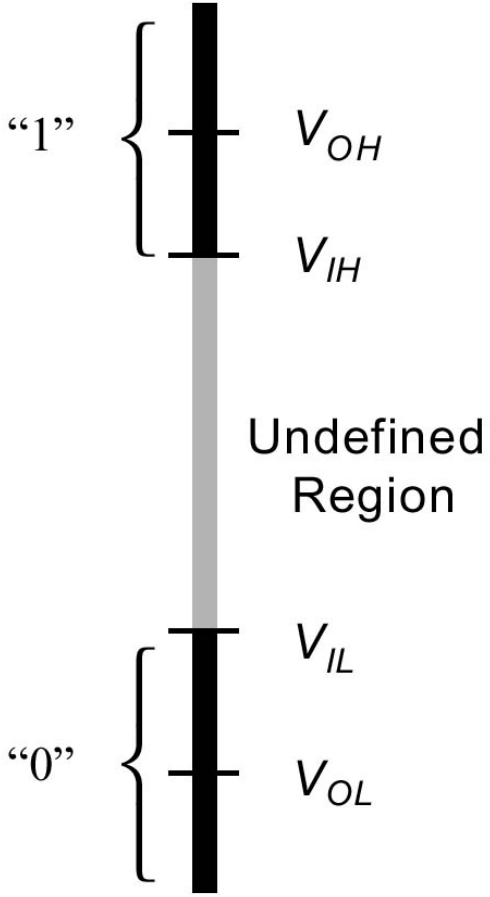
Noise Margins

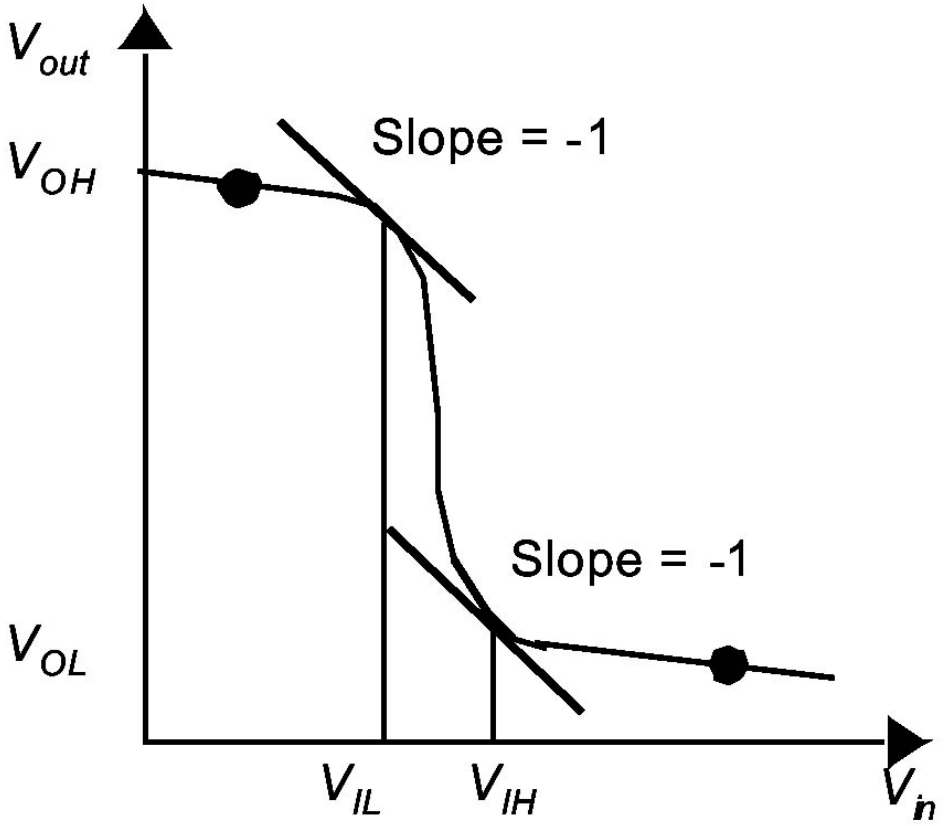




- $NM_H = V_{OH} - V_{IH}$ = High Noise Margin
- $NM_L = V_{IL} - V_{OL}$ = Low Noise Margin

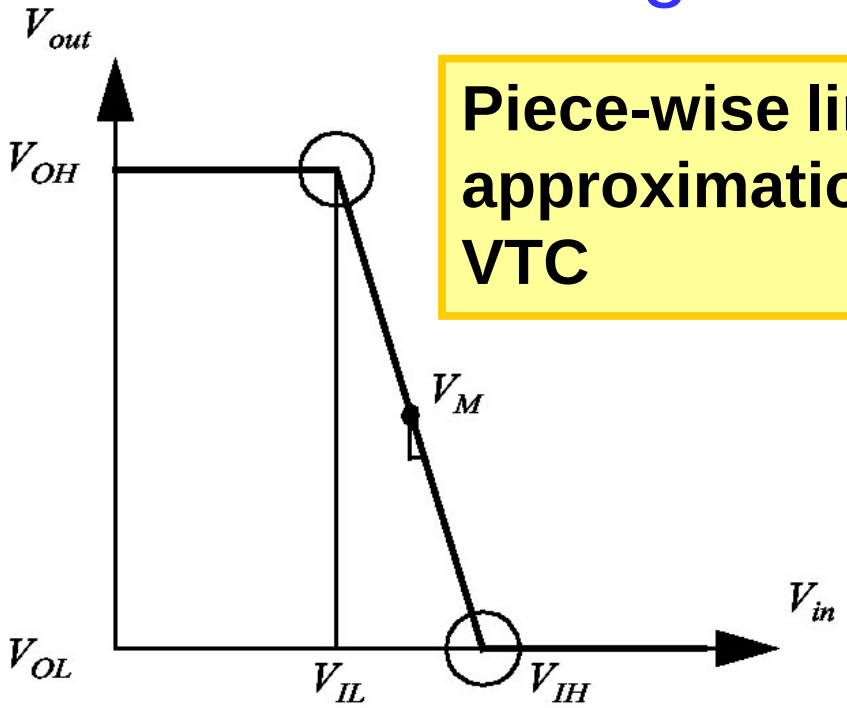
Noise Margin for Realistic Gates





Exercise: explain significance of slope = -1 for noise margin

Noise Margin Calculation



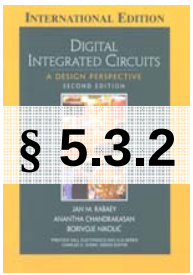
Piece-wise linear approximation of VTC

g = gain factor (slope of VTC)

We know how to compute V_M

Next: how to compute g

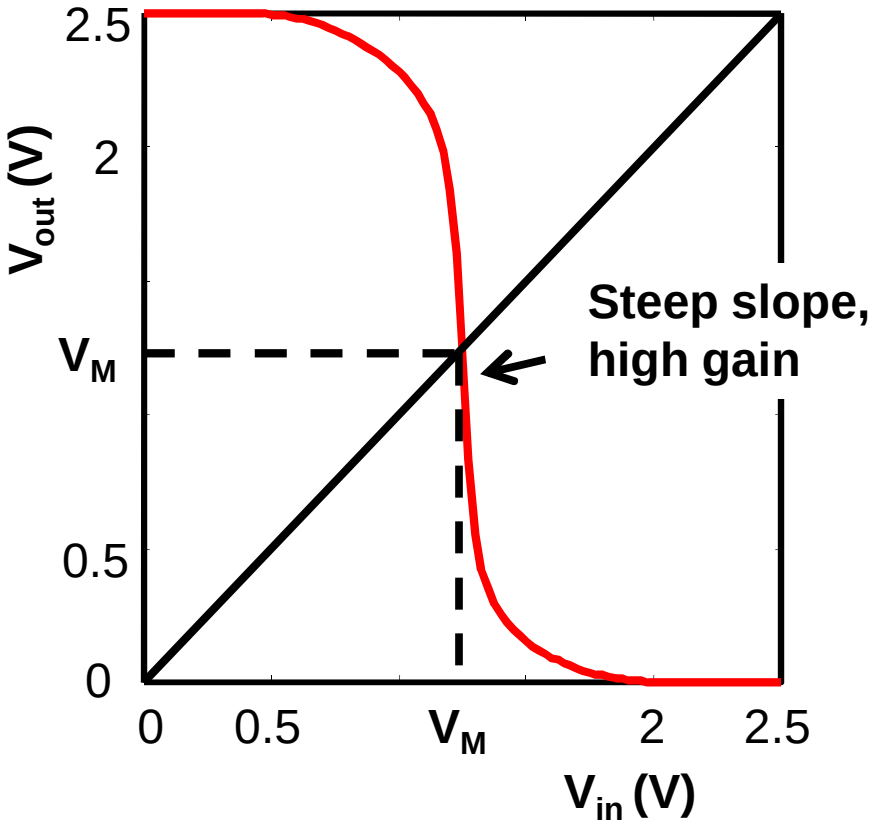
$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

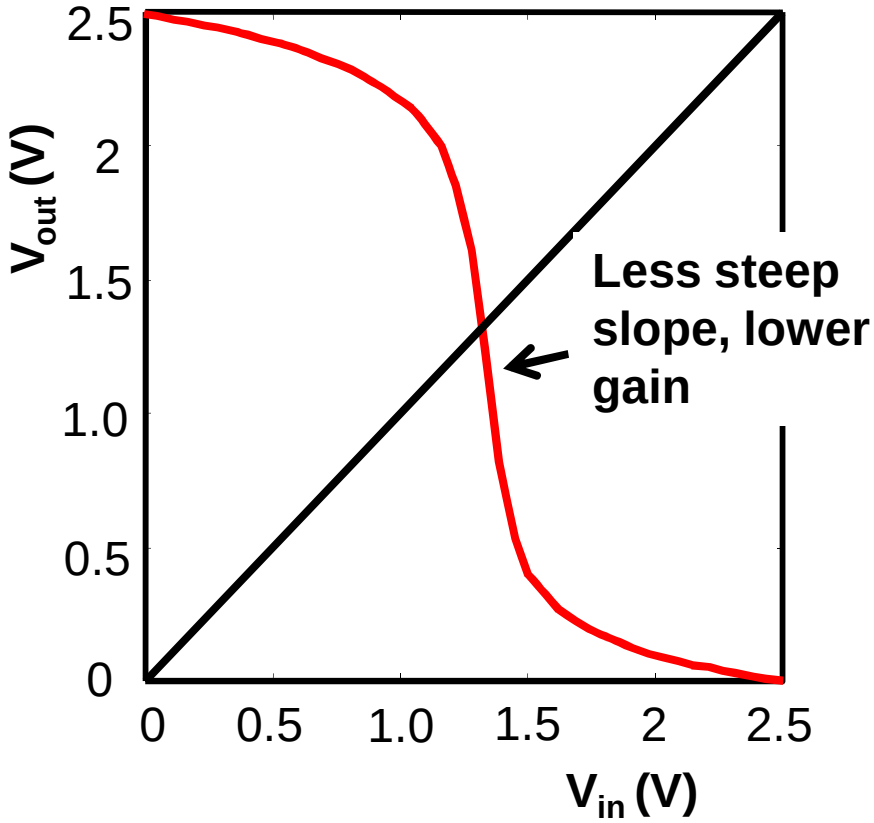


$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

Different Gain



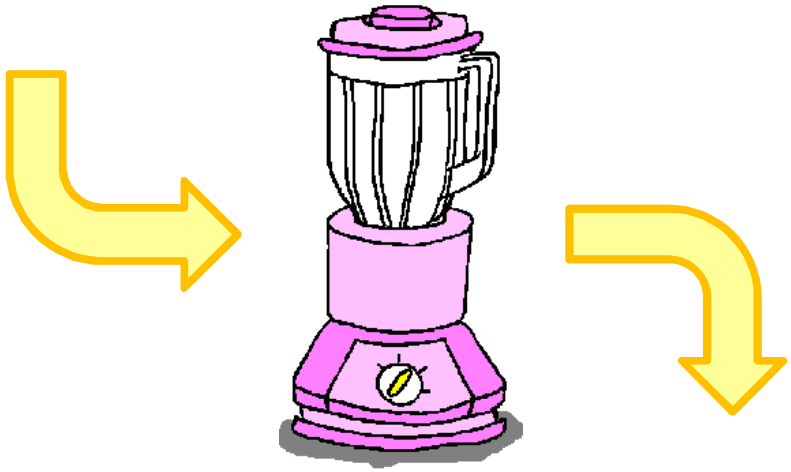


Noise Margin Calculation (2)

- **Approximate *g* as the slope in V_{out} vs. V_{in} at $V_{in} = V_M$**

$$k_n V_{DSAT_n}\left(V_{in} - V_{Tn} - V_{DSATn}/2\right)\left(1+\lambda_n V_{out}\right)+$$

$$k_p V_{DSAT_P}\left(V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2\right)\left(1+\lambda_p V_{out} - \lambda_p V_{DD}\right)=0$$



$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M} \approx \frac{1+r}{\left(V_M - V_T - V_{DSATp}/2\right)\left(\lambda_n - \lambda_p\right)} \qquad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

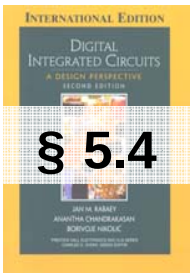
Noise Margin Calculation (3).

$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M} \approx \frac{1+r}{\left(V_M - V_T - V_{DSATp}/2\right)\left(\lambda_n - \lambda_p\right)} \qquad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

- Mostly determined by technology
- See example 5.2
- **Exercise:** verify calculation
- **Exercise:** explain why we add channel length modulation to the I_D expressions (we did not do this to determine V_M)

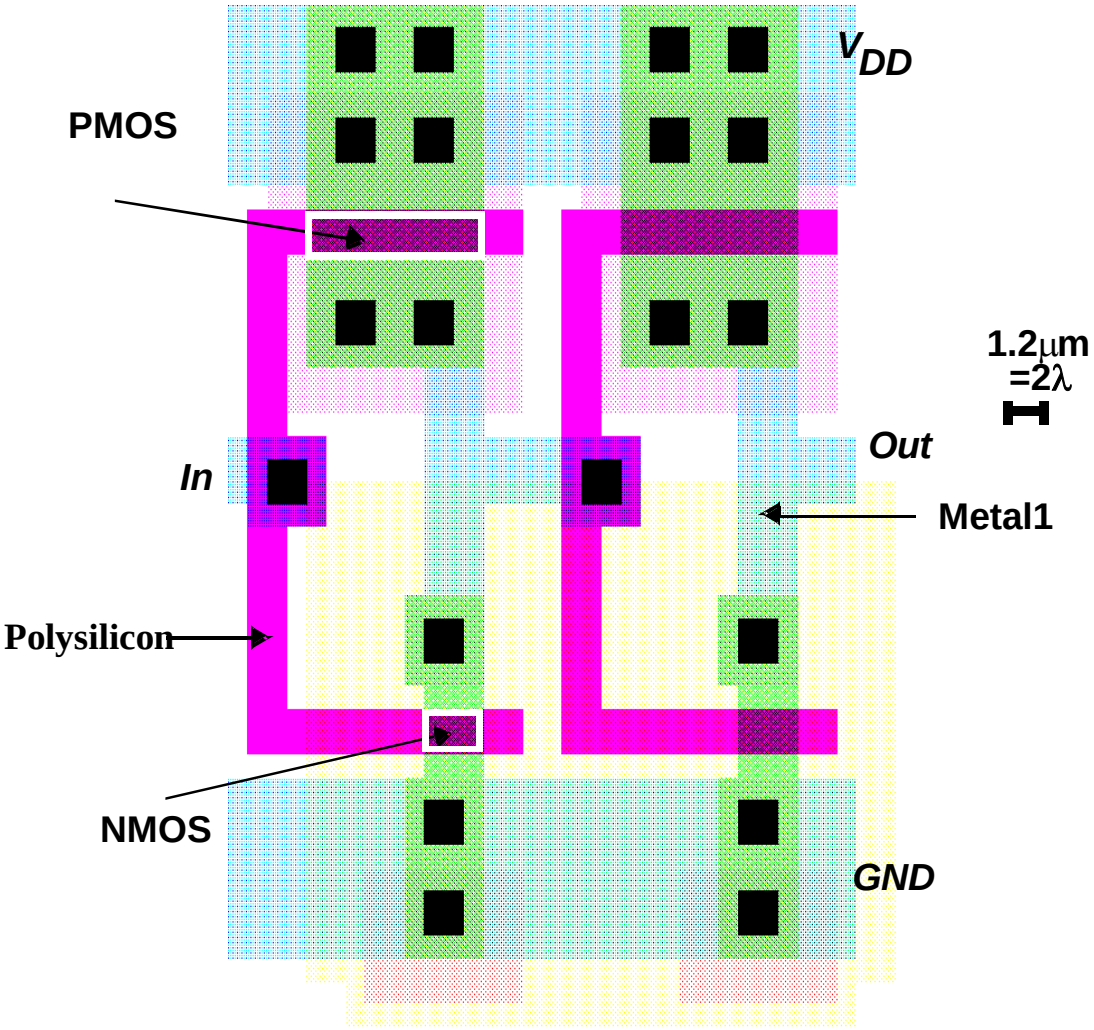
Dynamic Behavior (Performance)

- Capacitances
- Delay



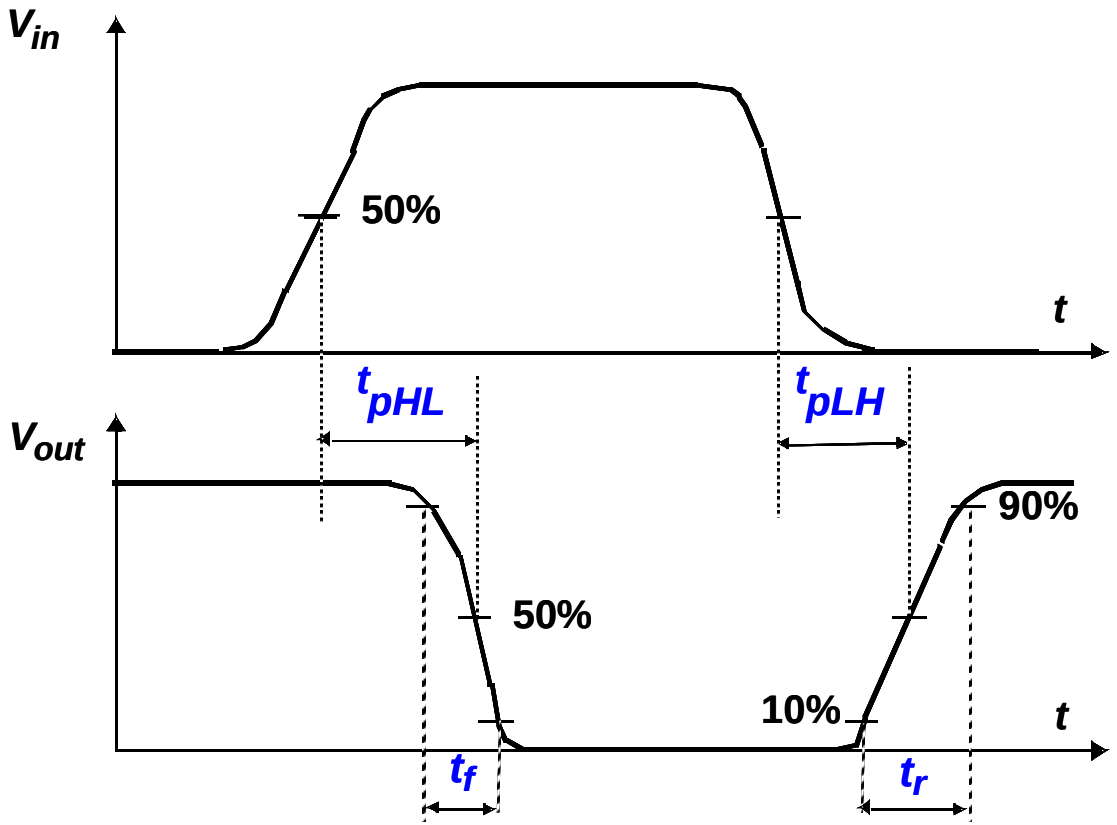
- But: we take much simpler model for capacitances compared to book.
- See the syllabus.
- § 5.4.1 of book is only illustration.

CMOS Inverters

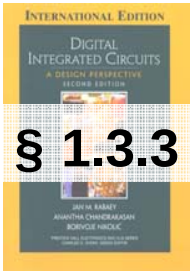


- What causes the **delay**?
- What is R_{on} ?
- Where are the **capacitances?**
- Which capacitances determine T_p?

Delay Definitions



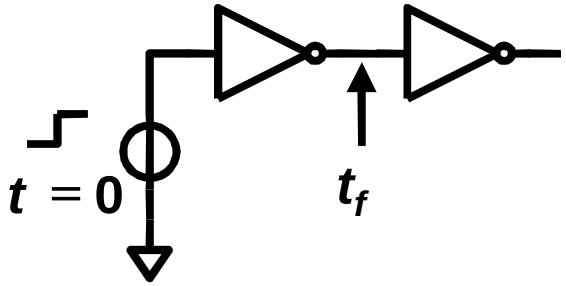
$$t_p = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right)$$



t_p : property of gate

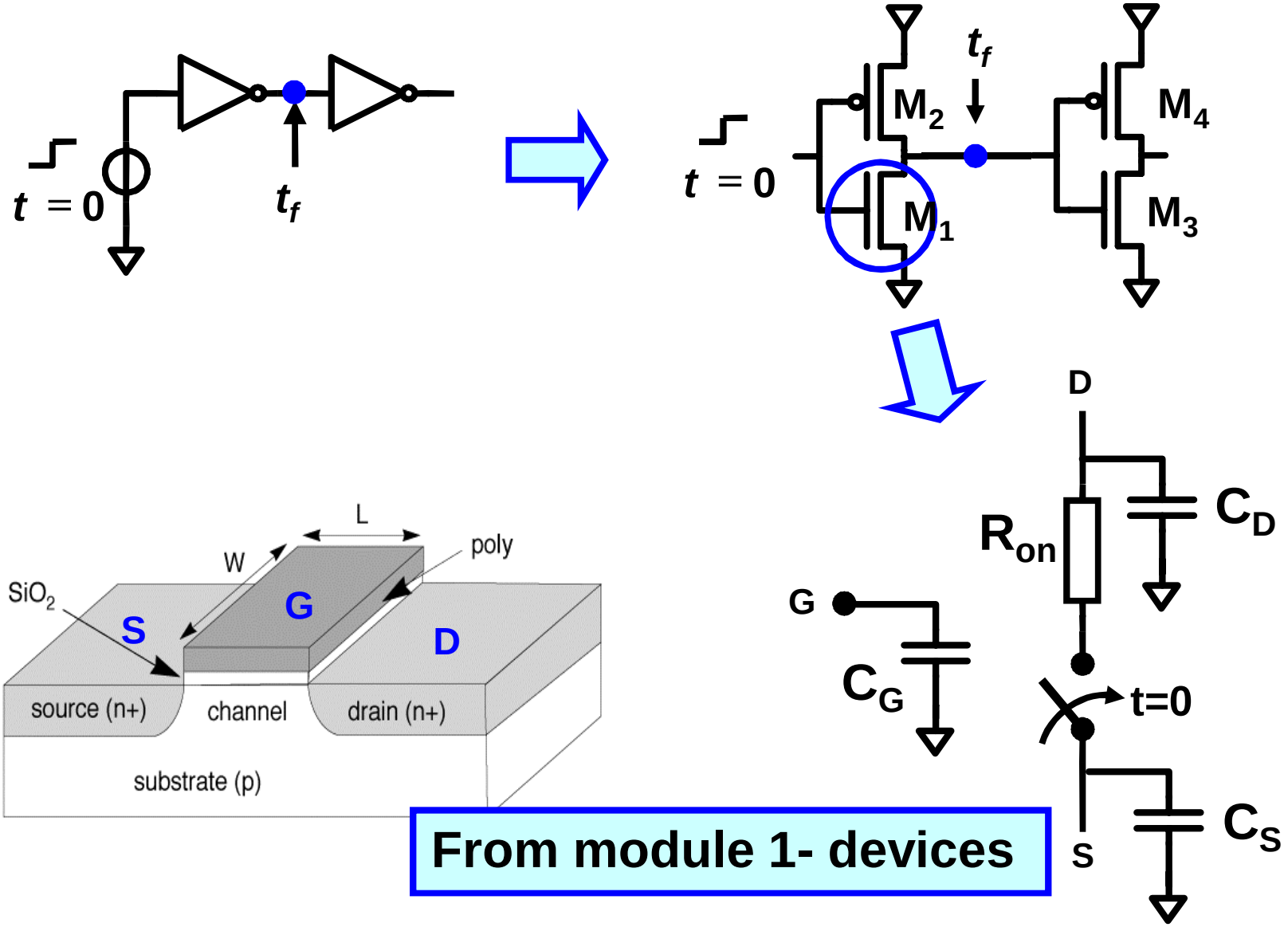
t_r, t_f : property of signal

CMOS Inverter Rise/Fall Delay



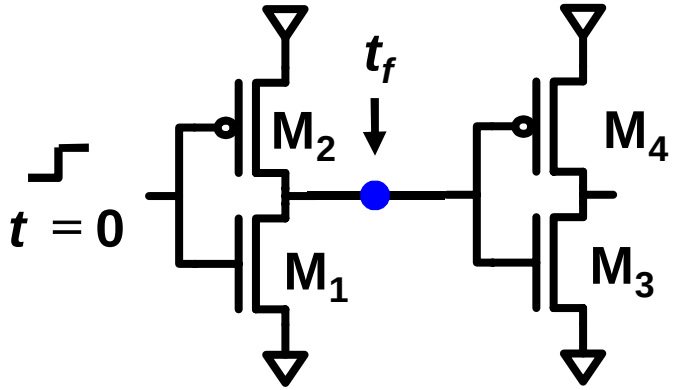
- **Goal: determine t_f, t_r and t_p**
- **First: compute relevant capacitances**
- **Second: determine equivalent R_{on}**
- **Third: compute RC delay (τ) and scale result**
- **Assume: ideal source, step input**

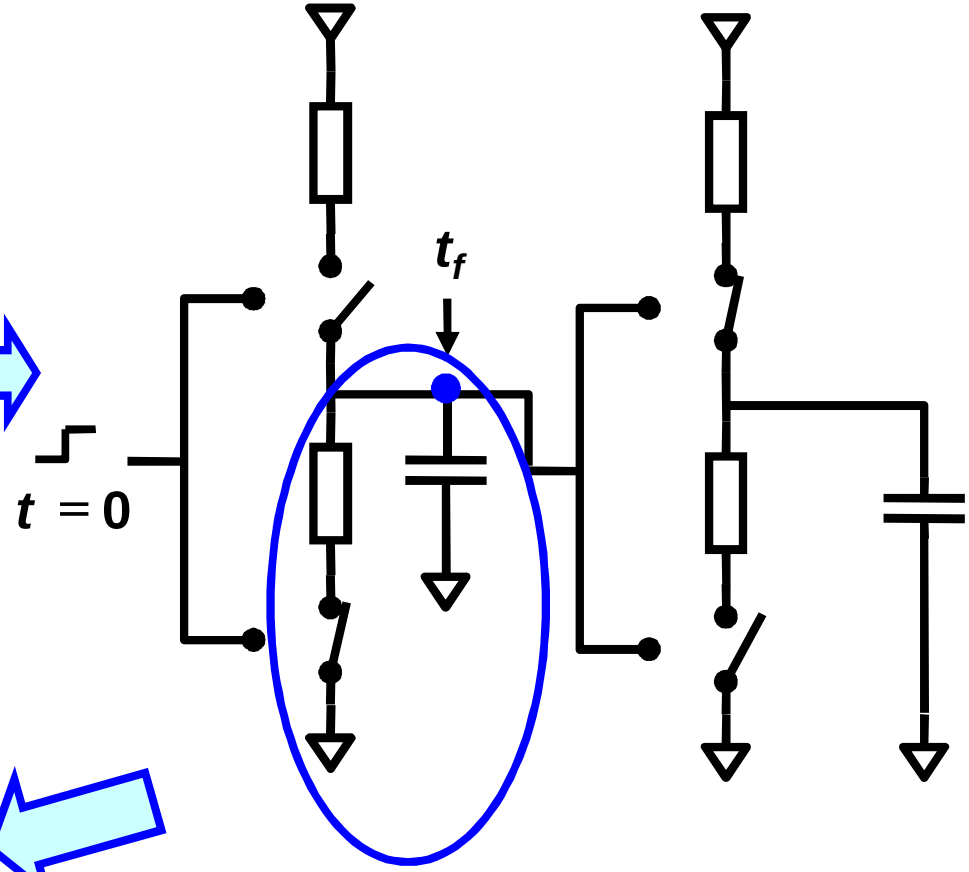
Modeling

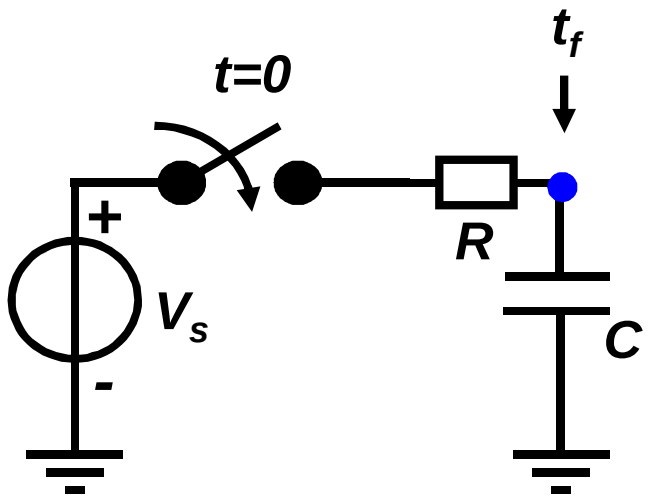


From module 1- devices

Modeling (2)







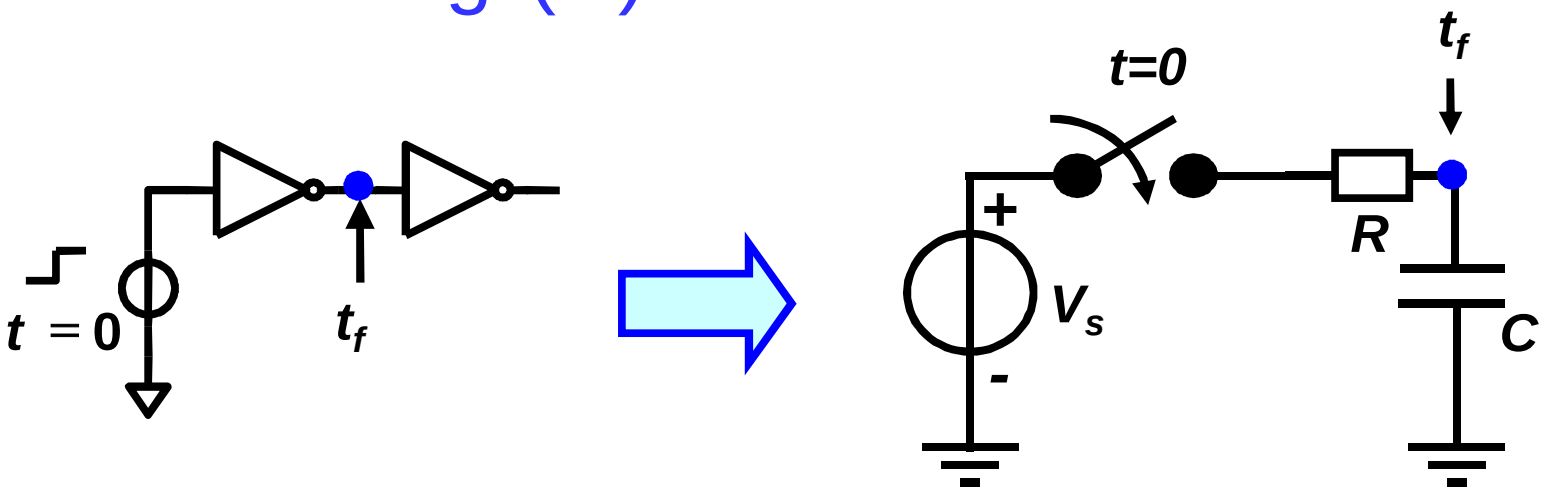
$R = R_{on1}$

$C = C_{D1} + C_{D2} + C_{G3} + C_{G4}$

$V_S = 0$

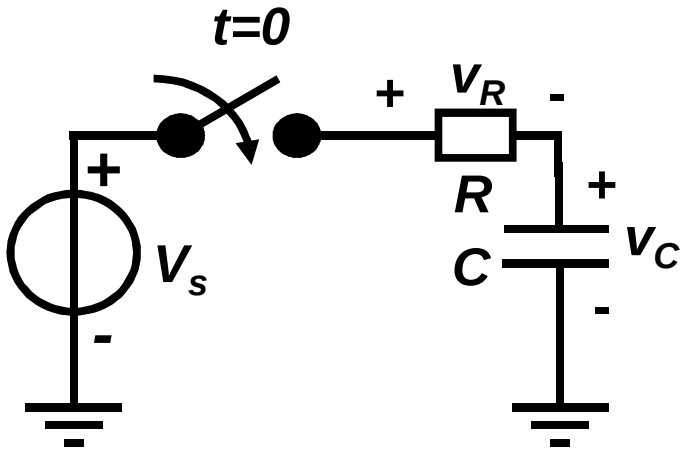
Frequently, we only include C_{Gi}

Modeling (3)

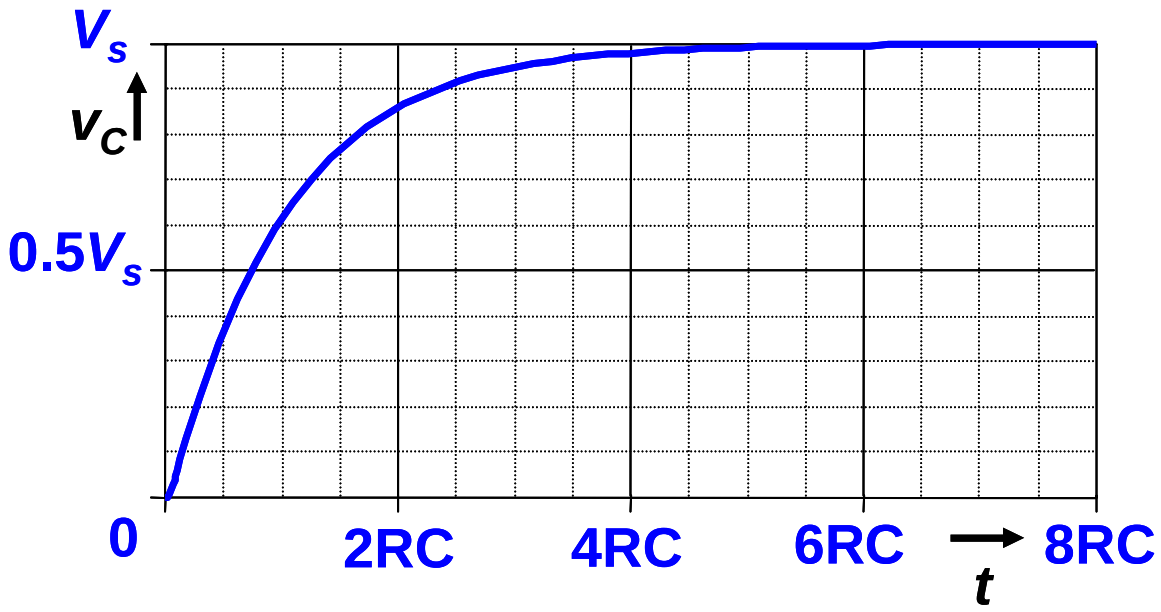


- Delay can be modeled using RC circuit
  - First order simplified model
- R is (linearized) on-resistance of active transistor
- C is sum of (linearized) C's that are switched
  - Typically, C_G of driven gate, C_D of driving gate
  - Plus relevant interconnect C
  - Might need to include interconnect R in model
- V_s is final voltage of delay node (initial voltage determined by previous state)

RC Delay Review (1)



$$v_C(t) = v_C(\infty) + (v_C(t_0) - v_C(\infty))e^{-(t-t_0)/\tau}$$



$$RC\frac{dv_c}{dt} = V_s - v_c$$

$$v_c = V_s(1 - e^{-\frac{t}{RC}})$$

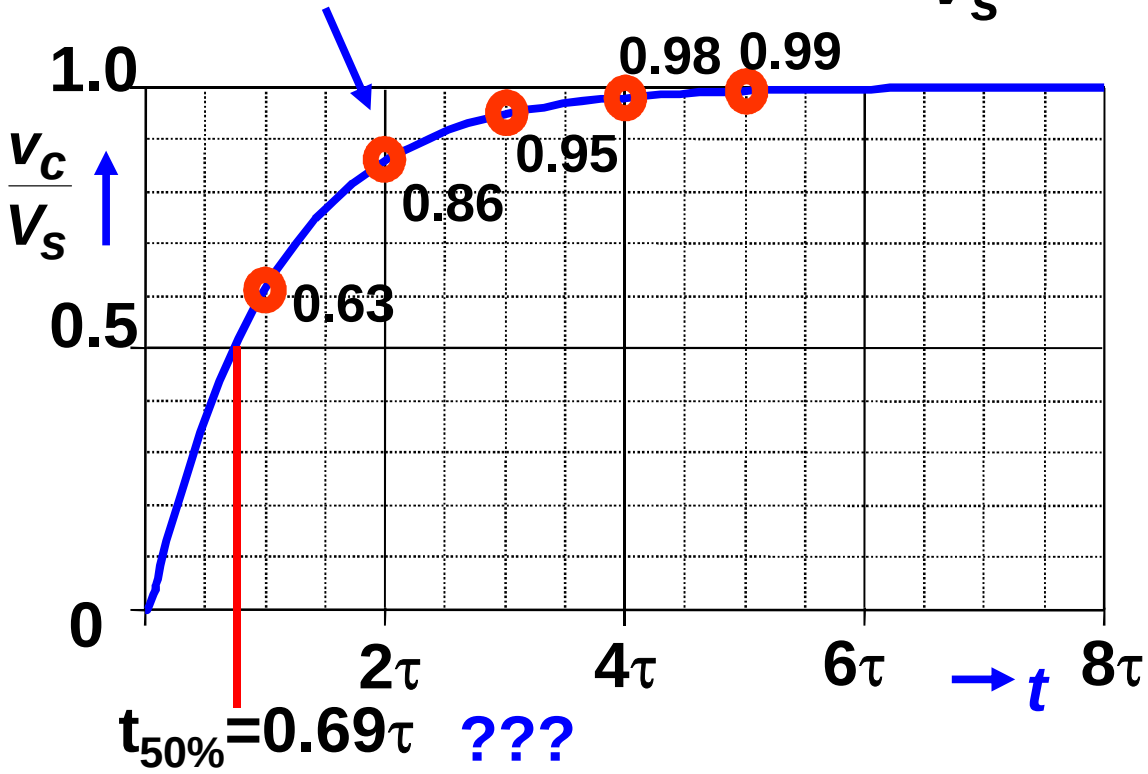
RC Delay Review (2)

- **Response can be normalized with respect to $\tau = RC$ and $V_S = v_C(t = \infty)$**

$$v_C = V_S(1 - e^{-\frac{t}{RC}})$$

$$\frac{v_C}{V_S} = (1 - e^{-t/\tau})$$

Example: $(1 - e^{-2}) = 0.86$



Each τ-step gives 63% of remaining swing

swing	time
0–50%	0.69τ
0–63%	1.0τ
10%–90%	2.2τ
0–90%	2.3τ

$$\frac{v_c}{V_s} = (1 - e^{-t/\tau})$$

$$\Downarrow$$

$$0.5 = (1 - e^{-t_{50\%}/\tau})$$

$$\Downarrow$$

$$0.5 = e^{-t_{50\%}/\tau}$$

$$\Downarrow$$

$$2 = e^{t_{50\%}/\tau}$$

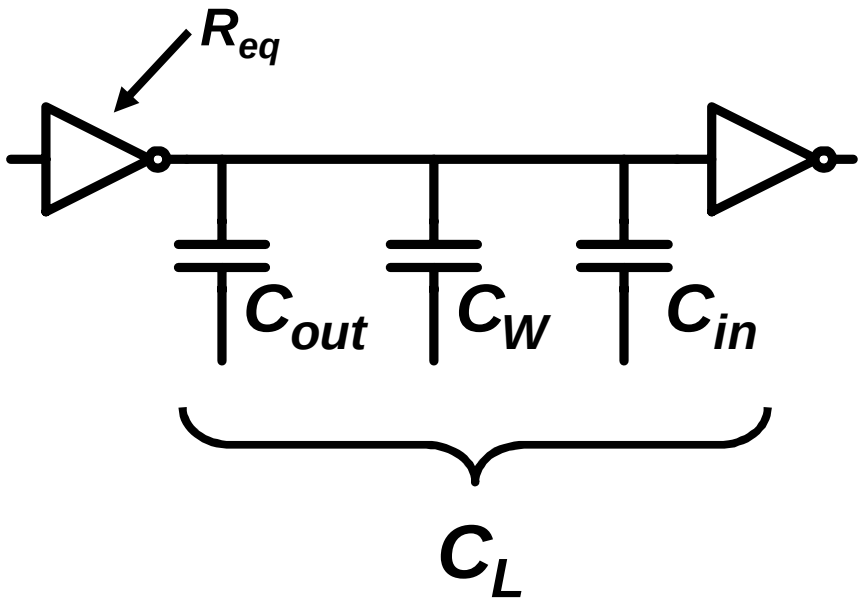
$$\Downarrow$$

$$\ln(2) = 0.69 = t_{50\%}/\tau$$

$$\Downarrow$$

$$t_{50\%} = 0.69\tau$$

Inverter Propagation Delay Summary.

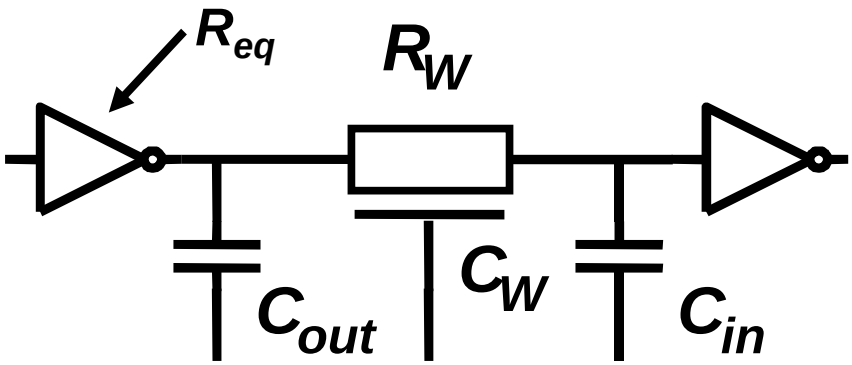


$$t_{pHL} = 0.69 R_{eqn} C_L$$

$$t_{pLH} = 0.69 R_{eqp} C_L$$

$$t_p = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right)$$ **Propagation time**

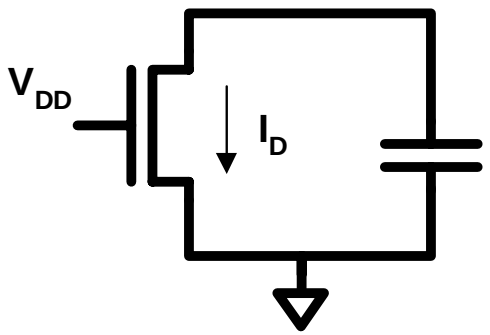
Propagation Delay w. Wire Resistance



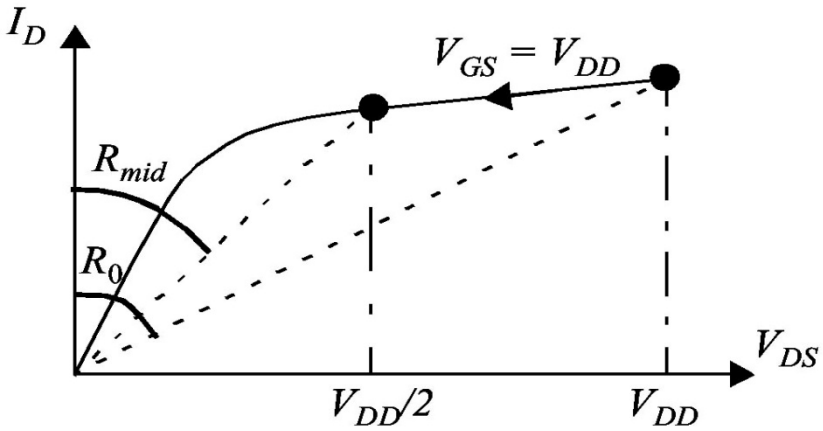
$$t_{PHL} = 0.69R_{eqn}(C_{out} + 0.5C_W)$$
$$+ 0.69(R_{eqn} + R_W)(0.5C_W + C_{in})$$

- **See module 3, interconnect**

Equivalent R_{on} (R_{eq})



(a) Schematic



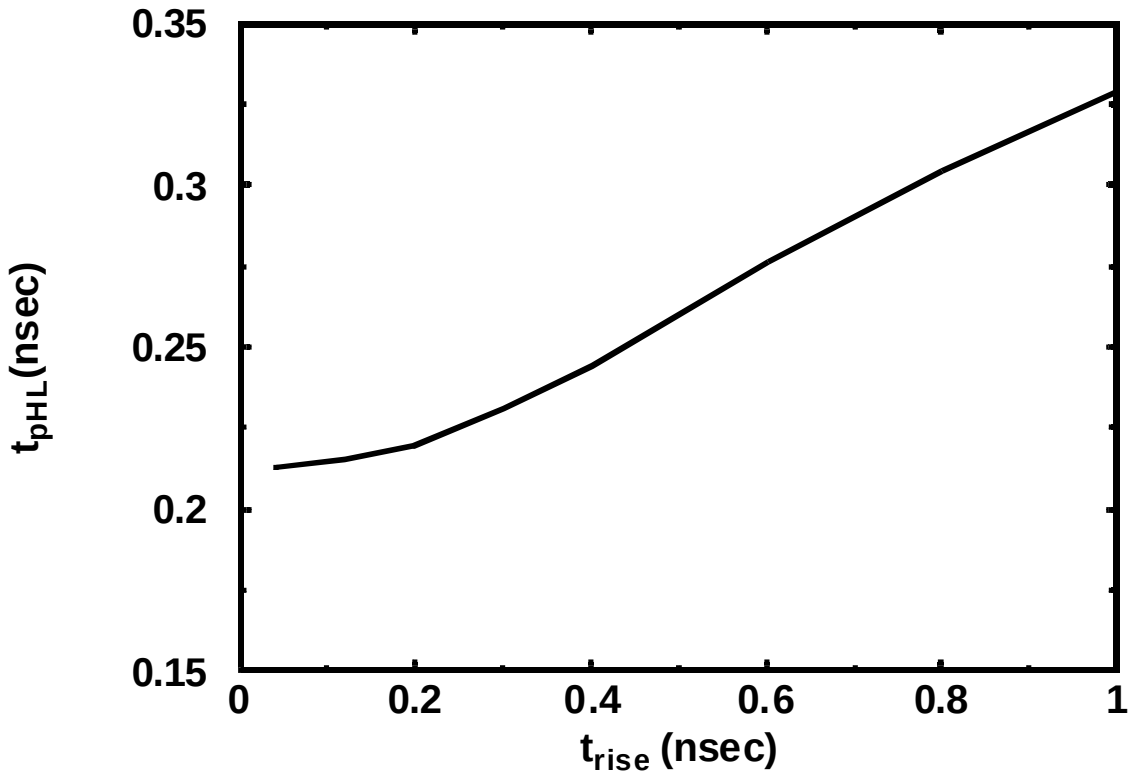
(b) trajectory traversed on ID-VDS curve.

$$R_{eq} = \frac{1}{2}\left[\frac{V_{DD}}{I_{DSAT}\left(1+\lambda V_{DD}\right)} + \frac{V_{DD}/2}{I_{DSAT}\left(1+\lambda V_{DD}/2\right)}\right]$$

$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

See 3-devices, example 3.8

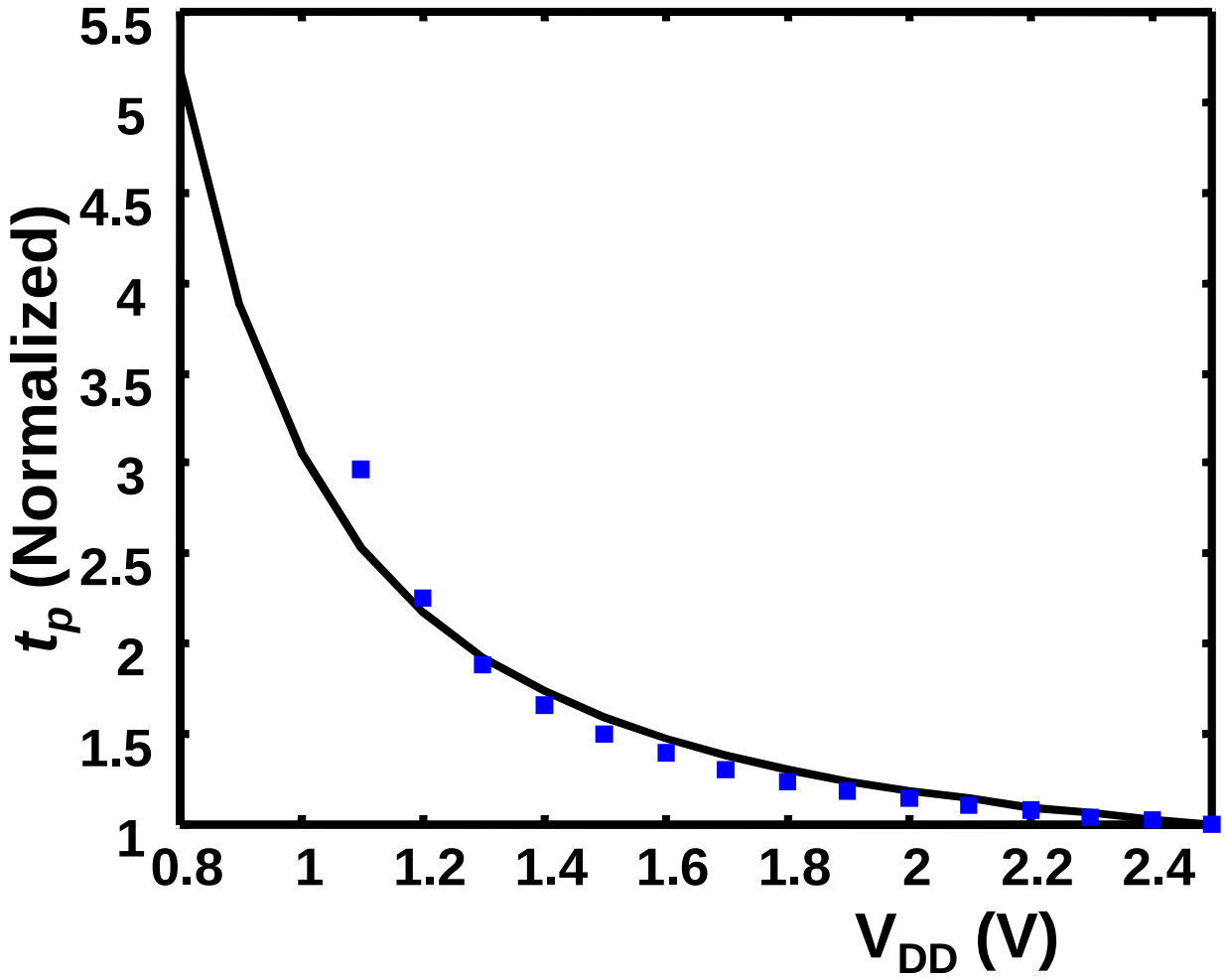
Impact of Rise Time on Delay

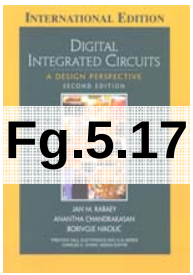


$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Empirical from the first edition of book

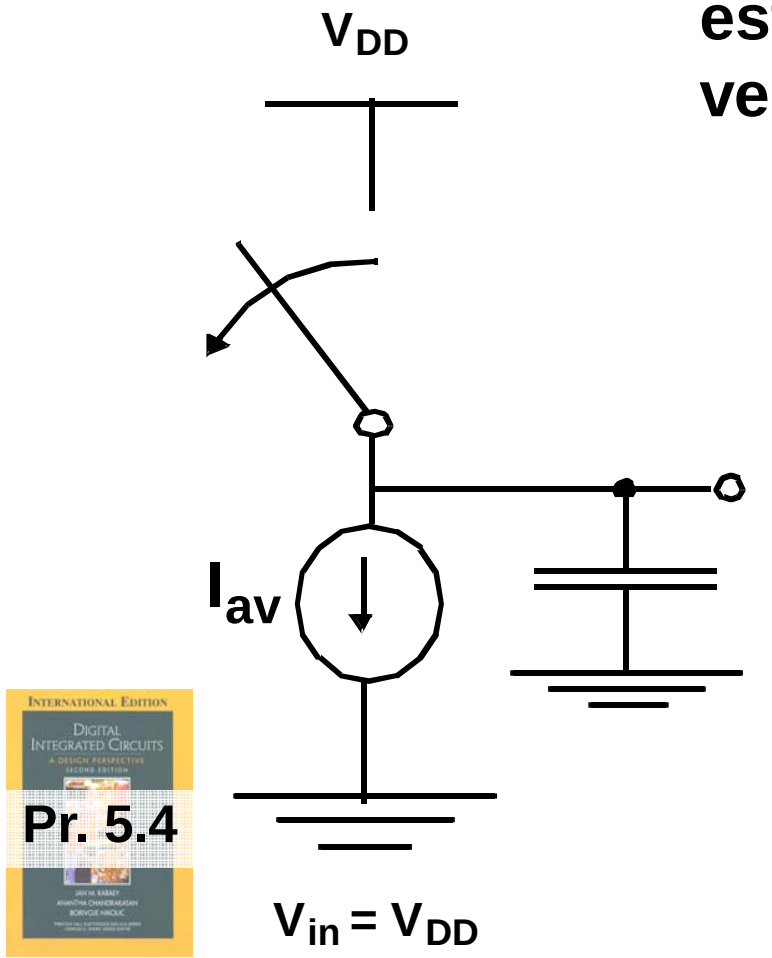
Delay as a function of V_{DD}





Fg.5.17

CMOS Inverter Propagation Delay



Alternative current-based estimate for T_p, assuming velocity saturation

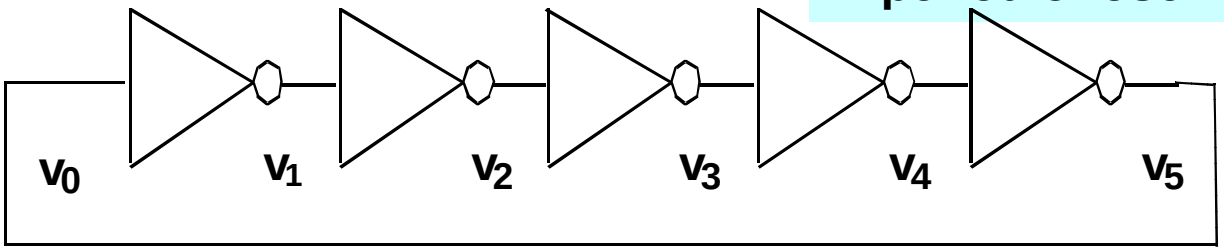
$$T_{pHL} = \frac{C_L \dfrac{V_{swing}}{2}}{I_{av}} \approx \frac{C_L V_{DD}}{2 I_{DSAT}\left(1 + \frac{3}{4}\lambda V_{DD}\right)}$$

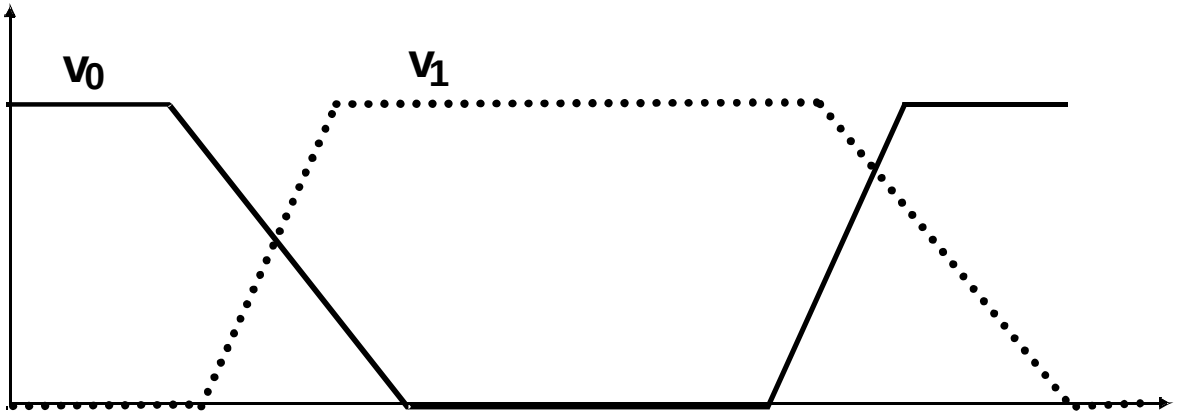
Exercise (Problem 5.4): Derive the expression above

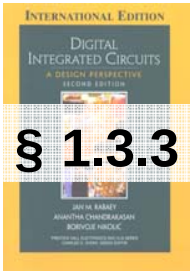
Ring Oscillator

Frequently used to obtain T_p by measurement (or simulation)

N: number of inverters
T_p: propagation delay
T: period of oscillation



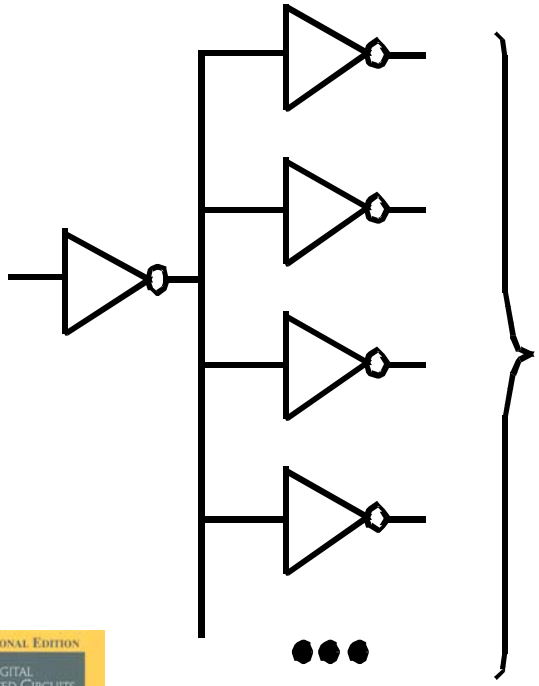




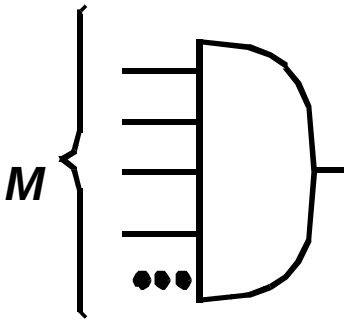
$$T = 2 \times T_p \times N \quad \Leftrightarrow \quad T_p = T/2N$$

Exercise: explain the factor 2 in the expression above

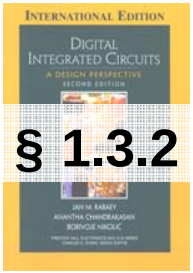
Fan-in and Fan-out.



(a) Fan-out *N*



(b) Fan-in *M*



Power

- **Dynamic Power**
- **Static Power**
- **Metrics**

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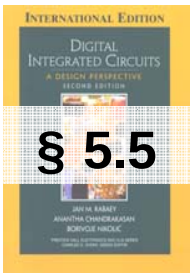
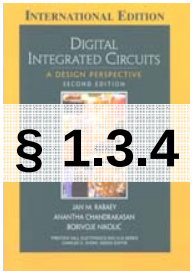


24 hours audio playback time

CMOS Power Dissipation

- **Power dissipation is a very important circuit characteristic**
- **CMOS has relatively low static dissipation**
- **Power dissipation was the reason that CMOS technology won over bipolar and NMOS technology for digital IC's**
- **(Extremely) high clock frequencies increase dynamic dissipation**
- **Low V_T increase leakage**
- **Advanced IC design is a continuous struggle to contain the power requirements!**



Power Density

Estimate

- **Furnace: 2000 Watt, r=10cm → P ≈ 6Watt/cm²**
- **Processor chip: 100 Watt, 3cm² → P ≈ 33Watt/cm²**

Power-aware design, design for low power, is blossoming subfield of VLSI Design

Where Does Power Go in CMOS

- **Dynamic Power Consumption**
  - **Charging and discharging capacitors**
- **Short Circuit Currents**
  - **Short circuit path between supply rails during switching**
- **Leakage**
  - **Leaking diodes and transistors**
  - **May be important for battery-operated equipment**

Dynamic Power

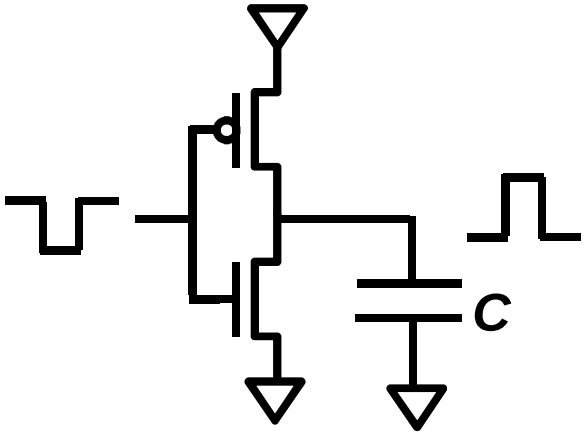
Dynamic Power

- E_i = energy of switching event i
  - (to first order) independent of switching speed
  - depends on process, layout
- Power = Energy/Time
  average power: $P_{avg} = \frac{1}{T}\sum_i E_i$

- E_i = Power-Delay-Product P-D
  - important quality measure

- Energy-Delay-Product E-D
  - combines power*speed performance

Transition Energy

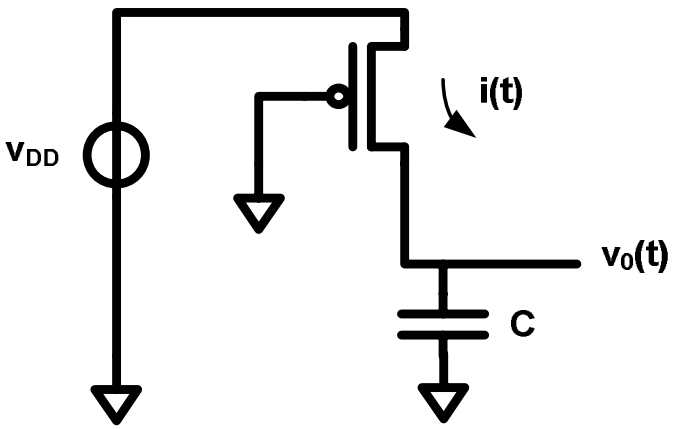


- Assume 1→0→1 transition at input
- Load cap must be charged and discharged again
- How much energy is delivered by power supply?

- Energy is power x time
- Assume timing of input signal such that output swing is complete
- Power supply only delivers energy for charging the capacitor
- Energy on capacitor is dissipated upon discharging

$$E_{delivered} = \int_0^\infty P(t)dt$$

Low-to-High Transition Energy



E_{VDD}: Energy delivered by supply

$$E_{V_{DD}} = \int_0^\infty i(t) V_{DD} dt$$

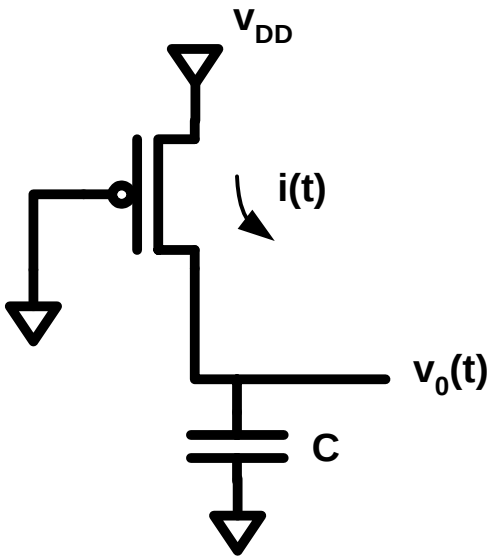
$$= \int_0^\infty C \frac{dv_0}{dt} V_{DD} dt$$

$$= \int_0^{V_{DD}} C V_{DD} dv_0 = \left[C V_{DD} v_0 \right]_0^{V_{DD}}$$

$$= C V_{DD}^2$$

- **Transition energy does not depend on switching speed**
- **Only on load capacitance and (square of) supply voltage**

Low-to-High Transition Energy



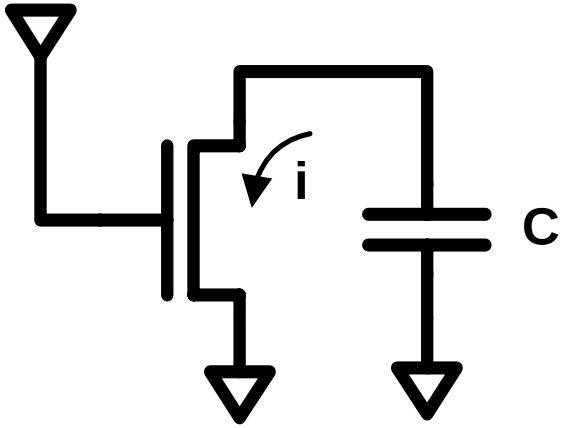
E_{diss}: Energy dissipated in transistor

$$E_{diss} = \int_0^\infty i(V_{DD} - v_0)dt$$

$$= \int_0^\infty iV_{DD}dt - \int_0^\infty iv_0 dt$$

$$= E_{V_{DD}} - E_C = \frac{1}{2}CV_{DD}^2$$

High-to-Low Transition Energy

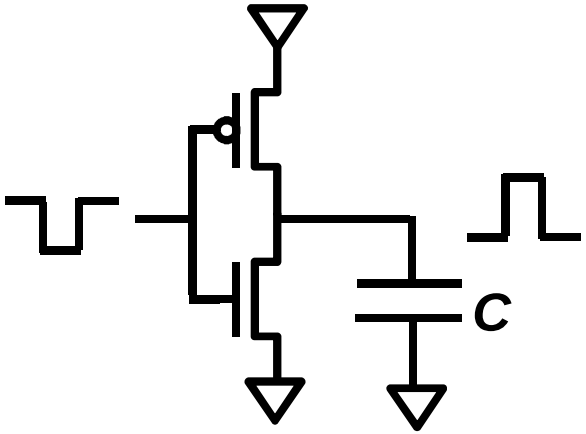


Equivalent circuit

- **On high-to-low transition, supply does not deliver energy**
- **Any energy that is on capacitor after charging, is destroyed (converted into heat, dissipated) upon discharging**

- **Show that this is all the energy on C: $\frac{1}{2}CV_{DD}^2$**

Dissipation Cycle



In one cycle:

- **Source delivers CV_{DD}^2 upon charging C**
- **Half of that is dissipated in pull-up transistor**
- **Rest is stored on capacitor**
- **And is completely destroyed upon discharging C**
- **So, CV_{DD}^2 is energy expended per cycle**

CMOS Dynamic Power Dissipation.

$$Energy = E_{charge} + E_{discharge}$$

$$Power = \frac{Energy}{Time} = \frac{Energy}{transition} \times \frac{\#\,transitions}{time}$$

$$= CV_{DD}^2 \times f$$

- **Independent of transistor on-resistances**
- **Can only reduce *C*, V_{DD} or *f* to reduce power**
- **In this formula, *f* accounts for switching activity (not necessarily a simple regular waveform)**
- **Can also include probability of switching explicitly, take α as switching factor**

Summary

- First Glance
- Digital Gate Characterization (§ 1.3)
- Static Behavior (Robustness) (§ 5.3)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance) (§ 5.4)
  - Capacitances
  - Delay
- Power (§ 5.5)
  - Dynamic Power, Static Power, Metrics