Part 2: Process
Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

Outline

- CMOS Processing
  - Wafer Production
  - CMOS Process Outline
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Only very briefly

Course Material for 02-Process

Chapter 2, 2nd ed.

P = primair, I = Illustratie, O = overslaan

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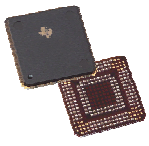
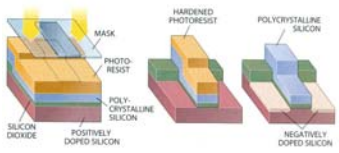
CMOS Processing
- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

IC Technology

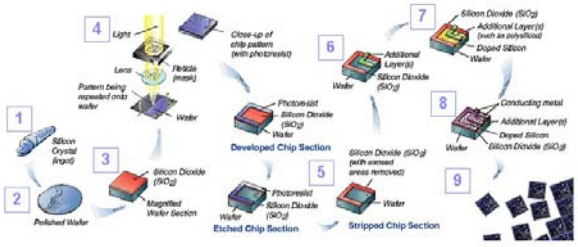


- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist

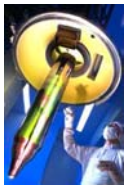


Multiple cycles, 100's STEPS in total

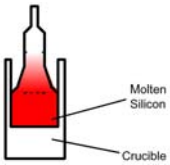
Another Overview of Semiconductor Processing



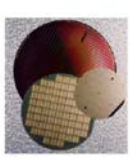
Wafer Processing – Czochralski Method

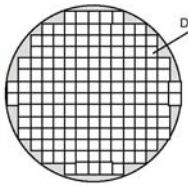


- Start with crucible of molten silicon (≈1425ºC)
- Insert crystal seed in melt
- Slowly rotate/raise seed to form single crystal boule
- After cooling, slice boule into wafers & polish



Wafer Structure

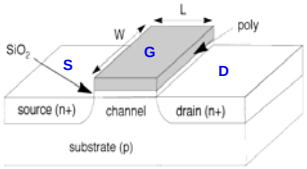


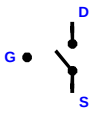


300 mm wafer (sematech)

CMOS Process Outline

MOS Transistor



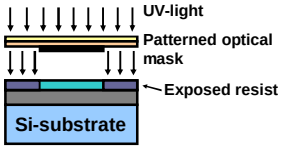


Position of switch depends on gate to source voltage

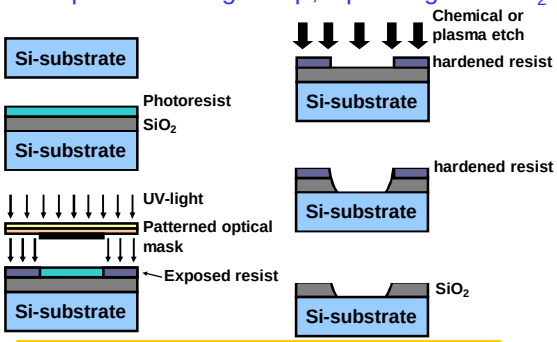
V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

How Patterns on a Chip are Created

- Basic Principle: Photolithography
  - Like projecting an image through a photographic negative (or positive)
- Coat wafer with Photoresist
- Shine UV light through glass mask
- Develop: dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")



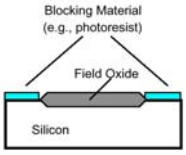
Example: Etching Step, opening of SIO_2



Etching is for removal of material, similar masking principles for deposition (adding of material)

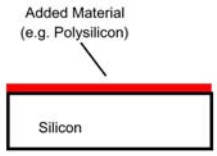
Oxidation

- SiO_2 formed by oxidation
  - Wet oxidation: heat with water (900ºC - 1200 ºC)
  - Dry oxidation:heat with pure oxygen (1200 ºC)
- Oxide occupies more volume
- Alternative: deposition



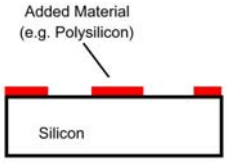
Adding Materials

- Add materials on top of silicon
  - Polysilicon
  - Metal
  - SiO_2
- Methods
  - Vapor deposition
  - Sputtering (Metal ions)



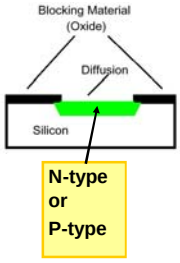
Patterning Added Materials

- Add material to wafer
- Coat with photoresist
- Selectively remove photo resist (PR), after exposure through mask
- Remove unprotected (by PR) material
- Remove remaining PR



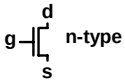
Diffusion

- Modify electrical properties of Si:
  - N-type (extra electrons)
  - or p-type
    (fewer electrons ⇔ extra holes)
- Introduce dopant via ion implant e.g. Arsenic (N), Boron (P)
  (bombard Si surface with ions)
- Blocking implant in selective areas using oxide or PR (photo-resist)
- Allow dopants to diffuse
- Diffusion spreads both vertically, horizontally

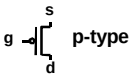


CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



n-type



p-type

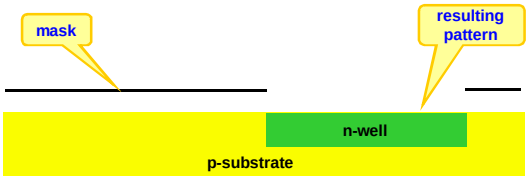
- "on" when V_g is high
- With n-type s/d
- Electrons (n) as carrier
- Built in p-type Si

- "on" when V_g is low
- With p-type s/d
- Holes (p) as carrier
- Built in n-type Si

n-well (for PMOS) in p-type substrate (for NMOS)

Simplified Outline of Process Flow

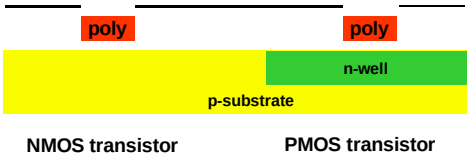
Place n-well to provide properly-doped substrate for n-type, p-type transistors :



NMOS transistor PMOS transistor

Outline of Process Flow, cont'd

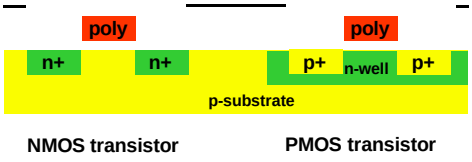
Pattern gate next, to later act as a mask for source and drain diffusions:



NMOS transistor PMOS transistor

Outline of Process Flow, cont'd

Add s/d diffusions, with self-masking by poly gate:

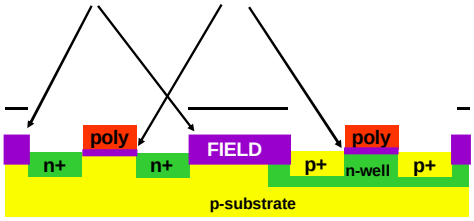


NMOS transistor PMOS transistor

Self-masking: Poly also works as a mask, ensuring good alignment of s/d to gate

Outline of Process Flow, cont'd

With Field Oxide and Gate Oxide shown



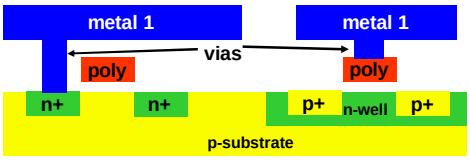
NMOS transistor PMOS transistor

Self-masking: Poly also works as a mask, ensuring good alignment of s/d to gate

Outline of Process Flow, cont'd

Start adding metal layers:

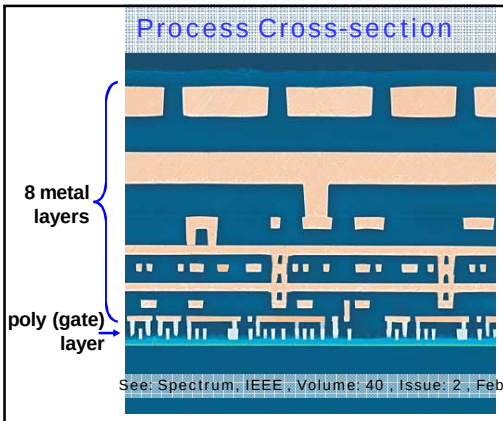
Via: contact hole between metal layers



NMOS transistor PMOS transistor

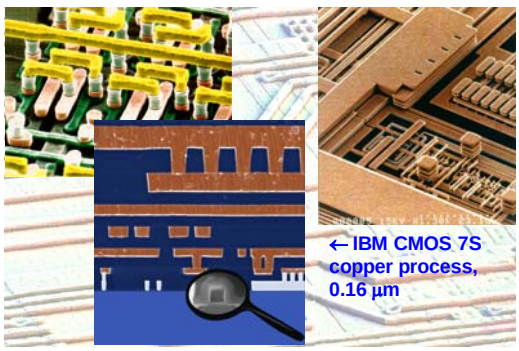
Similar for subsequent metal layers

Process Cross-section



See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

Interconnect Examples (motorola, ibm)



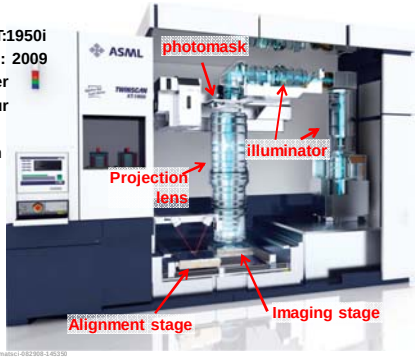
← IBM CMOS 7S copper process, 0.16 µm

IC Recipe Precisely Fixed

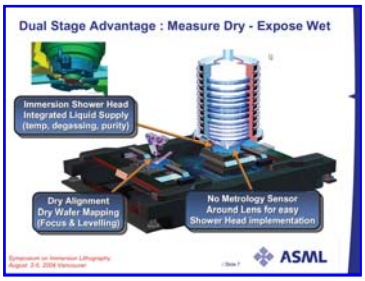
- Process conditions (temperature, time, concentration, ...) very critical
- Many strong compatibility issues of materials and processes
- Very expensive and difficult to tune
- Very expensive equipment and facilities
- Need Billions of turnover for break-even

Wafer Stepper (Step and Scan)

ASML Twinscan XT:1950i
- First production: 2009
- 193 nm ArF Laser
- >175 Wafers/Hour
- <2.5 nm overlay
- 32 nm resolution



Immersion Lithography



- Water, rather than air between lens and wafer
- Improved imaging because of higher index of refraction
- Alignment stage for mapping height profile of wafer in advance of exposure
- DOF < 1µm

Compare Stepper Wafer Size and Resolution to NL scale

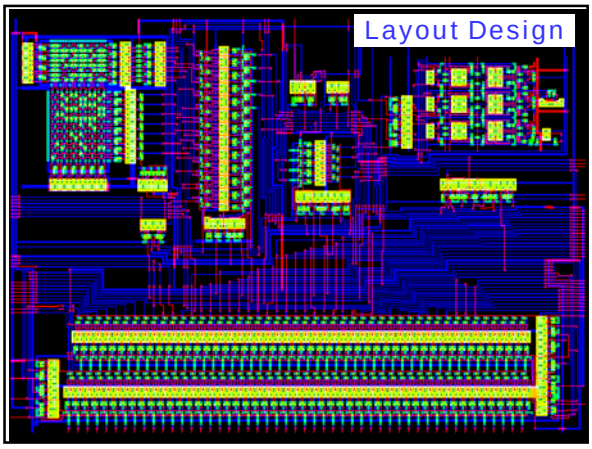
- Resolution: 32nm
- Wafer size: Ø 300mm
- Netherlands: 40.000 km^2 ~ Ø 225km

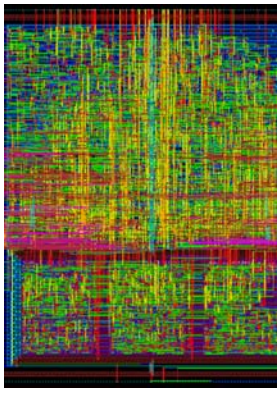
300mm	1	32nm
225km	750x10^3	2.4cm

A 'magnified' waferstepper could 'print' the Netherlands with a resolution of 2.4 cm in 21 sec.

Better than 7.7x10^6 sheets of A4 at 300 dpi …

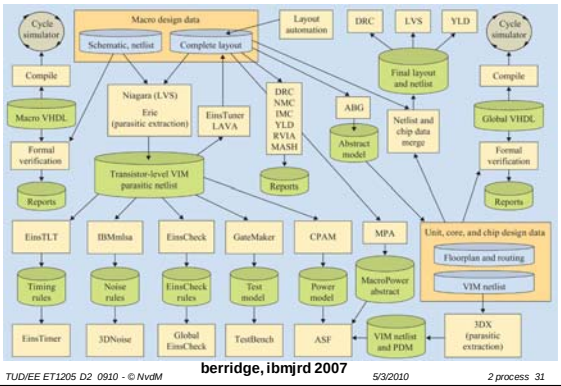
… a pile of paper of 800 m high





- Mostly created by software
- Chip design software is a difficult to tame beast
- But w/o software it is impossible to design a chip

IBM Power6 Physical Design Flow

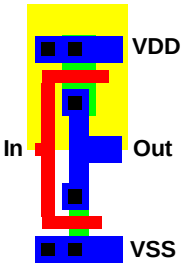


berridge, ibmjrd 2007

Layout Design

Layout Design Concepts

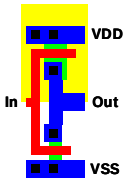
- Layer map
- Layout examples
- Stick diagrams



You should be able to understand such a drawing as well as simpler drawings called 'stick diagram'

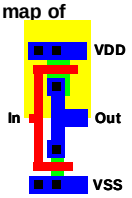
Layout Design

- Layout is design of fabrication masks
- Each mask is drawn in different color
- Layout is not a free-form drawing
  - Most often: Manhattan Layout (rectangular)
  - Sometimes 45-degree angles
  - Curved geometry only for special applications
- Layout should obey Design Rules



Layer Map

- Layers are assigned colors and/or patterns, not always 1 to 1
- Is a matter of convention
- Site-dependent, process dependent, tool dependent
- Be prepared to reverse-engineer layer map of unknown layouts



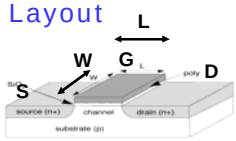
Our Reduced CMOS Layer Map

yellow	nwell	– place for P-transistors
green	active	– source and drain regions
red	polysilicon	– gate material
blue	metal 1	– first interconnect metal
black	contact, via	– hole in interlayer oxide

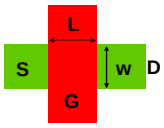
- Our layouts will be composed of these colors
- Or equivalent B/W patterns
- Compare to / instead of color plate 1
- Occasionally, we can use 2nd metal in dark blue
- Note: active = active area = diff = diffusion, well ≈ tub

Transistor Layout

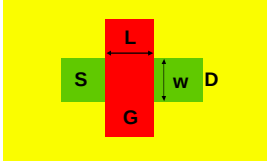
n-well (p-sub)



n-type

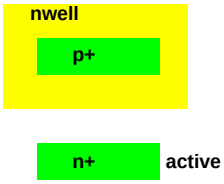


p-type

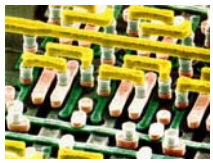


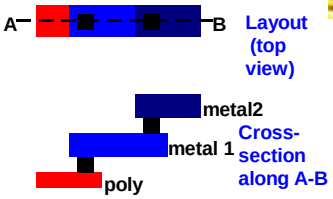
Polarity of Active Area

- Active layer or active area is the source/drain implant layer (area). Usually abbreviated as 'active' only.
- Normally, a so-called select mask determines polarity of active
- See color plate 5
- We will implicitly define polarity of active by n-well
- Or we will even omit the nwell and use the context

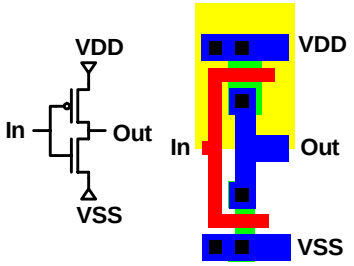


Contact Holes and Vias





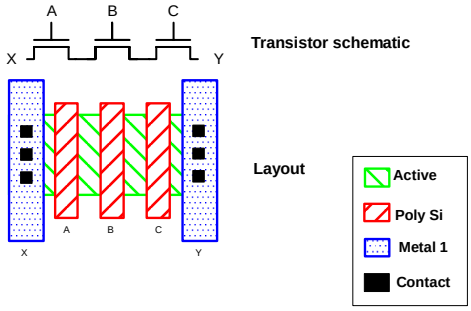
Invertor Layout



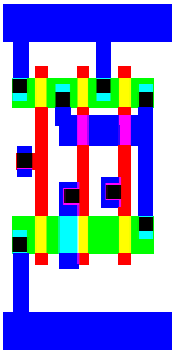
Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

Given such a layout, you should be able to draw the circuit on the left, as well as the different cross-sections

From Schematic to Layout



NAND3_X1 (45nm)



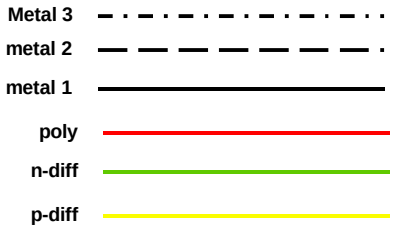
Standard cell:

Fixed pitch and width of VDD and VSS traces

Stick diagrams

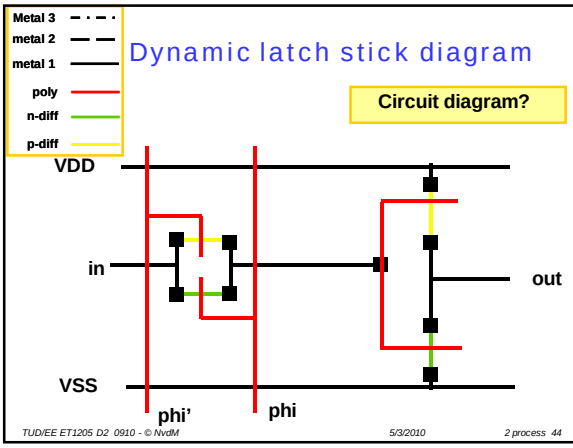
- A stick diagram is a cartoon of a layout.
- Does show components/vias but only relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.

Stick layers



- Caution: stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff

Dynamic latch stick diagram



Design Rules

- The fabrication process will suffer from tolerances
- Chip features will have a practical minimum size to allow them to be fabricated reliably enough (with high enough yield)
- This is captured into a set of precise Design Rules
- Modern processes have terribly complex set of design rules as a compromise between flexibility and manufacturability
- We will ignore this subject
- But you will have to understand it during OP next year.

Summary

- CMOS Processing
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- CMOS Process Outline
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Why we need design rules