Chapter 4

Problems

1. [M, None, 4.x] Figure 0.1 shows a clock-distribution network. Each segment of the clock network (between the nodes) is 5 mm long, 3 μm wide, and is implemented in polysilicon. At each of the terminal nodes (such as *R*) resides a load capacitance of 100 fF.

a. Determine the average current of the clock driver, given a voltage swing on the clock lines of 5 V and a maximum delay of 5 nsec between clock source and destination node *R*. For this part, you may ignore the resistance and inductance of the network

b. Unfortunately the resistance of the polysilicon cannot be ignored. Assume that each straight segment of the network can be modeled as a Π-network. Draw the equivalent circuit and annotate the values of resistors and capacitors.

c. Determine the dominant time-constant of the clock response at node *R*.

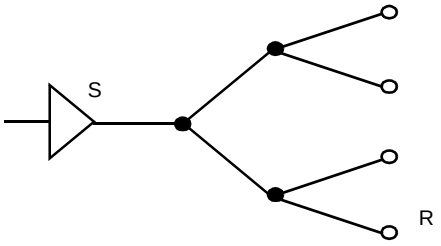

Figure 0.1 Clock-distribution network.

2. [C, SPICE, 4.x] You are designing a clock distribution network in which it is critical to minimize skew between local clocks (*CLK*1, *CLK*2, and *CLK*3). You have extracted the *RC* network of Figure 0.2, which models the routing parasitics of your clock line. Initially, you notice that the path to *CLK*3 is shorter than to *CLK*1 or *CLK*2. In order to compensate for this imbalance, you insert a transmission gate in the path of *CLK*3 to eliminate the skew.

a. Write expressions for the time-constants associated with nodes *CLK*1, *CLK*2 and *CLK*3. Assume the transmission gate can be modeled as a resistance R_3.

b. If $R_1 = R_2 = R_4 = R_5 = R$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C$, what value of R_3 is required to balance the delays to *CLK*1, *CLK*2, and *CLK*3?

c. For $R = 750\Omega$ and $C = 200$fF, what (W/L)'s are required in the transmission gate to eliminate skew? Determine the value of the propagation delay.

d. Simulate the network using SPICE, and compare the obtained results with the manually obtained numbers.

3. [M, None, 4.x]Consider a CMOS inverter followed by a wire of length *L*. Assume that in the reference design, inverter and wire contribute equally to the total propagation delay t_{pref}. You may assume that the transistors are velocity-saturated. The wire is scaled in line with the **ideal wire scaling model**. Assume initially that the wire is **a local wire**.

a. Determine the new (total) propagation delay as a a function of t_{pref}, assuming that technology and supply voltage scale with a factor 2. Consider only first-order effects.

b. Perform the same analysis, assuming now that the wire scales a **global wire**, and the wire length scales inversely proportional to the technology.

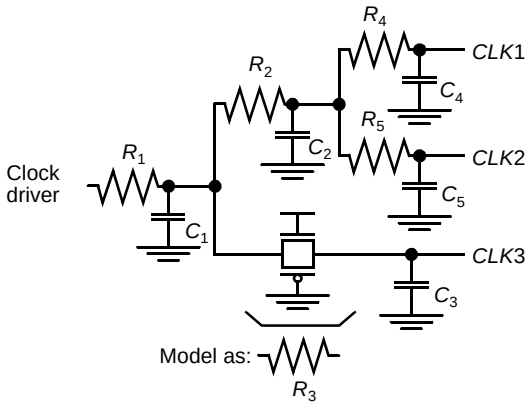

Figure 0.2 *RC* clock-distribution network.

c. Repeat b, but assume now that the wire is scaled along the constant resistance model. You may ignore the effect of the fringing capacitance.

d. Repeat b, but assume that the new technology uses a better wiring material that reduces the resistivity by half, and a dielectric with a 25% smaller permittivity.

e. Discuss the energy dissipation of part a. as a function of the energy dissipation of the original design E_{ref}.

f. Determine for each of the statements below if it is true, false, or undefined, and explain in one line your answer.

- When driving a small fan-out, increasing the driver transistor sizes raises the short-circuit power dissipation.
- Reducing the supply voltage, while keeping the threshold voltage constant decreases the short-circuit power dissipation.
- Moving to Copper wires on a chip will enable us to build faster adders.
- Making a wire wider helps to reduce its RC delay.
- Going to dielectrics with a lower permittivity will make RC wire delay more important.

4. [M, None, 4.x] A two-stage buffer is used to drive a metal wire of 1 cm. The first inverter is of minimum size with an input capacitance Ci=10 fF and an internal propagation delay t_{p0}=50 ps and load dependent delay of 5ps/fF. The width of the metal wire is 3.6 μm. The sheet resistance of the metal is 0.08 Ω/ , the capacitance value is 0.03 fF/μm2 and the fringing field capacitance is 0.04fF/μm.

a. What is the propagation delay of the metal wire?

b. Compute the optimal size of the second inverter. What is the minimum delay through the buffer?

c. If the input to the first inverter has 25% chance of making a 0-to-1 transition, and the whole chip is running at 20MHz with a 2.5 supply voltage, then what's the power consumed by the metal wire?

5. [M, None, 4.x]To connect a processor to an external memory an off -chip connection is necessary. The copper wire on the board is 15 cm long and acts as a transmission line with a characteristic impedance of 100Ω(See Figure 0.3). The memory input pins present a very high impedance which can be considered infinite. The bus driver is a CMOS inverter consisting of very large devices: (50/0.25) for the NMOS and (150/0.25) for the PMOS, where all sizes are

in µm. The minimum size device, (0.25/0.25) for NMOS and (0.75/0.25) for PMOS, has the on resistance 35 kΩ.

a. Determine the time it takes for a change in the signal to propagate from source to destination (time of flight). The wire inductance per unit length equals $75*10^{-8}$ H/m.

b. Determine how long it will take the output signal to stay within 10% of its final value. You can model the driver as a voltage source with the driving device acting as a series resistance. Assume a supply and step voltage of 2.5V. Hint: draw the lattice diagram for the transmission line.

c. Resize the dimensions of the driver to minimize the total delay.

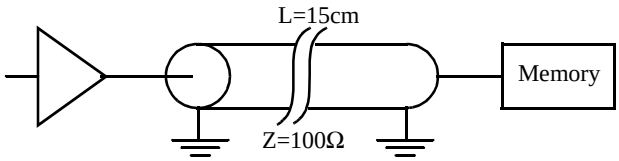

Figure 0.3 The driver, the connecting copper wire and the memory block being accessed.

6. [M, None, 4.x] A two stage buffer is used to drive a metal wire of 1 cm. The first inverter is a minimum size with an input capacitance C_i=10 fF and a propagation delay t_{p0}=175 ps when loaded with an identical gate. The width of the metal wire is 3.6 µm. The sheet resistance of the metal is 0.08 Ω/ , the capacitance value is 0.03 fF/µm2 and the fringing field capacitance is 0.04 fF/µm.

a. What is the propagation delay of the metal wire?

b. Compute the optimal size of the second inverter. What is the minimum delay through the buffer?

7. [M, None, 4.x] For the RC tree given in Figure 0.4 calculate the Elmore delay from node A to node B using the values for the resistors and capacitors given in the below in Table 0.1.

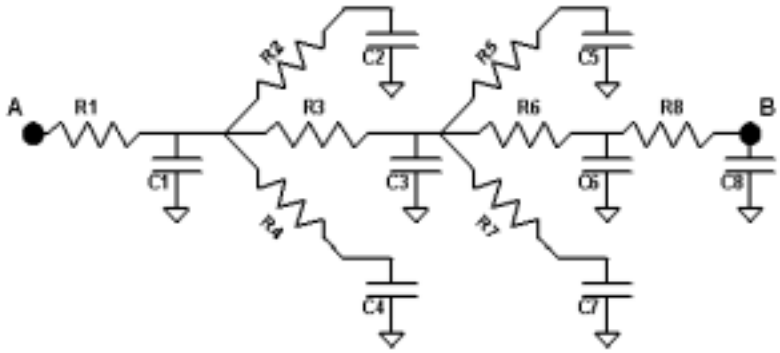

Figure 0.4 RC tree for calculating the delay

Table 0.1 Values of the components in the RC tree of Figure 0.4

Resistor	Value(Ω)	Capacitor	Value(fF)
R1	0.25	C1	250
R2	0.25	C2	750
R3	0.50	C3	250
R4	100	C4	250
R5	0.25	C5	1000
R6	1.00	C6	250
R7	0.75	C7	500
R8	1000	C8	250

8. [M, SPICE, 4.x] In this problem the various wire models and their respective accuracies will be studied.

a. Compute the 0%-50% delay of a 500um x 0.5um wire with resistance of 0.08 Ω/ , with area capacitance of 30aF/um2, and fringing capacitance of 40aF/um. Assume the driver has a 100Ω resistance and negligible output capacitance.

- Using a lumped model for the wire.
- Using a PI model for the wire, and the Elmore equations to find tau. (see Chapter 4, figure 4.26).
- Using the distributed RC line equations from Chapter 4, section 4.4.4.

b. Compare your results in part a. using spice (be sure to include the source resistance). For each simulation, measure the 0%-50% time for the output

- First, simulate a step input to a lumped R-C circuit.
- Next, simulate a step input to your wire as a PI model.
- Unfortunately, our version of SPICE does not support the distributed RC model as described in your book (Chapter 4, section 4.5.1). Instead, simulate a step input to your wire using a PI3 distributed RC model.

9. [M, None, 4.x] A standard CMOS inverter drives an aluminum wire on the first metal layer. Assume Rn=4kΩ, Rp=6kΩ. Also, assume that the output capacitance of the inverter is negligible in comparison with the wire capacitance. The wire is .5um wide, and the resistivity is 0.08 Ω/ ..

a. What is the "critical length" of the wire?

b. What is the equivalent capacitance of a wire of this length? (For your capacitance calculations, use Table 4.2 of your book , assume there's field oxide underneath and nothing above the aluminum wire)

10. [M, None, 4.x] A 10cm long lossless transmission line on a PC board (relative dielectric constant = 9, relative permeability = 1) with characteristic impedance of 50Ω is driven by a 2.5V pulse coming from a source with 150Ω resistance.

a. If the load resistance is infinite, determine the time it takes for a change at the source to reach the load (time of flight).

Now a 200Ω load is attached at the end of the transmission line.

b. What is the voltage at the load at t = 3ns?

c. Draw lattice diagram and sketch the voltage at the load as a function of time. Determine how long does it take for the output to be within 1 percent of its final value.

11. [C, SPICE, 4.x] Assume V_{DD}=1.5V. Also, use short-channel transistor models forhand analysis.

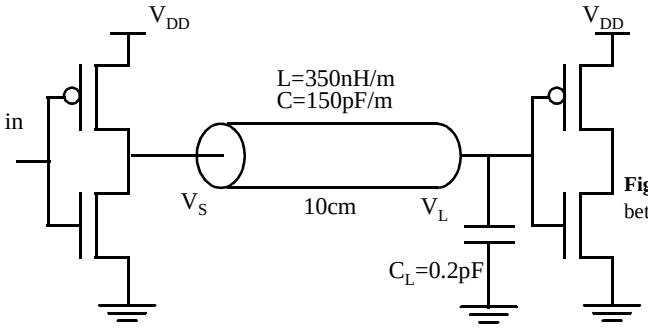

Figure 0.5 Transmission line between two inverters

a. The Figure 0.5 shows an output driver feeding a 0.2 pF effective fan-out of CMOS gates through a transmission line. Size the two transistors of the driver to optimize the delay. Sketch waveforms of V_S and V_L, assuming a square wave input. Label critical voltages and times.

b. Size down the transistors by m times (m is to be treated as a parameter). Derive a first order expression for the time it takes for V_L to settle down within 10% of its final voltage level.Compare the obtained result with the case where no inductance is associated with the wire.Please draw the waveforms of V_L for both cases, and comment.

c. Use the transistors as in part a). Suppose C_L is changed to 20pF. Sketch waveforms of V_S and V_L, assuming a square wave input. Label critical voltages and instants.

d. Assume now that the transmission line is lossy. Perform Hspice simulation for three cases: R=100 Ω/cm; R=2.5 Ω/cm; R=0.5 Ω/cm. Get the waveforms of V_S, V_L and the middle point of the line. Discuss the results.

12. [M, None, 4.x] Consider an isolated 2mm long and 1μm wide M1(Metal1)wire over a silicon substrate driven by an inverter that has zero resistance and parasitic output capccitance. How will the wire delay change for the following cases? Explain your reasoning in each case.

a. If the wire width is doubled.

b. If the wire length is halved.

c. If the wire thickness is doubled.

d. If thickness of the oxide between the M1 and the substrate is doubled.

13. [E, None, 4.x] In an ideal scaling model, where all dimensions and voltages scale with a factor of S >1 :

a. How does the delay of an inverter scale?

b. If a chip is scaled from one technology to another where all wire dimensions,including the vertical one and spacing, scale with a factor of S, how does the wire delayscale? How does the overall operating frequency of a chip scale?

c. Repeat b) for the case where everything scales, except the vertical dimension of wires (it stays constant).