

CMOS INVERTER

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4 inverter 1

Course Material for Inverter

Chapter 5, 2nd ed.

P = primair, I = Illustratie, O = overslaan

P	5.1	Introduction	180
P	5.2	The Static CMOS inverter - intuitive	181 - 184
P	1.3.2	Functionality and Robustness	18 - 27
P	5.3	Evaluating the Robustness ...	184 - 191
I	5.3.3	Robustness Revisited	191 - 193
P	1.3.3	Performance	27 - 30
I	5.4	Performance of the CMOS inverter	193 - 213
P	1.3.4	Power and Energy Consumption	30 - 31
I	5.5	Power, Energy, and Energy-Delay	213 - 223
O	5.5.2	Static Consumption	223 - 225
O	5.5.3	Putting it All Together	225 - 227
O	5.5.4	Analyzing Power Consumption using SPICE	227 - 229
O	5.6	Perspective: Technology scaling...	229 - 231
P	5.7	Summary	232 - 233

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The CMOS Inverter - Outline

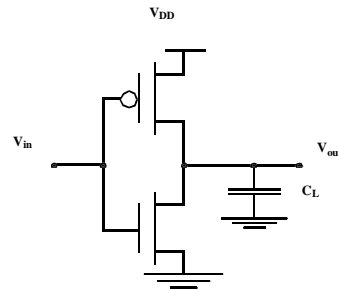
- First Glance
- Digital Gate Characterization
- Static Behavior (Robustness)
 - VTC
 - Switching Threshold
 - Noise Margins
- Dynamic Behavior (Performance)
 - Capacitances
 - Delay
- Power
 - Dynamic Power, Static Power, Metrics

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The CMOS Inverter: A First Glance

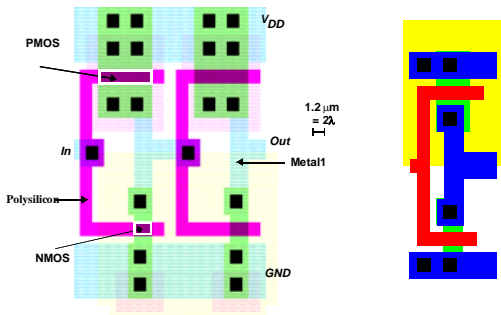


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CMOS Inverters (1)

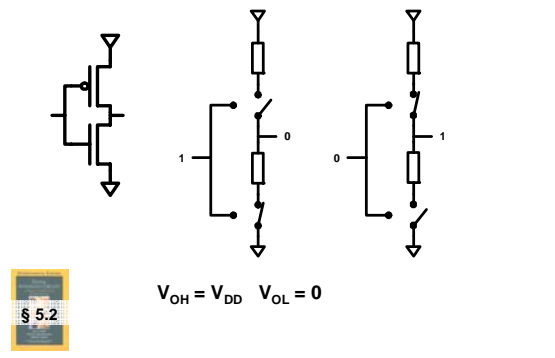


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CMOS Inverter Operation Principle



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Digital Gate Fundamental Parameters

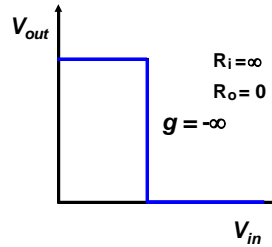
- **Functionality**
- **Reliability, Robustness**
- **Area**
- **Performance**
 - Speed (delay)
 - Power Consumption
 - Energy

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The Ideal Inverter

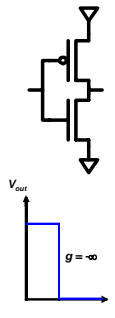


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Static CMOS Properties.



Basic inverter belongs to class of **static circuits**: output always connected to either V_{DD} or V_{SS} . **Not ideal but:**

- **Rail to rail voltage swing**
- **Ratio less design**
- **Low output impedance**
- **Extremely high input impedance**
- **No static power dissipation**
- **Good noise properties/margins**

Exercise: prioritize the list above

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Voltage Transfer Characteristic (VTC)

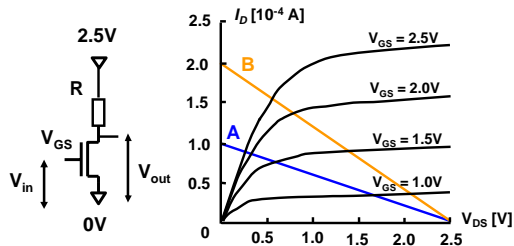


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Load Line (Ckt Theory)



Exercise:

The **blue** load line A corresponds to $R =$
 The **orange** load line B corresponds to $R =$
 With load line A and $V_{GS} = 1V$, $V_{out} =$
 Draw a graph $V_{out}(V_{in})$ for load line A and B

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PMOS Load Lines

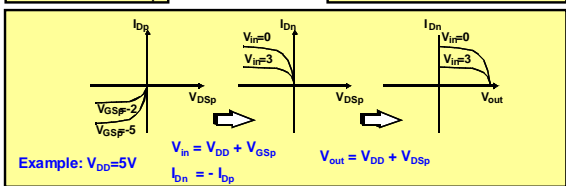
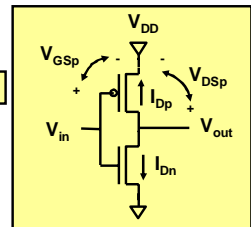
Goal: Combine I_{Dn} and I_{Dp} in one graph

Kirchoff:

$$V_{in} = V_{DD} + V_{GSp}$$

$$I_{Dn} = -I_{Dp}$$

$$V_{out} = V_{DD} + V_{DSp}$$

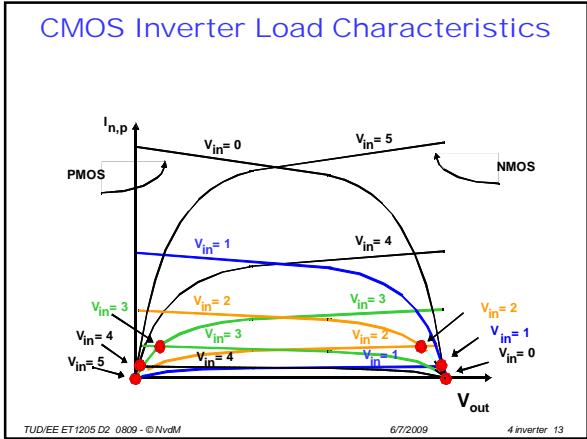


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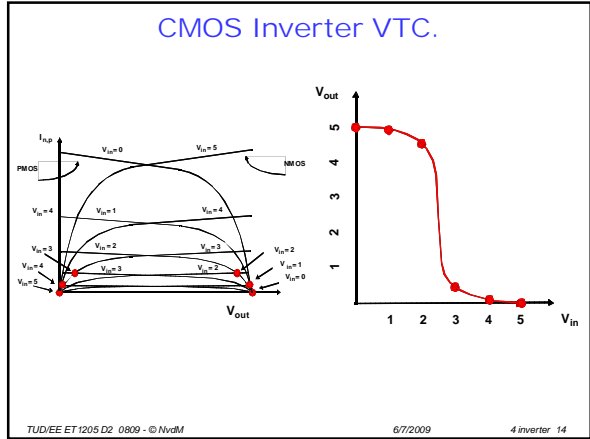
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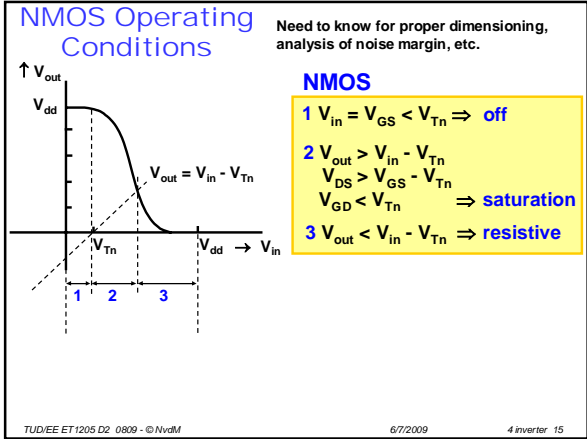
CMOS Inverter Load Characteristics



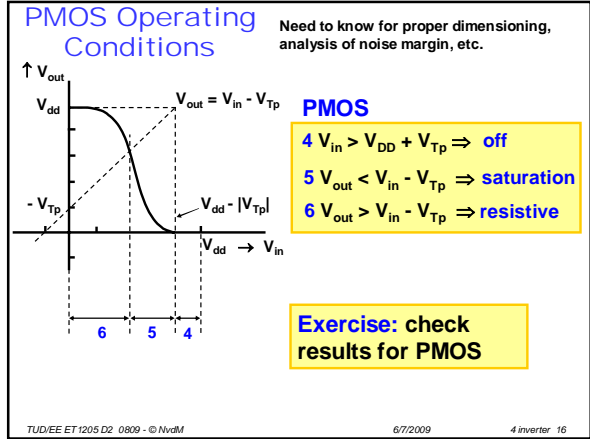
CMOS Inverter VTC.



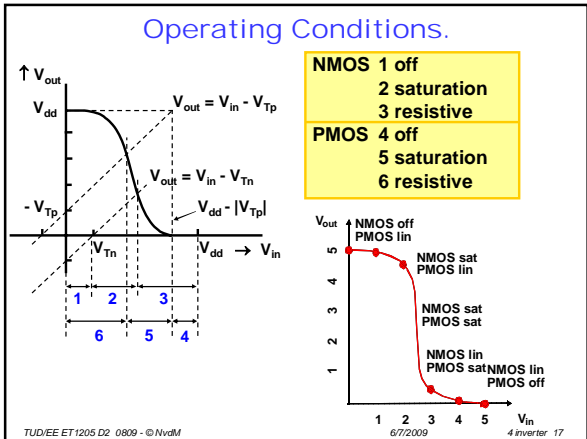
NMOS Operating Conditions



PMOS Operating Conditions



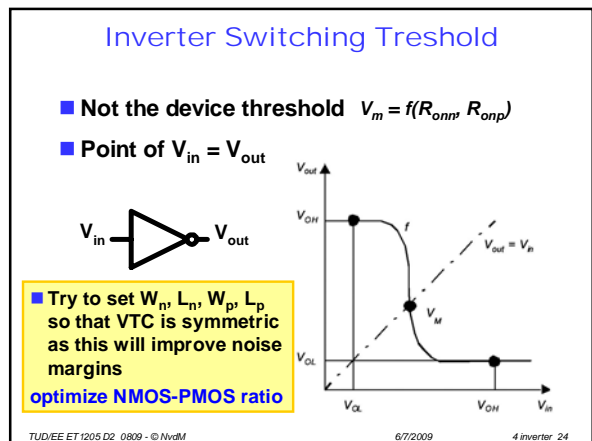
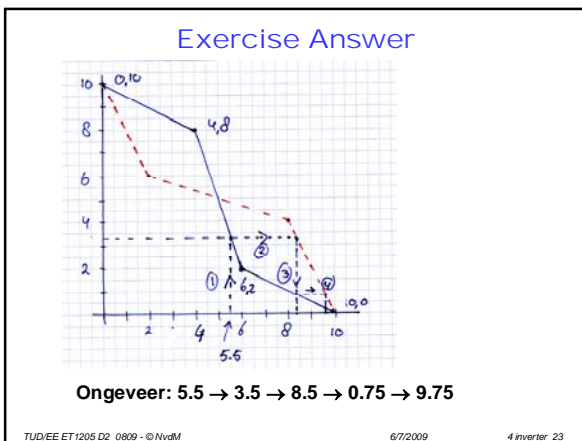
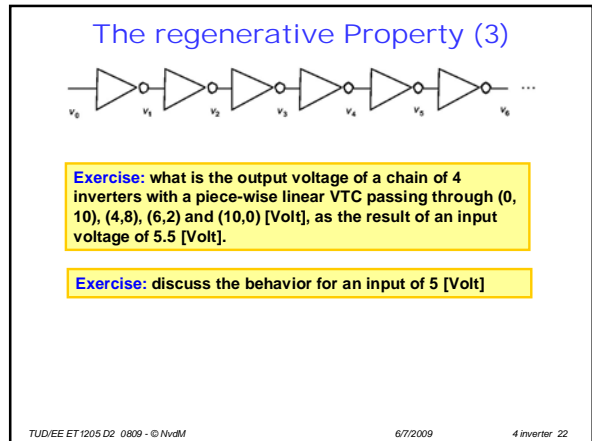
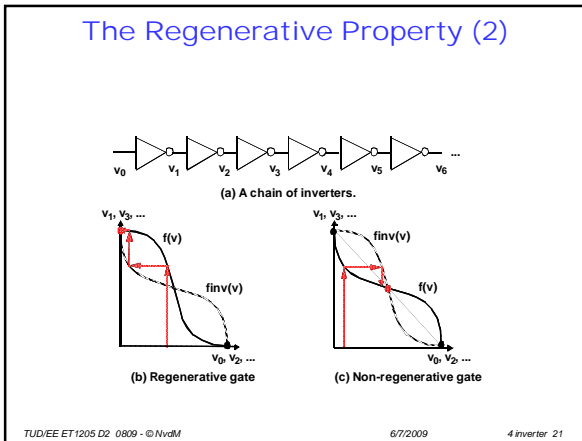
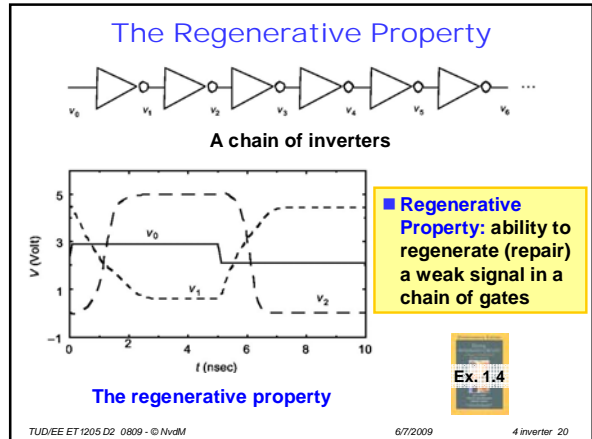
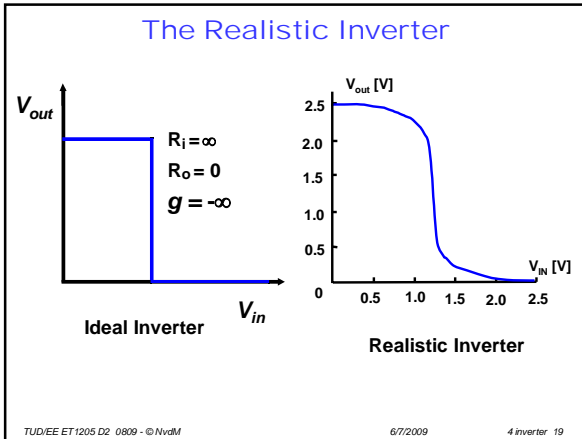
Operating Conditions.



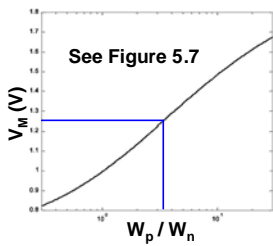
Inverter Static Behavior

- Regeneration
- Noise margins
- Delay metrics





Simulated Gate Switching Threshold



See Figure 5.7

Electrical Design Rule

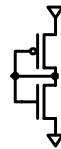
$$W_p \approx 2.5 W_n$$

- Assumes $L_p = L_n$
- Should be applied consistently

- Symmetrical VTC $\Rightarrow V_m \approx \frac{1}{2} V_{DD} \Rightarrow W_p/W_n \approx \square$
- In practice: choose somewhat smaller value of W_p/W_n
- Why? \square

Inverter Switching Threshold Analytical Derivation

- V_M is V_{in} such that $V_{in} = V_{out}$
- $V_{DS} = V_{GS} \Leftrightarrow V_{GD} = 0 \Rightarrow$ saturation
 - Assume $V_{DSAT} < V_M - V_T$ (velocity saturation)
 - Ignore channel length modulation (for simplicity – is it allowed?)
- V_M follows from
 - $I_{DSATn}(V_M) = -I_{DSATp}(V_M)$



Inverter Switching Threshold Analytical Derivation (ctd)

$$I_{DSATn}(V_M) = -I_{DSATp}(V_M) \quad I_D = kV_{DSAT}(V_{GS} - V_T - V_{DSAT}/2)$$

$$\Leftrightarrow k_n V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2) = -k_p V_{DSATp} (V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)$$

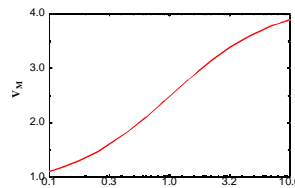
$$\Leftrightarrow \frac{k_p}{k_n} = \frac{-V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2)}{V_{DSATp} (V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)} \quad k = \frac{W}{L} k'$$

$$\Rightarrow \frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp} (V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)}$$

- See Example 5.1:
- $(W/L)_p = 3.5 (W/L)_n$ for typical conditions and $V_M = \frac{1}{2} V_{DD}$
- Usually: $L_n = L_p$

Gate Switching Threshold w/o Velocity Saturation.

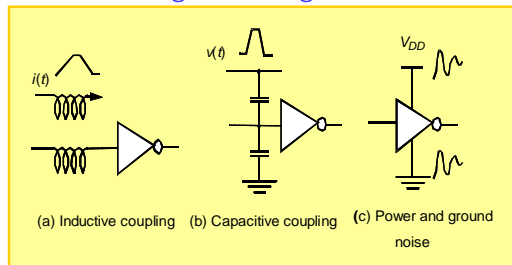
- Long channel approximation
- Applicable with low V_{DD}



Exercise (Problem 5.1): derive V_M for long-channel approximation as shown below

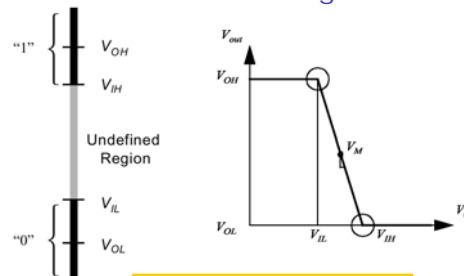
$$V_M = \frac{r(V_{DD} - V_{Tp} + V_{Tn})}{1+r} \quad \text{with} \quad r = \sqrt{\frac{-k_p}{k_n}}$$

Noise in Digital Integrated Circuits



Study behavior of static CMOS Gates with noisy signals

Noise Margins



- V_{OL} = Output Low Voltage
- V_{IL} = Input Low Voltage
- $V_{OH}, V_{IH} = \dots$

Noise Margins

$NM_H = V_{OH} - V_{IH} = \text{High Noise Margin}$
 $NM_L = V_{IL} - V_{OL} = \text{Low Noise Margin}$

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Noise Margin for Realistic Gates

Exercise: explain significance of slope = -1 for noise margin

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Noise Margin Calculation

Piece-wise linear approximation of VTC

$g = \text{gain factor (slope of VTC)}$

We know how to compute V_M
Next: how to compute g

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = -\frac{V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL}$$

§ 5.3.2

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Noise Margin Calculation (2)

■ Approximate g as the slope in V_{out} vs. V_{in} at $V_{in} = V_M$
 $k_n V_{DSATn} (V_{in} - V_{Tn} - V_{DSATn} / 2)(1 + \lambda_n V_{out}) +$
 $k_p V_{DSATp} (V_{in} - V_{DD} - V_{Tp} - V_{DSATp} / 2)(1 + \lambda_p V_{out} - \lambda_p V_{DD}) = 0$
 $g = \frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_M} \approx \frac{1+r}{(V_M - V_T - V_{DSATp} / 2)(\lambda_n - \lambda_p)} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$

■ Mostly determined by technology
 ■ See example 5.2

■ **Exercise:** verify calculation
 ■ **Exercise:** explain why we add channel length modulation to the I_D expressions (we did not do this to determine V_M)

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Dynamic Behavior (Performance)

- Capacitances
- Delay

■ But: we take much simpler model for capacitances compared to book.
 ■ See the syllabus.
 ■ § 5.4.1 of book is only illustration.

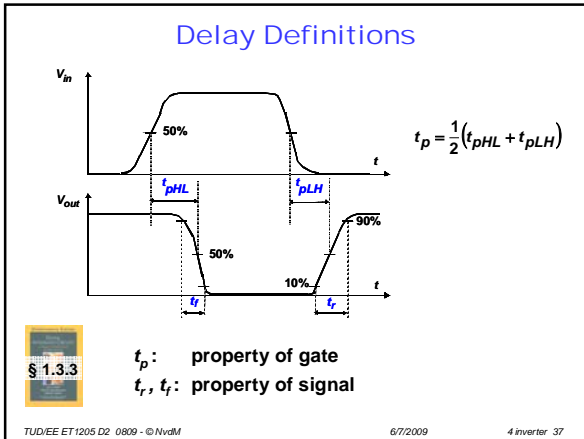
§ 5.4

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CMOS Inverters

- What causes the delay?
- What is R_{on} ?
- Where are the capacitances?
- Which capacitances determine T_p ?

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CMOS Inverter Rise/Fall Delay

- Goal: determine t_r , t_f and t_p
- First: compute relevant capacitances
- Second: determine equivalent R_{on}
- Third: compute RC delay (τ) and scale result
- Assume: ideal source, step input

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Modeling

From module 1- devices

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Modeling (2)

$R = R_{on1}$
 $C = C_{D1} + C_{D2} + C_{G3} + C_{G4}$
 $V_s = 0$

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Modeling (3)

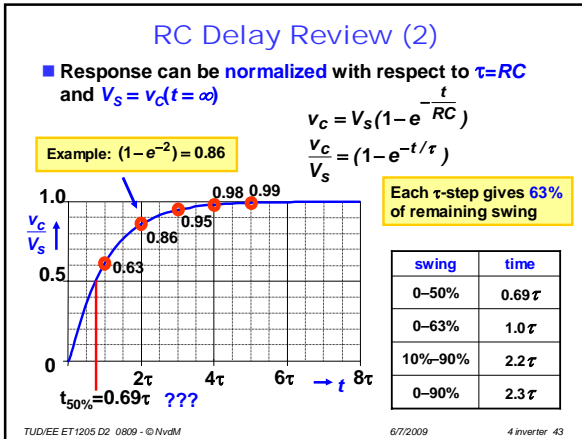
- Delay can be modeled using RC circuit
 - First order simplified model
- R is (linearized) on-resistance of active transistor
- C is sum of (linearized) C's that are switched
 - Typically, C_G of driven gate, C_D of driving gate
 - Plus relevant interconnect C
 - Might need to include interconnect R in model
- V_s is final voltage of delay node (initial voltage determined by previous state)

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RC Delay Review (1)

$v_c(t) = v_c(\infty) + (v_c(t_0) - v_c(\infty))e^{-(t-t_0)/\tau}$
 $RC \frac{dv_c}{dt} = V_s - v_c$
 $v_c = V_s(1 - e^{-\frac{t}{RC}})$

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$$\frac{v_C}{V_S} = (1 - e^{-t/\tau})$$

$$\Downarrow$$

$$0.5 = (1 - e^{-t_{50\%}/\tau})$$

$$\Downarrow$$

$$0.5 = e^{-t_{50\%}/\tau}$$

$$\Downarrow$$

$$2 = e^{t_{50\%}/\tau}$$

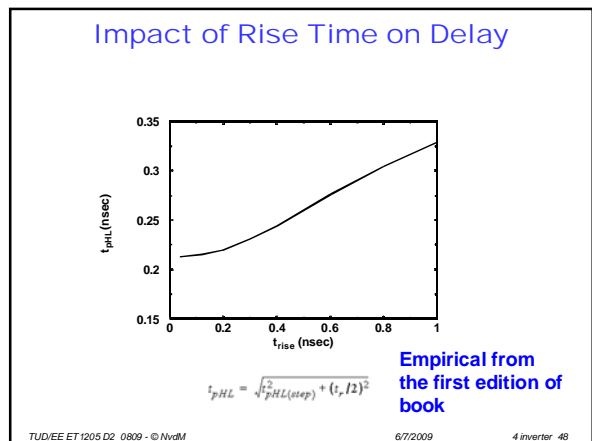
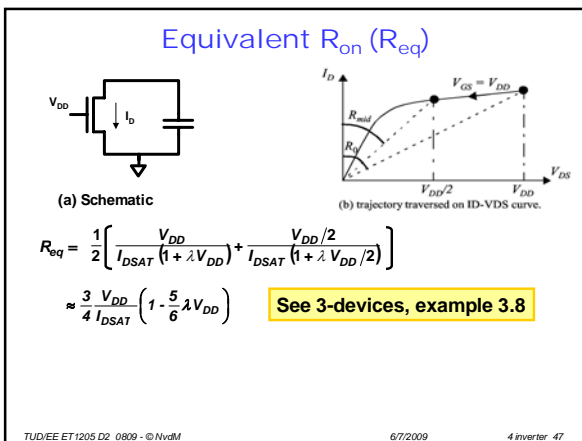
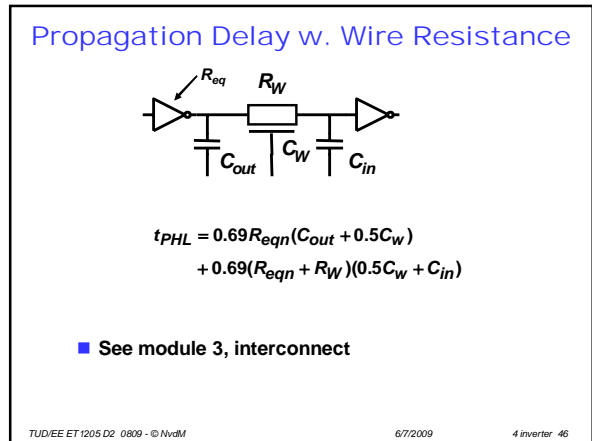
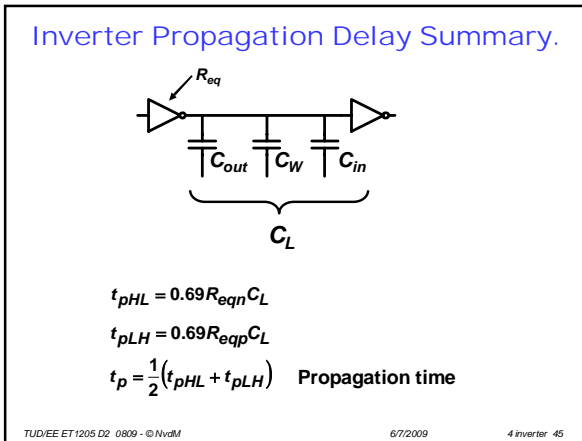
$$\Downarrow$$

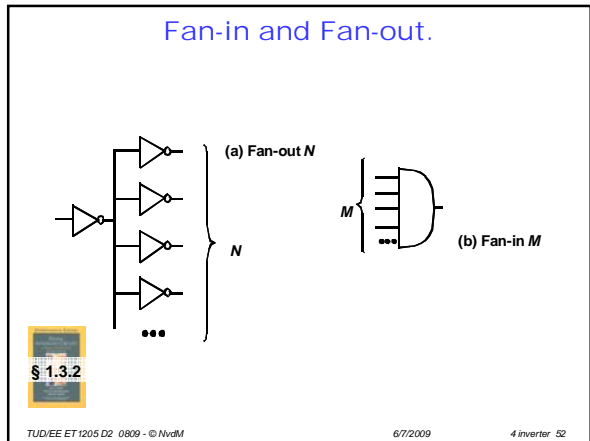
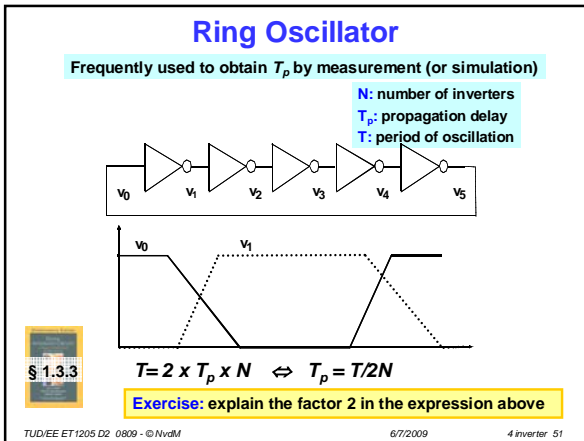
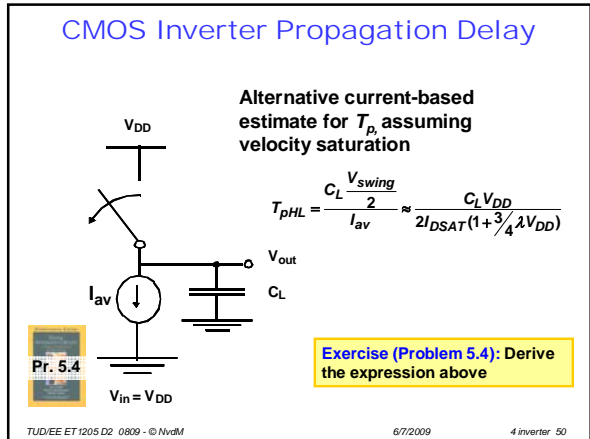
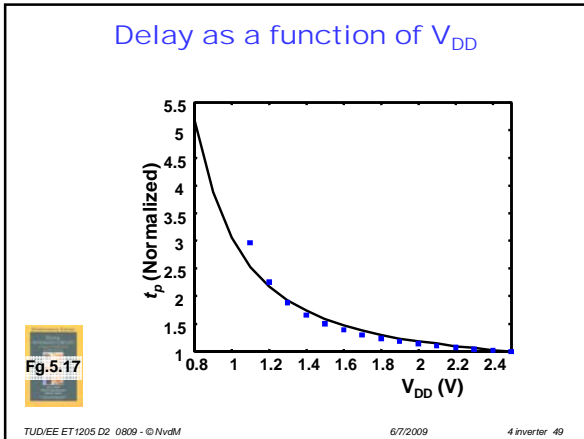
$$\ln(2) = 0.69 = t_{50\%}/\tau$$

$$\Downarrow$$

$$t_{50\%} = 0.69\tau$$

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Power (§ 5.5)

- Dynamic Power
- Static Power
- Metrics

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- ### CMOS Power Dissipation
- Power dissipation is a **very important** circuit characteristic
 - CMOS has relatively low static dissipation
 - Power dissipation was the reason that CMOS technology won over bipolar and NMOS technology for digital IC's
 - (Extremely) high clock frequencies increase dynamic dissipation
 - Low V_T increase leakage
 - Advanced IC design is a continuous struggle to contain the power requirements!
- § 1.3.4** **§ 5.5**
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Power Density



Estimate

- Furnace: 2000 Watt, $r=10\text{cm}$ → $P \approx 6\text{Watt/cm}^2$
- Processor chip: 100 Watt, 3cm^2 → $P \approx 33\text{Watt/cm}^2$

Power-aware design, design for low power, is blossoming subfield of VLSI Design

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Where Does Power Go in CMOS

- **Dynamic Power Consumption**
Charging and discharging capacitors
- **Short Circuit Currents**
Short circuit path between supply rails during switching
- **Leakage**
Leaking diodes and transistors
May be important for battery-operated equipment

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Dynamic Power

Dynamic Power

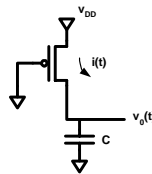
- E_i = energy of switching event i
 - (to first order) independent of switching speed
 - depends on process, layout
- Power = Energy/Time
$$P = \frac{1}{T} \sum_i E_i$$
- E_i = Power-Delay-Product P-D
 - important quality measure
- Energy-Delay-Product E-D
 - combines power*speed performance

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Low-to-High Transition Energy



Equivalent circuit for low-to-high transition

E_C - Energy stored on C

$$E_C = \int_0^\infty i v_0 dt \quad v_0 = v_0(t) \quad i = i(t) = C \frac{dv_0}{dt}$$

$$= \int_0^\infty C v_0 \frac{dv_0}{dt} dt$$

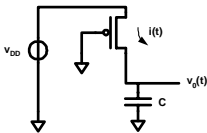
$$= \int_0^{V_{DD}} C v_0 dv_0 = \frac{1}{2} C v_0^2 \Big|_0^{V_{DD}} = \frac{1}{2} C V_{DD}^2$$

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Low-to-High Transition Energy



$E_{V_{DD}}$ Energy delivered by supply

$$E_{V_{DD}} = \int_0^\infty i(t) V_{DD} dt = \int_0^{V_{DD}} C V_{DD} \frac{dv_0}{dt} dt = C V_{DD}^2$$

$$E_{V_{DD}} = C V_{DD}^2 \quad E_C = \frac{1}{2} C V_{DD}^2$$

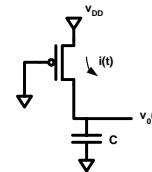
Where is the rest?

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Low-to-High Transition Energy



E_{diss} Energy dissipated in transistor

$$E_{diss} = \int_0^\infty i (V_{DD} - v_0) dt$$

$$= \int_0^\infty i V_{DD} dt - \int_0^\infty i v_0 dt$$

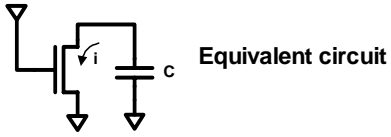
$$= E_{V_{DD}} - E_C \quad \text{☺}$$

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High-to-Low Transition Energy



Exercise: Show that the energy that is dissipated in the transistor upon discharging C from V_{DD} to 0 equals $E_{diss} = \frac{1}{2}CV_{DD}^2$

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CMOS Dynamic Power Dissipation.

$$Energy = E_{charge} + E_{discharge}$$

$$Power = \frac{Energy}{Time} = \frac{Energy}{transition} \times \frac{\#transitions}{time}$$
$$= CV_{DD}^2 \times f$$

- Independent of transistor on-resistances
- Can only reduce C, V_{DD} or f to reduce power
- In this formula, f accounts for switching activity (not necessarily a simple regular waveform)

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Summary

- First Glance
- Digital Gate Characterization (§ 1.3)
- Static Behavior (Robustness) (§ 5.3)
 - VTC
 - Switching Threshold
 - Noise Margins
- Dynamic Behavior (Performance) (§ 5.4)
 - Capacitances
 - Delay
- Power (§ 5.5)
 - Dynamic Power, Static Power, Metrics

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