

Part 2: Process

Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

Outline

- **CMOS Processing**
 - **Wafer Production**
 - **CMOS Process Outline**
 - **Photolithography**
 - **Material Deposition & Removal**
 - **Oxide Growth & Removal**
- **Layout Design**
 - **Layer map**
 - **Layout examples**
 - **Stick diagrams**
- **Design Rules**
 - **Only very briefly**

Course Material for 02-Process

Chapter 2, 2nd ed.

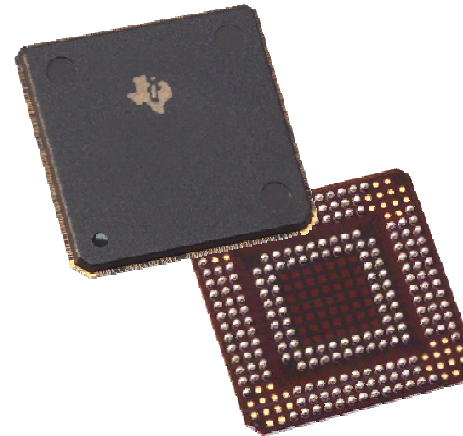
P = primair, I = Illustratie, O = overslaan

P	2.1	Introduction	36
P	2.2-2.2.2	Manufacturing CMOS Integrated Circuits	36-41
P	2.2.3	Some Recurring Process Steps	41-42
P	2.2.4	Simplified CMOS Process Flow	42-44
I	2.3	Design Rules	47-50
I	2.4	Packaging Integrated Circuits	51-61
I	2.5	Perspective - Trends in Process Technology	61-64
P	2.6	Summary	64
I	Insert A	IC Layout	67-71

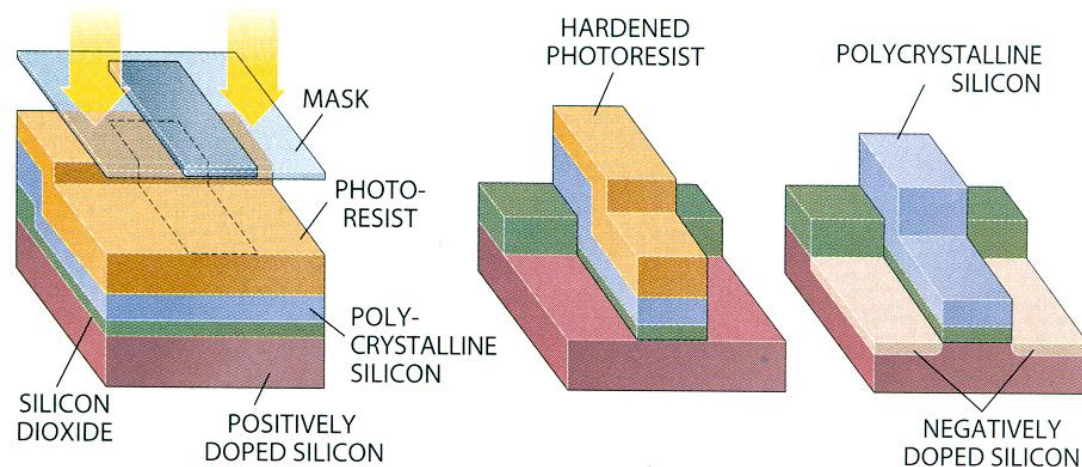
CMOS Processing

- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

IC Technology

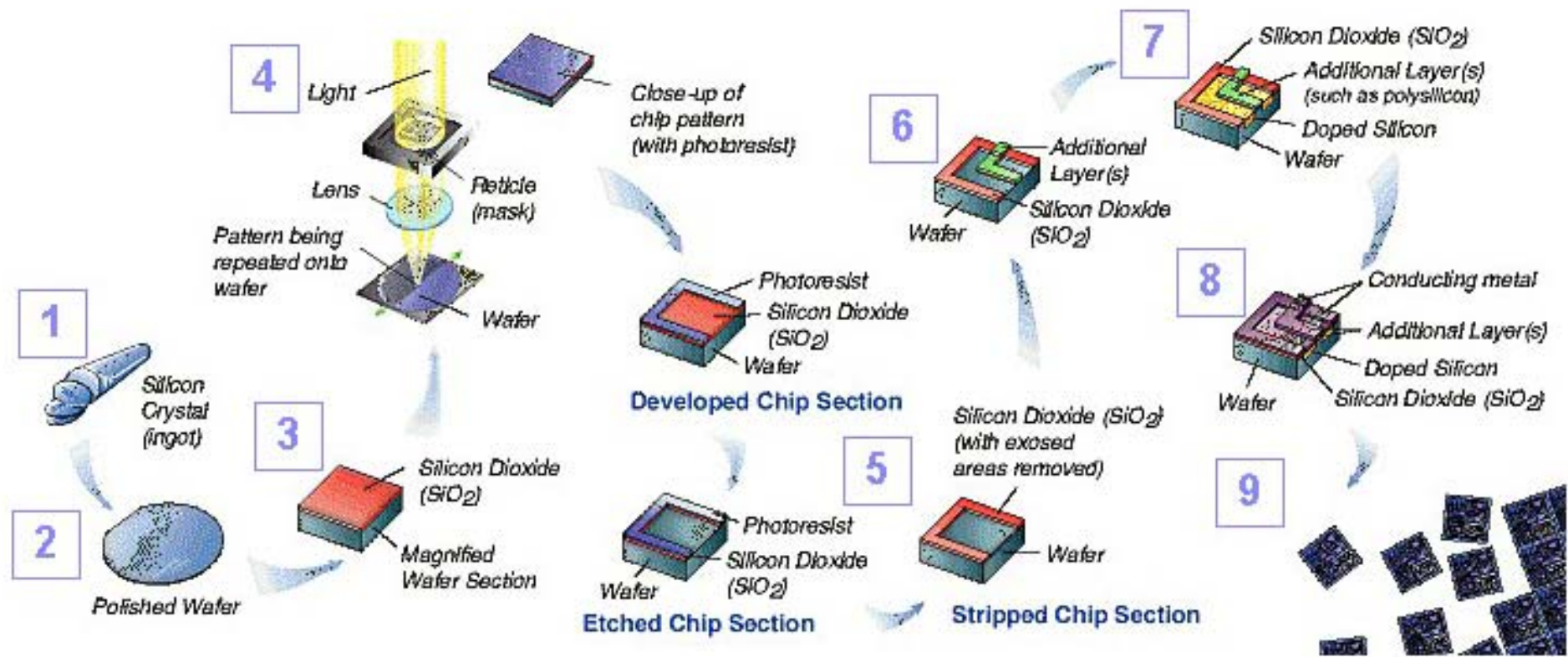


- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist



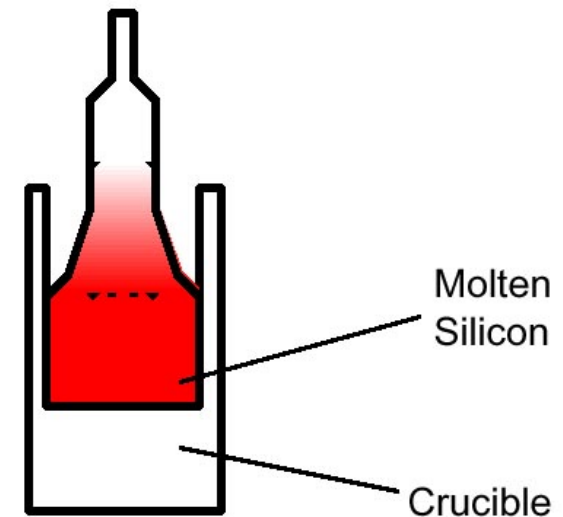
Multiple cycles, 100's STEPS in total

Another Overview of Semiconductor Processing

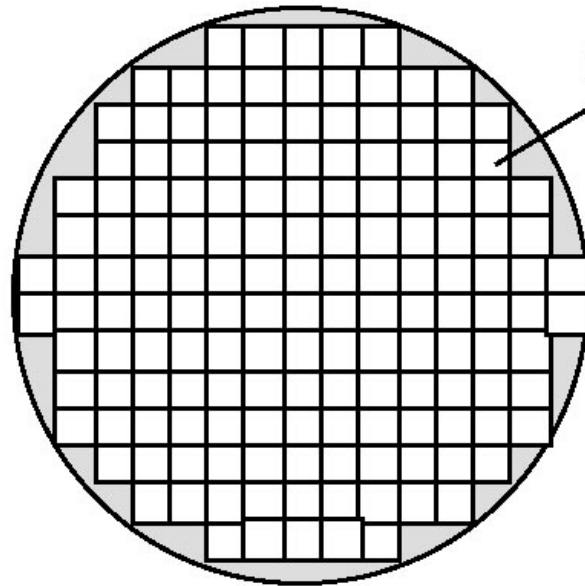
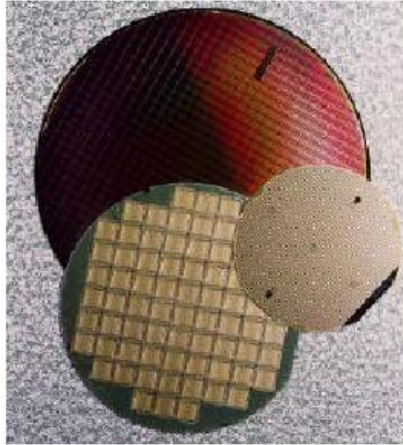


Wafer Processing – Czochralski Method

- Start with crucible of molten silicon ($\approx 1425^{\circ}\text{C}$)
- Insert crystal **seed** in melt
- Slowly rotate/raise seed to form single crystal **boule**
- After cooling, slice boule into **wafers** & polish



Wafer Structure



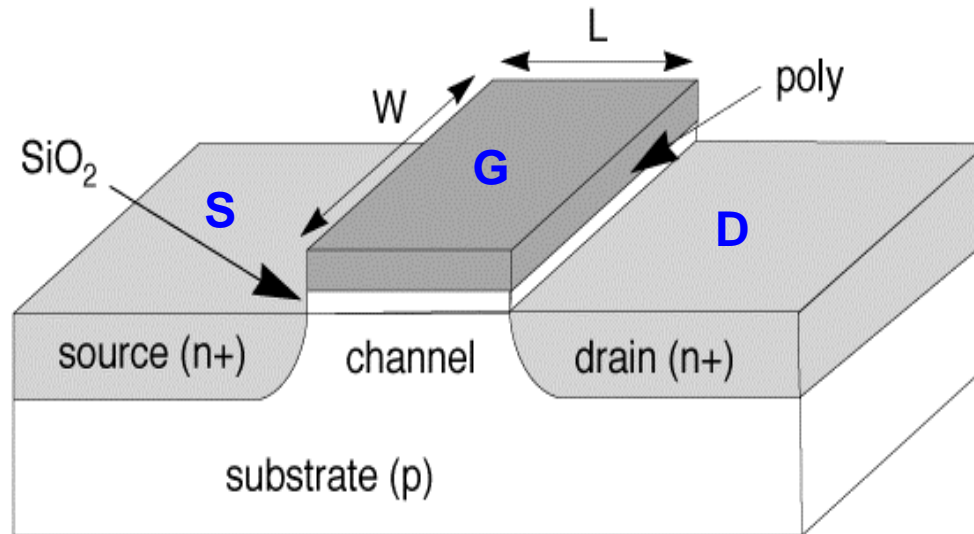
Die - Single IC chip



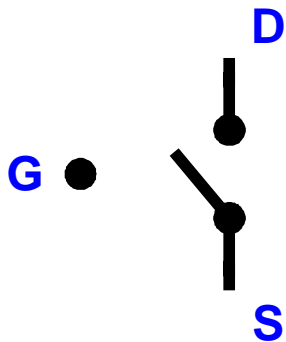
**300 mm
wafer
(sematech)**

CMOS Process Outline

MOS Transistor



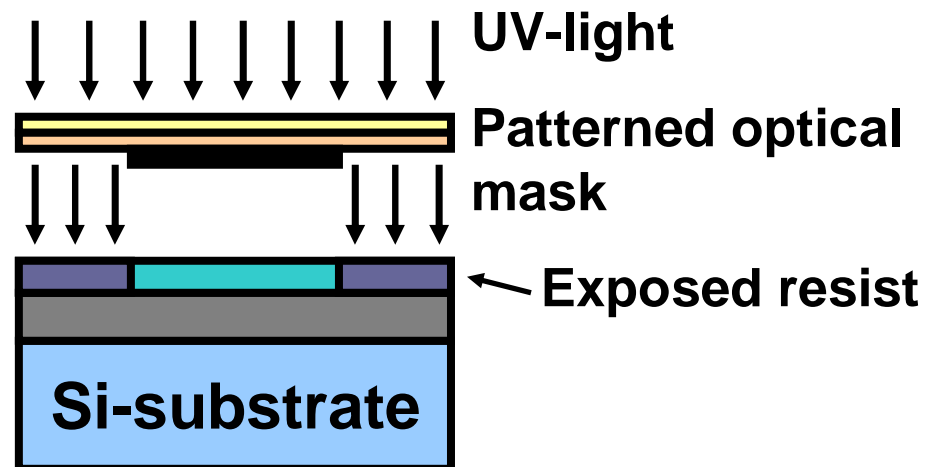
Position of switch depends on gate to source voltage



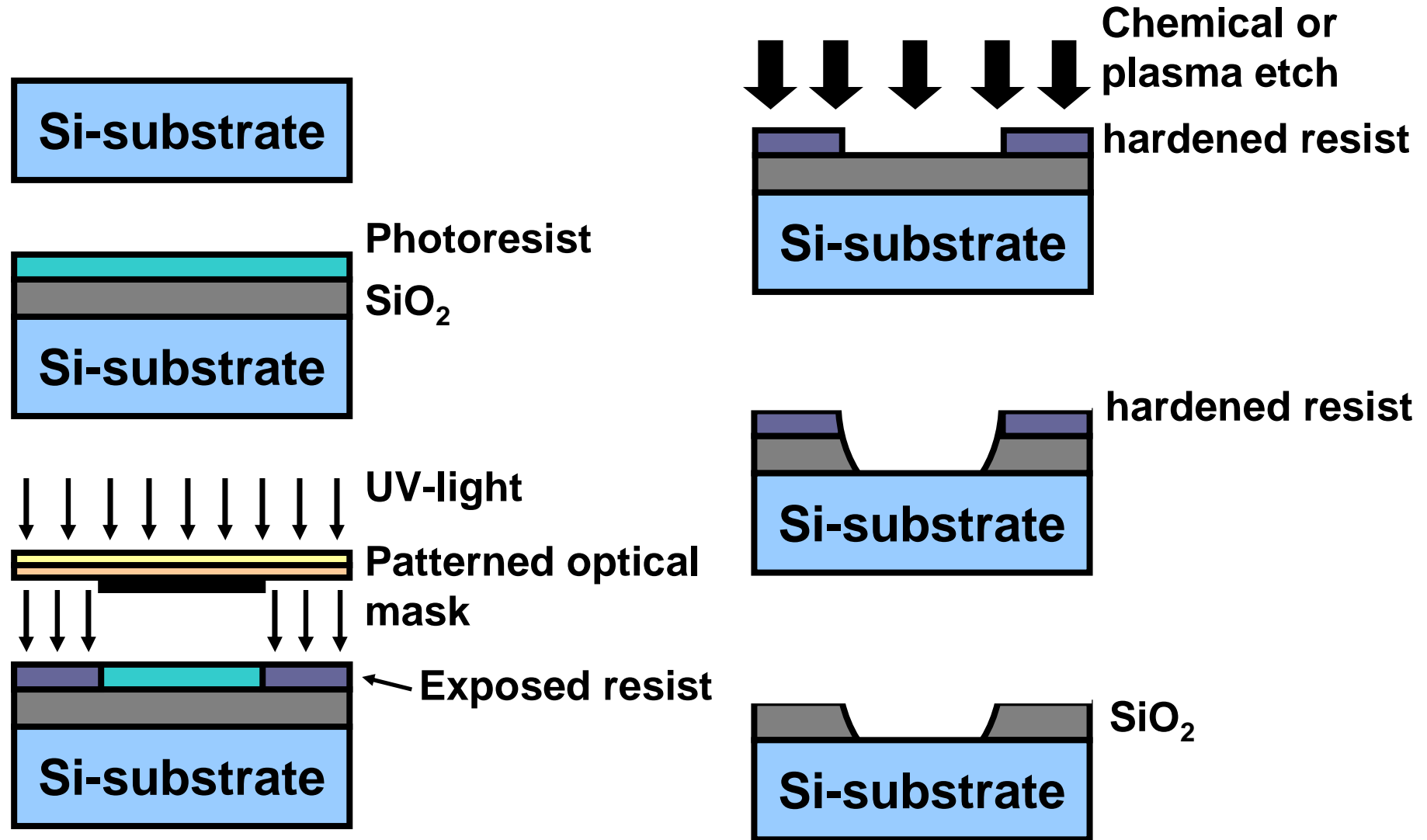
V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

How Patterns on a Chip are Created

- **Basic Principle: Photolithography**
 - Like **projecting an image** through a photographic negative (or positive)
- Coat wafer with **Photoresist**
- **Shine UV light** through glass mask
- **Develop:** dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")



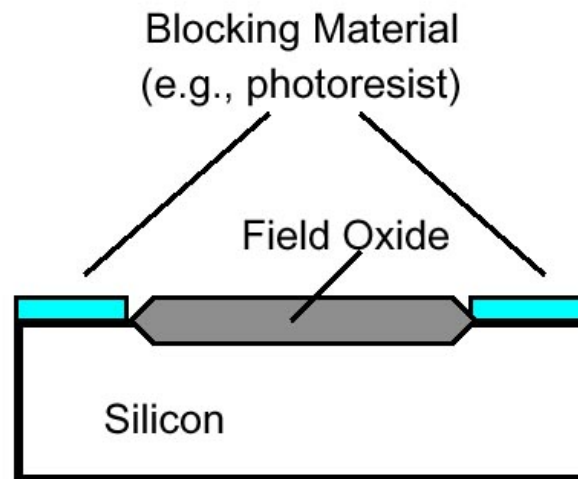
Example: Etching Step, opening of SiO₂



Etching is for removal of material, similar masking principles for deposition (adding of material)

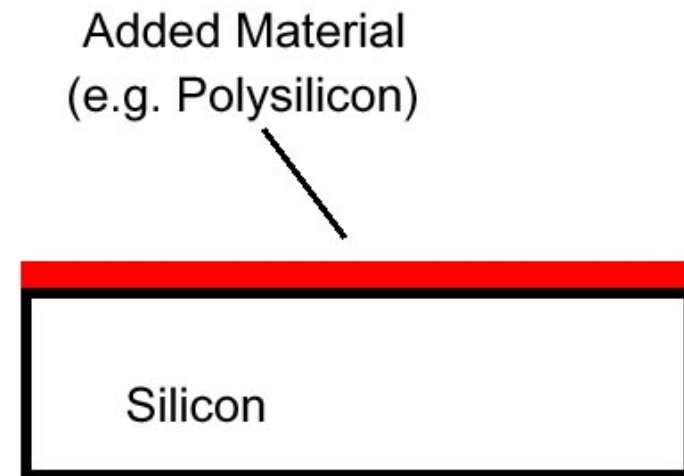
Oxidation

- **SiO₂ formed by oxidation**
 - **Wet oxidation: heat with water (900°C - 1200 °C)**
 - **Dry oxidation: heat with pure oxygen (1200 °C)**
- **Oxide occupies more volume**
- **Alternative: deposition**



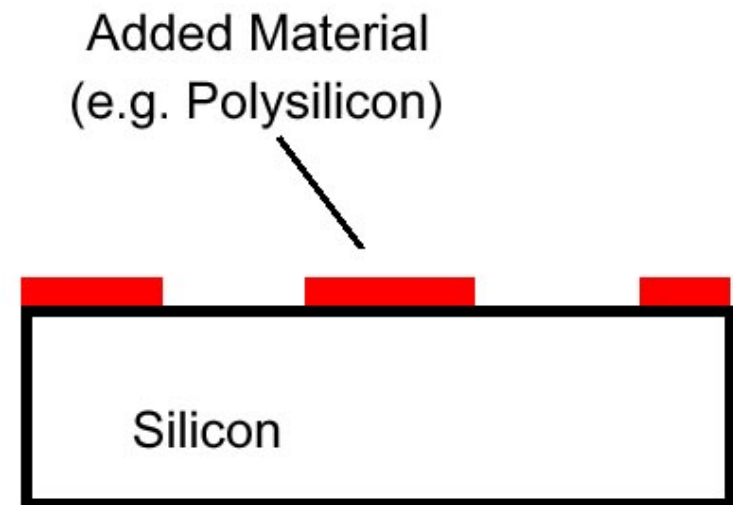
Adding Materials

- **Add materials on top of silicon**
 - **Polysilicon**
 - **Metal**
 - **SiO₂**
- **Methods**
 - **Vapor deposition**
 - **Sputtering (Metal ions)**



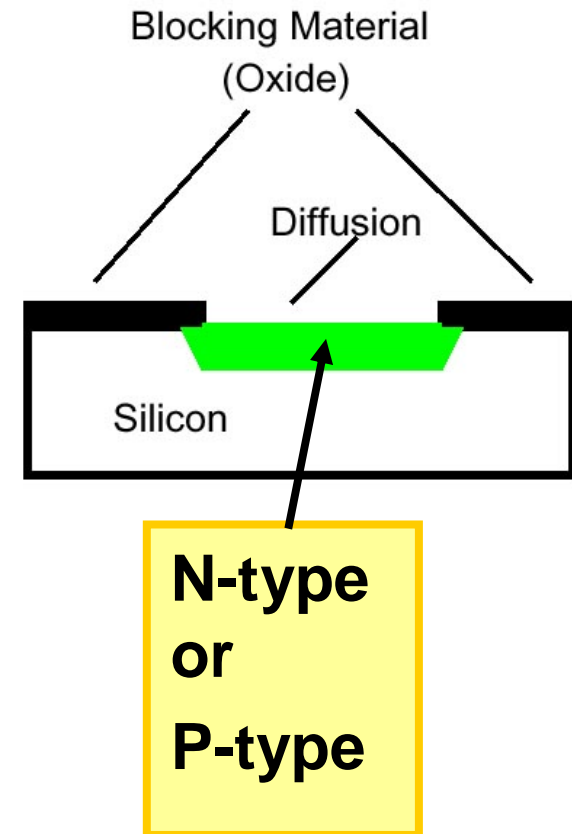
Patterning Added Materials

- Add material to wafer
- Coat with photoresist
- Selectively remove photo resist (PR), after exposure through mask
- Remove unprotected (by PR) material
- Remove remaining PR



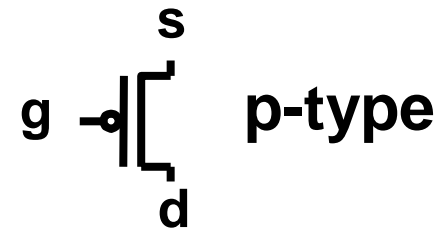
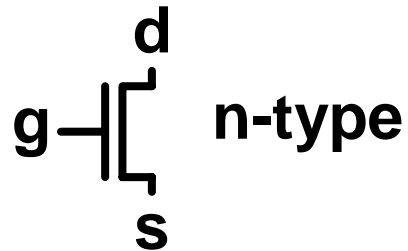
Diffusion

- **Modify electrical properties of Si:**
 - **N-type** (extra electrons)
 - **or p-type**
(fewer electrons \Leftrightarrow extra holes)
- Introduce **dopant** via epitaxy or ion implant e.g. Arsenic (N), Boron (P)
- Allow dopants to **diffuse**
- Block diffusion in selective areas using oxide or PR (photo-resist)
- Diffusion spreads both vertically, horizontally



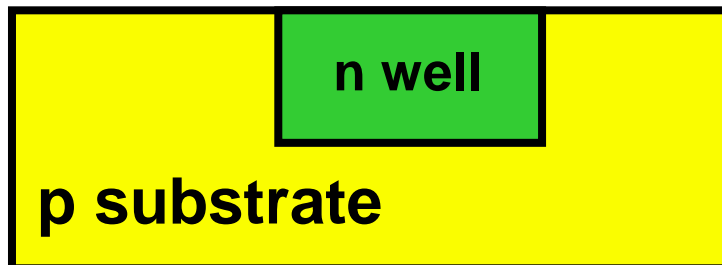
CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



- “on” when V_g is high
- With **n-type s/d**
- **Electrons (n)** as carrier
- Built in **p-type Si**

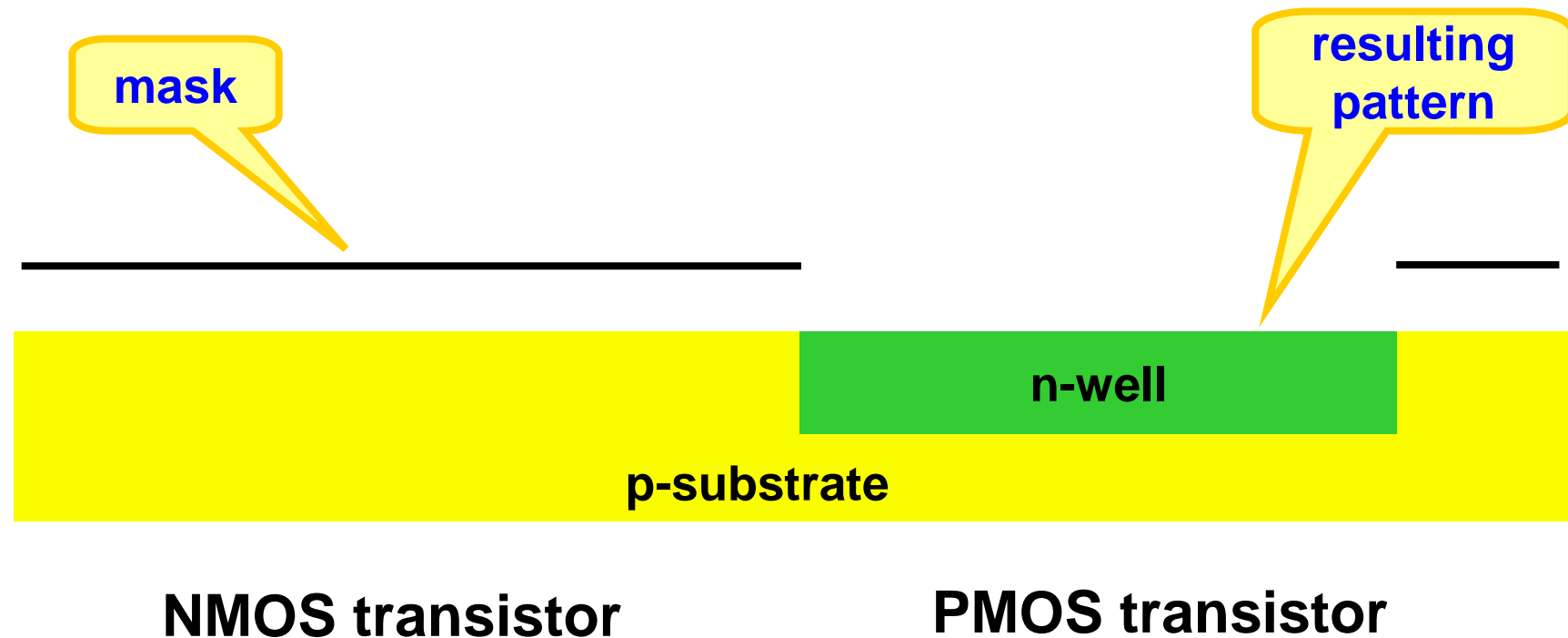
- “on” when V_g is low
- With **p-type s/d**
- **Holes (p)** as carrier
- Built in **n-type Si**



n-well (for PMOS) in p-type substrate (for NMOS)

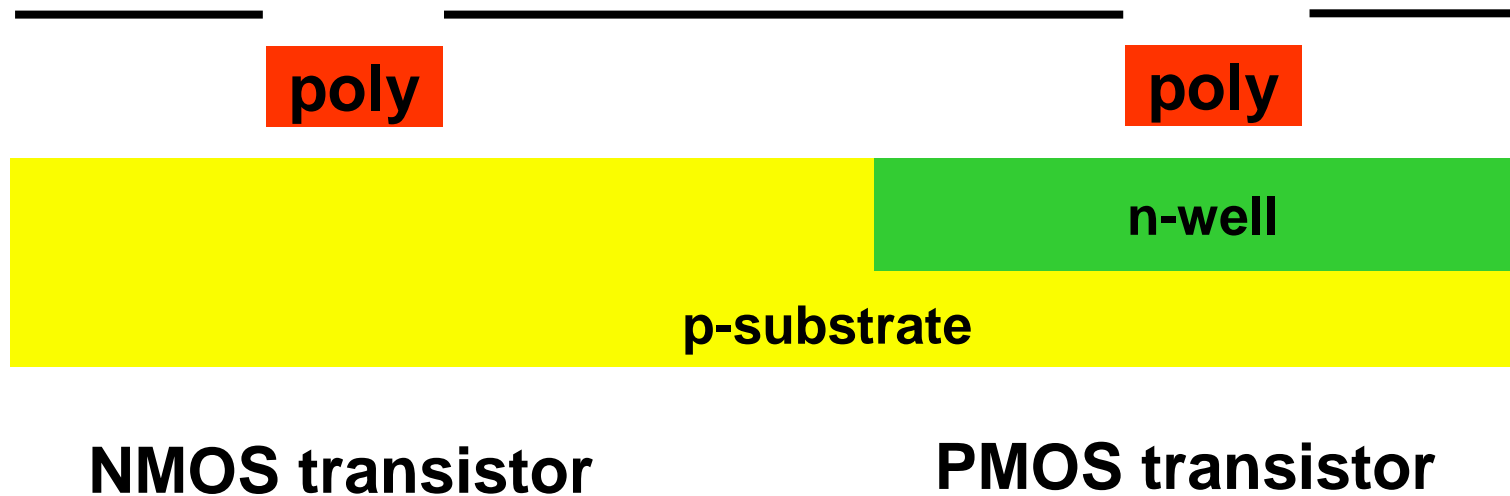
Simplified Outline of Process Flow

Place **n-well** to provide properly-doped substrate for n-type, p-type transistors :



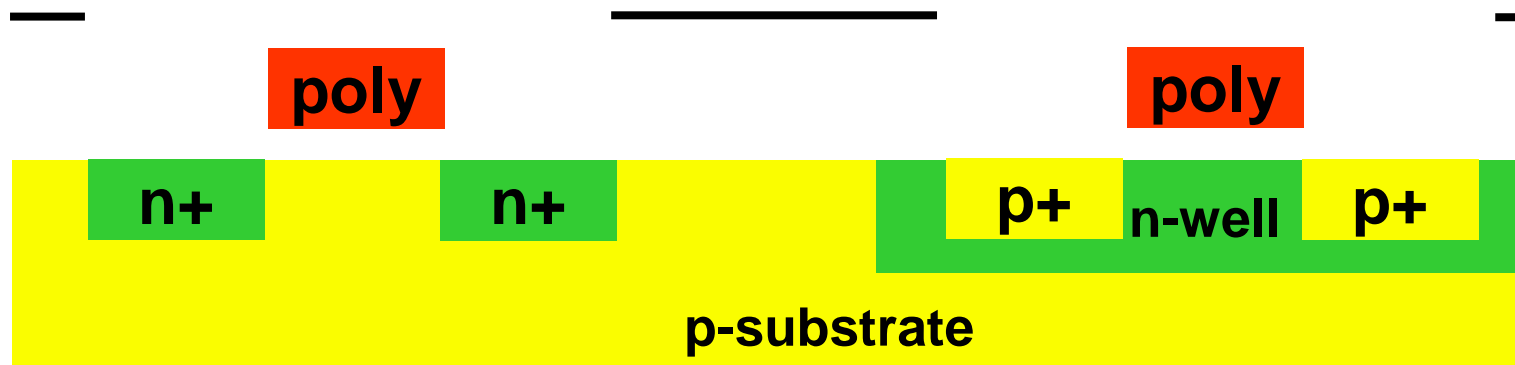
Outline of Process Flow, cont'd

Pattern **gate** next, to later act as a mask for source and drain diffusions:



Outline of Process Flow, cont'd

Add **s/d diffusions**,
with self-masking by poly gate:



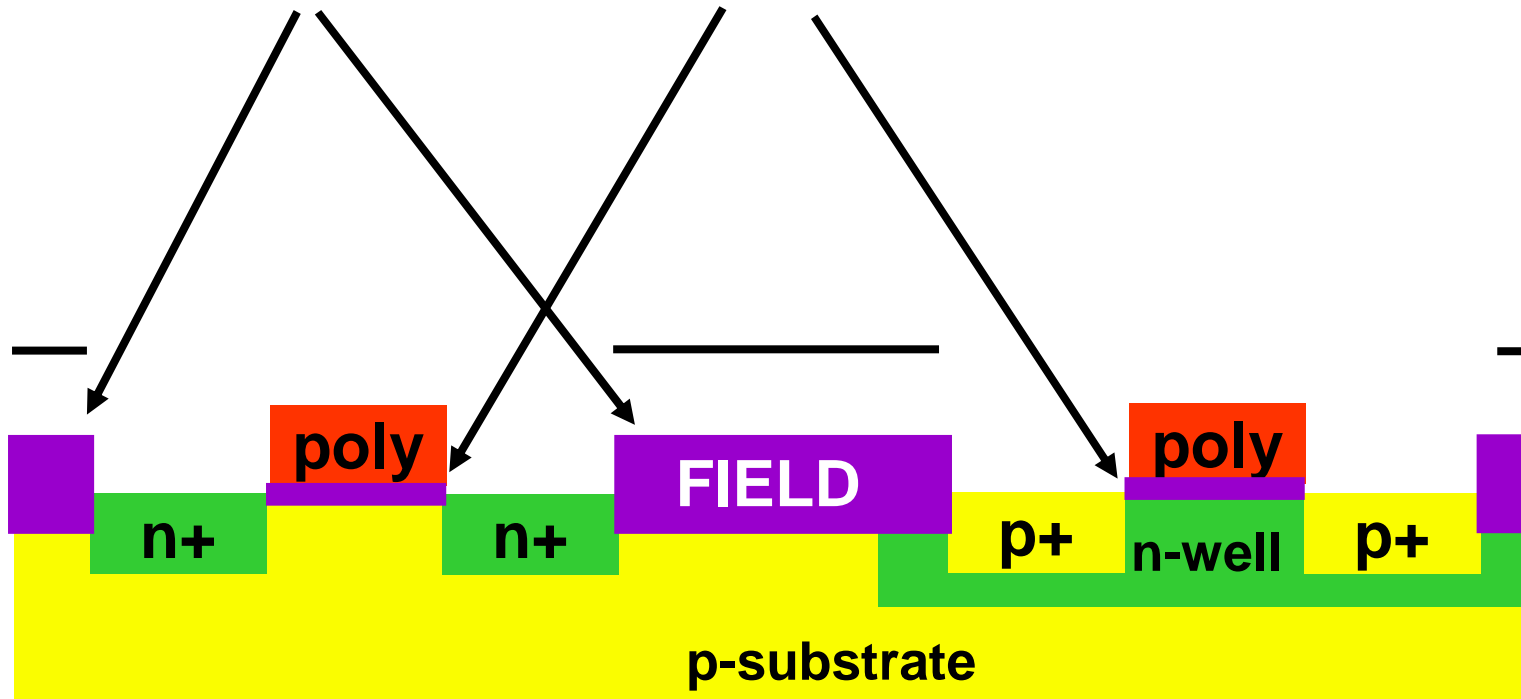
NMOS transistor

PMOS transistor

**Self-masking: Poly also works as a mask,
ensuring good alignment of s/d to gate**

Outline of Process Flow, cont'd

With Field Oxide and Gate Oxide shown



NMOS transistor

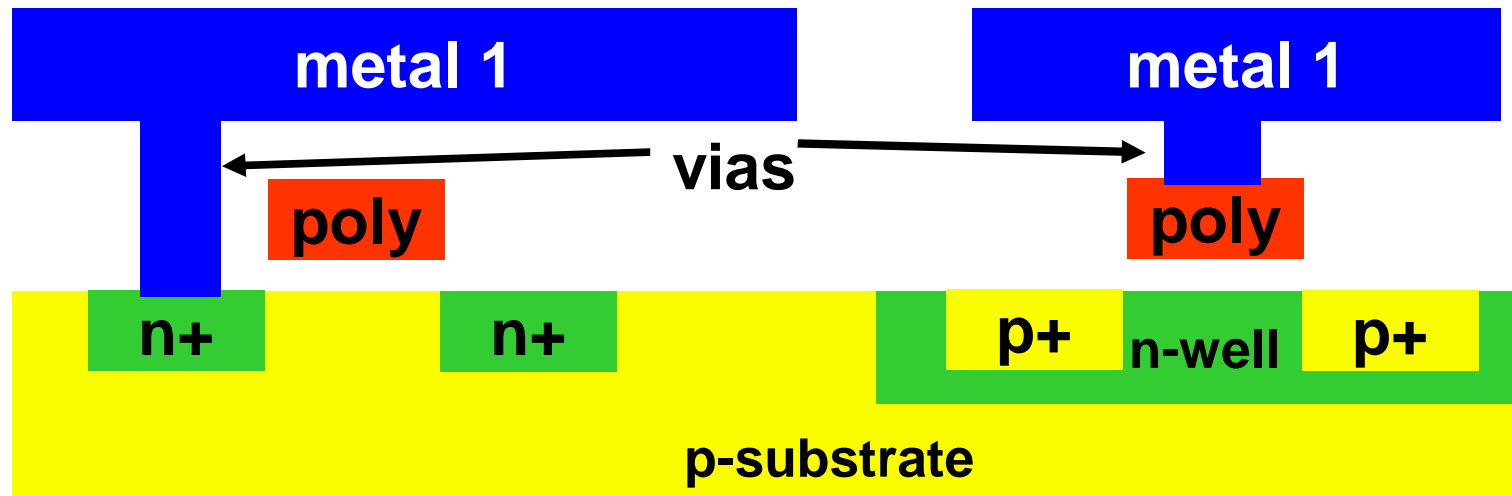
PMOS transistor

**Self-masking: Poly also works as a mask,
ensuring good alignment of s/d to gate**

Outline of Process Flow, cont'd

Start adding **metal layers**:

Via: contact hole between metal layers



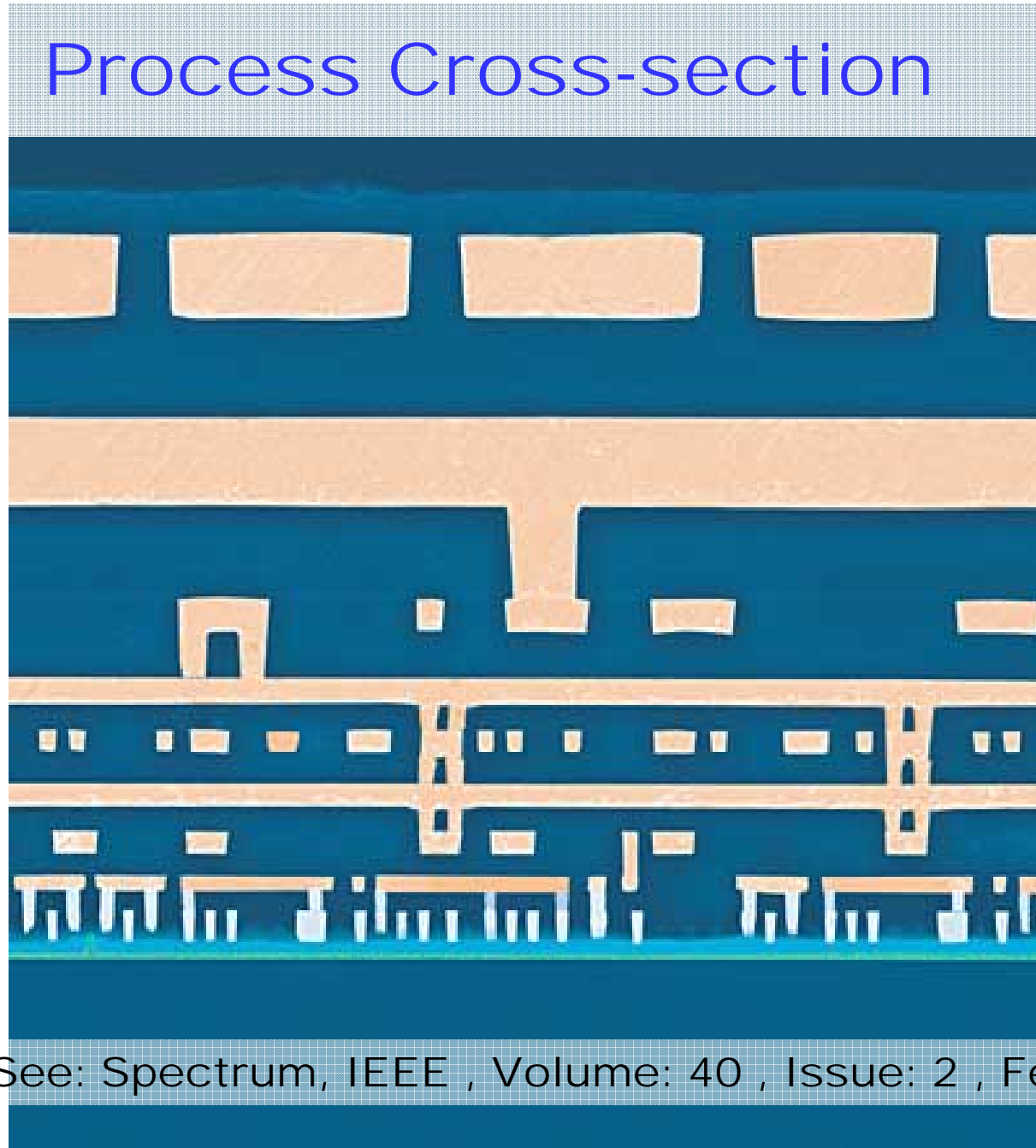
NMOS transistor

PMOS transistor

Similar for subsequent metal layers

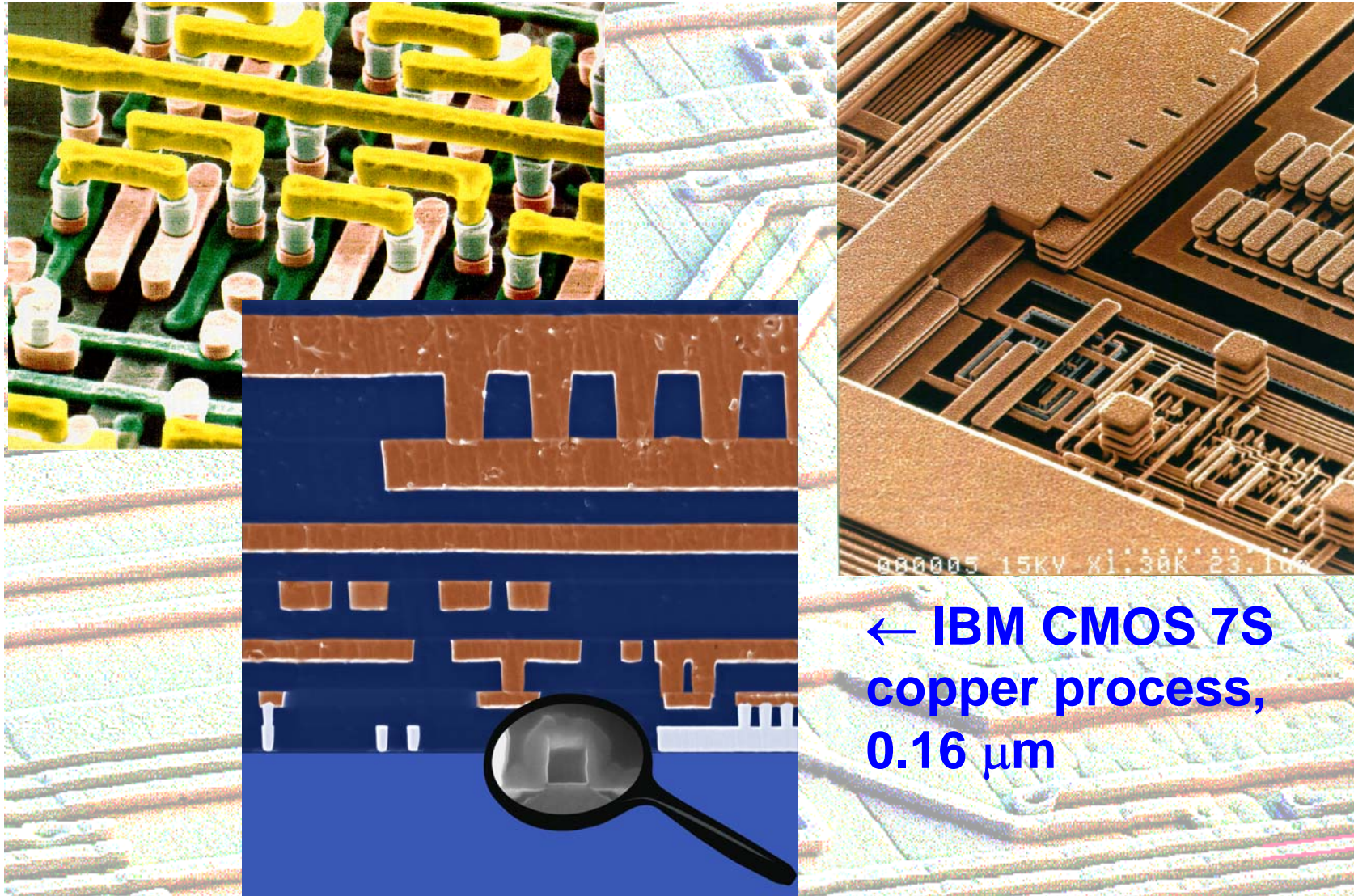
Process Cross-section

8 metal layers
poly (gate) layer



See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

Interconnect Examples (motorola, ibm)

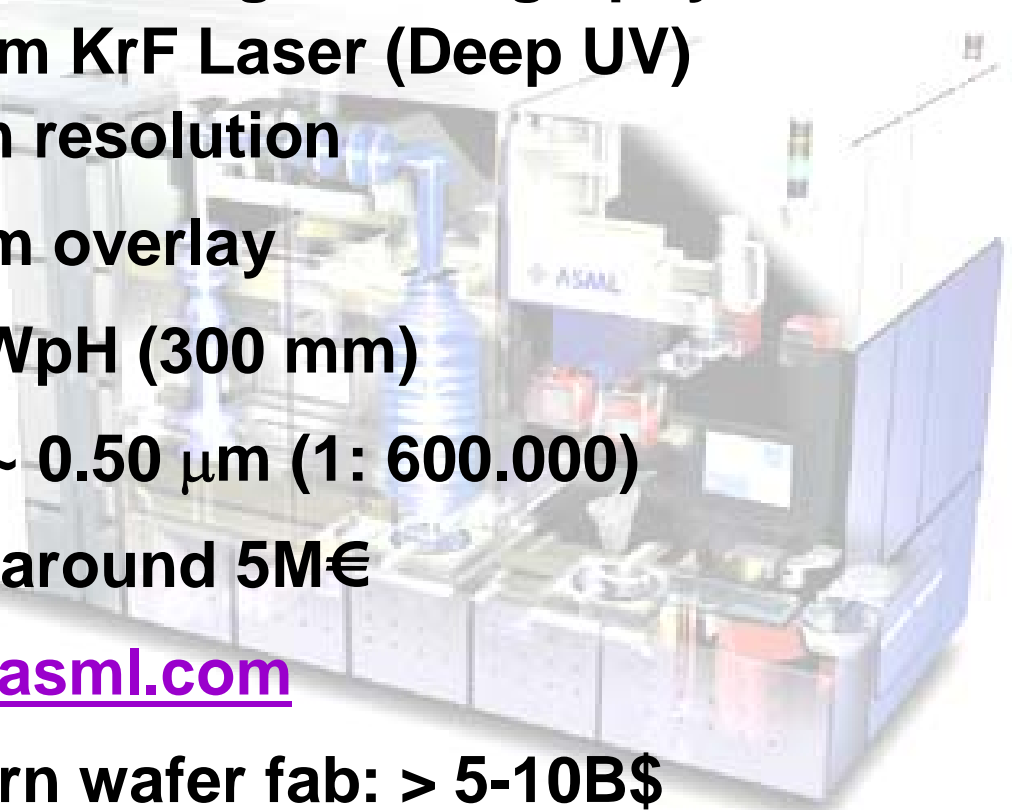


IC Recipe Precisely Fixed

- Process conditions (temperature, time, concentration, ...) **very critical**
- Many **strong compatibility** issues of materials and processes
- Very expensive and **difficult to tune**
- Very expensive **equipment** and facilities
- Need **Billions** of turnover for break-even

Complex Lithographic Process

- Example: ASML TWINSCAN™ XT:1250
- Sub wave length Lithography
193 nm KrF Laser (Deep UV)
- 65 nm resolution
- < 8 nm overlay
- > 85 WpH (300 mm)
- DOF ~ 0.50 μm (1: 600.000)
- price around 5M€
- www.asml.com
- Modern wafer fab: > 5-10B\$



Compare Stepper Wafer Size and Resolution to NL scale

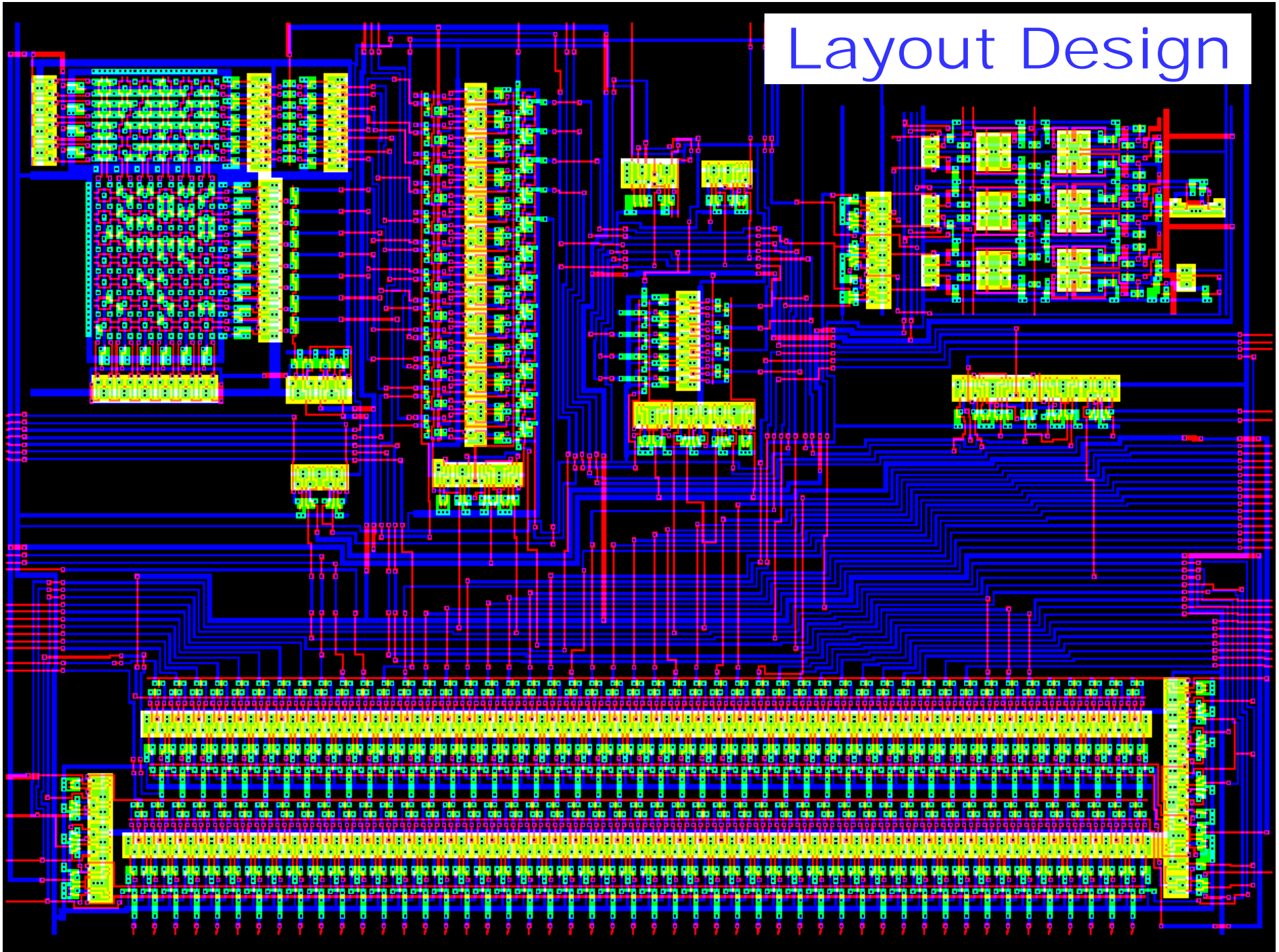
- Wafer size: \varnothing 300mm
- Resolution: 45nm
- Netherlands: 40.000 km² ~ 200km x 200km

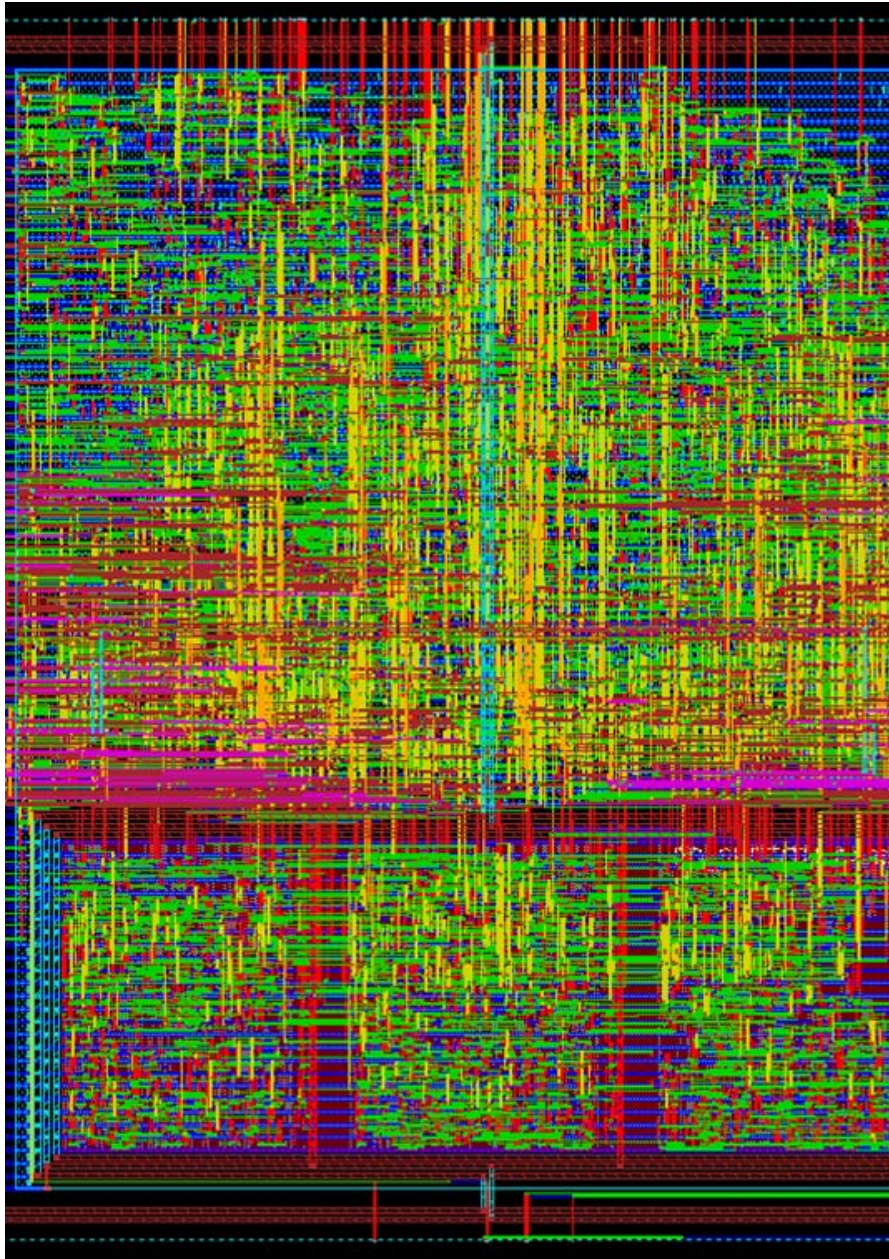
300mm	1	45nm
200km	667x10 ³	3cm

A 'magnified' waferstepper could 'print' the Netherlands with a resolution of 3 cm in 42 sec.

Equivalent to a 44 terabit camera (6.7x6.7 Mega pixel)

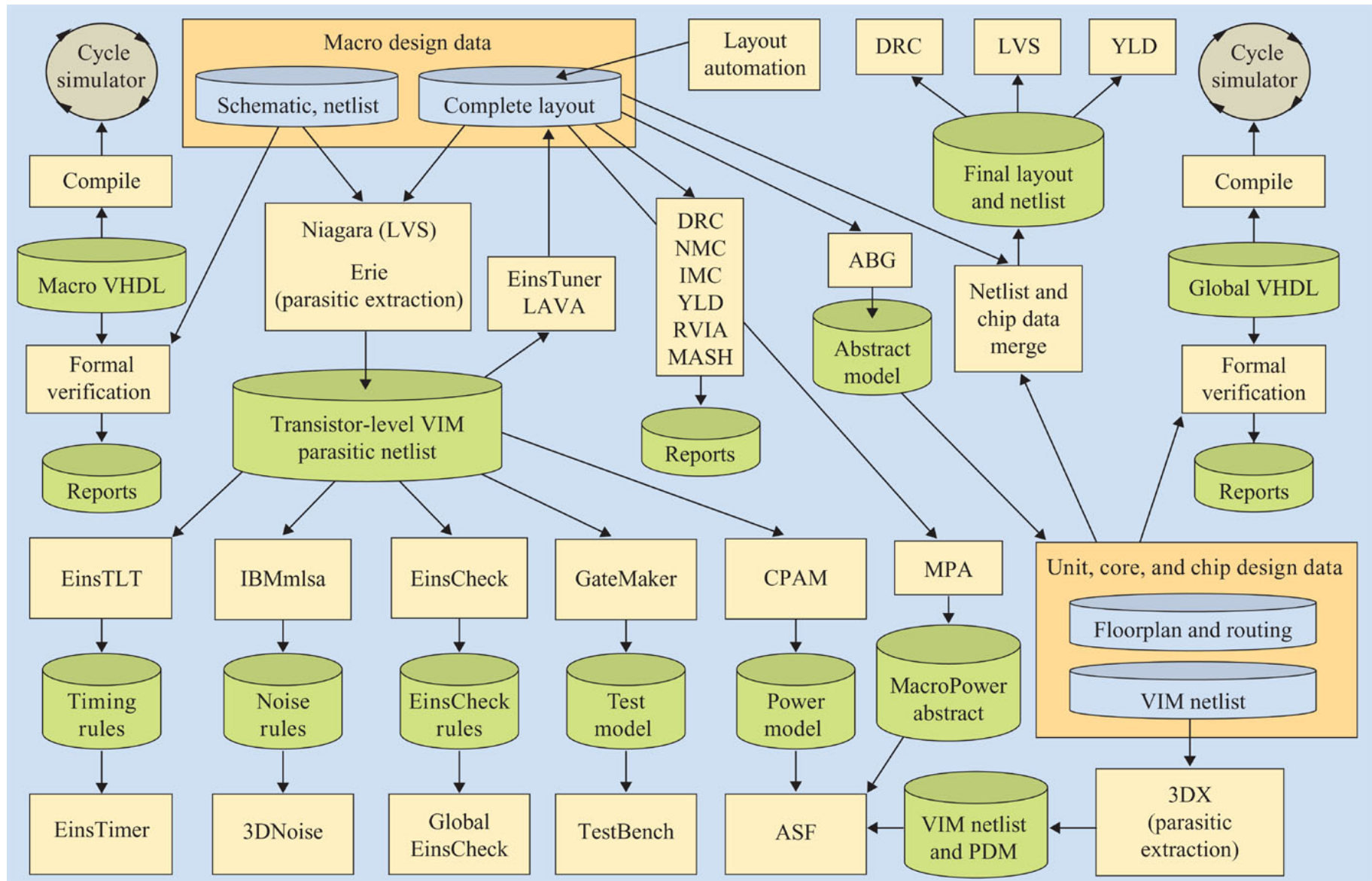
Layout Design





- **Mostly created by software**
- **Chip design software is a difficult to tame beast**
- **But w/o software it is impossible to design a chip**

IBM Power6 Physical Design Flow

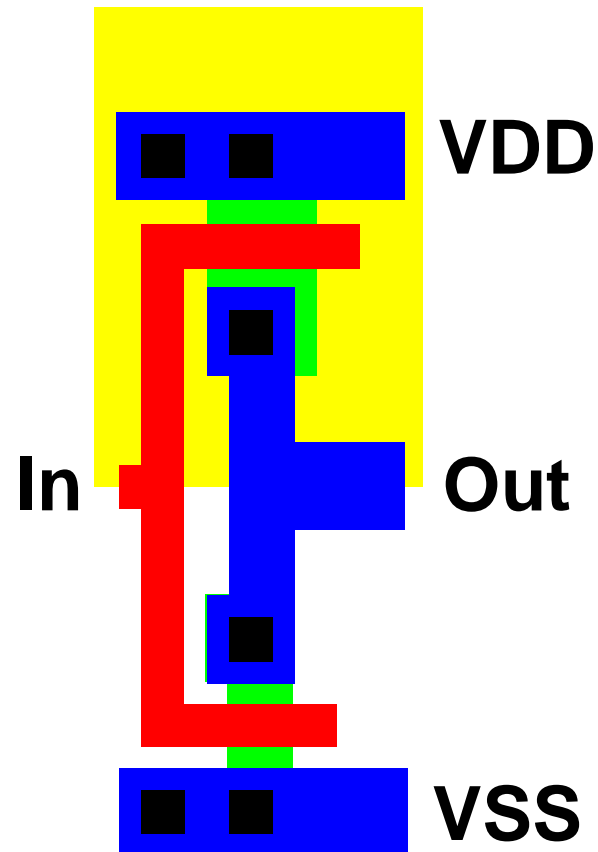


berridge, ibmjrd 2007

Layout Design

Layout Design Concepts

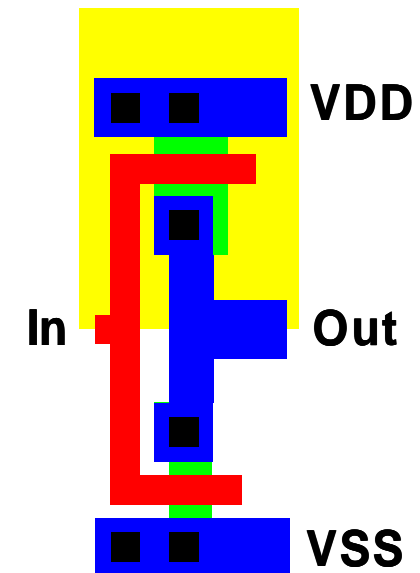
- Layer map
- Layout examples
- Stick diagrams



You should be able to understand such a drawing as well as simpler drawings called 'stick diagram'

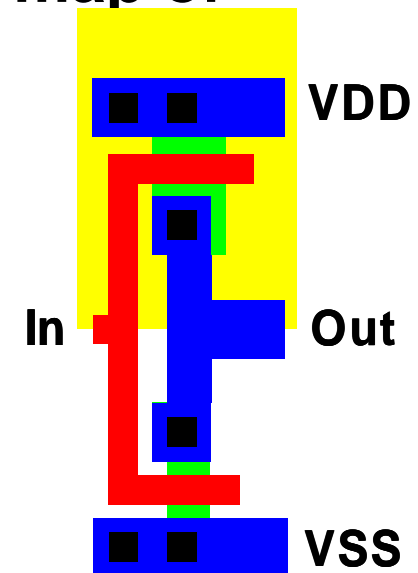
Layout Design

- Layout is design of **fabrication masks**
- Each mask is drawn in **different color**
- Layout is not a free-form drawing
 - Most often: **Manhattan Layout** (rectangular)
 - Sometimes 45-degree angles
 - Curved geometry only for special applications
- Layout should obey **Design Rules**








Layer Map

- **Layers** are assigned **colors** and/or **patterns**, not always 1 to 1
- Is a matter of **convention**
- **Site-dependent, process dependent, tool dependent**
- Be prepared to **reverse-engineer** layer map of **unknown layouts**



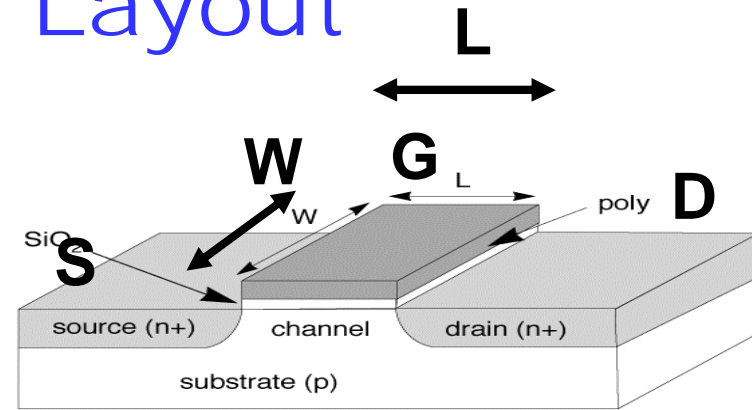
Our Reduced CMOS Layer Map

yellow		nwell – place for P-transistors
green		active – source and drain regions
red		polysilicon – gate material
blue		metal 1 – first interconnect metal
black		contact, via – hole in interlayer oxide

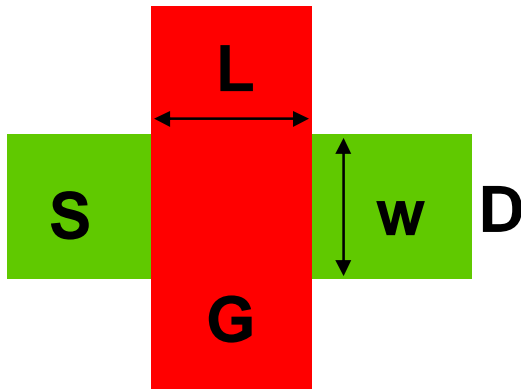
- Our layouts will be composed of these colors
- Or equivalent B/W patterns
- Compare to / instead of color plate 1
- **Note:** active = active area = diff = diffusion, well \approx tub

Transistor Layout

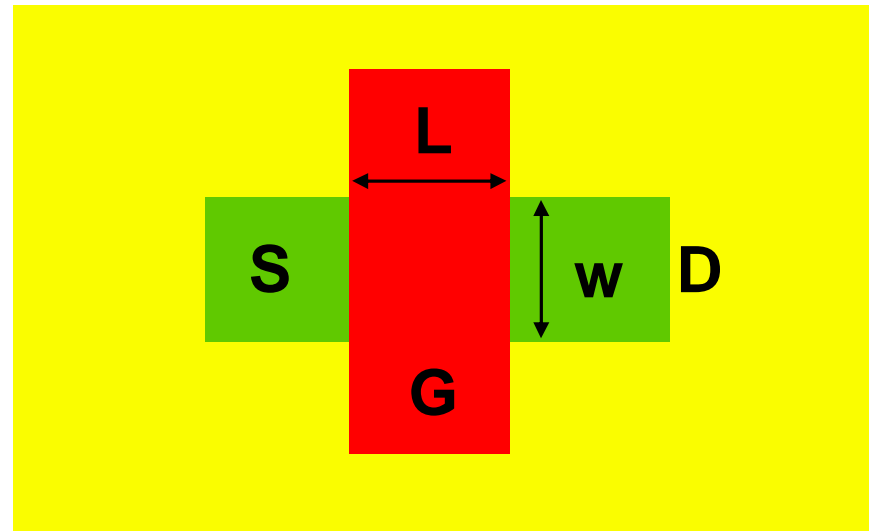
n-well (p-sub)



n-type

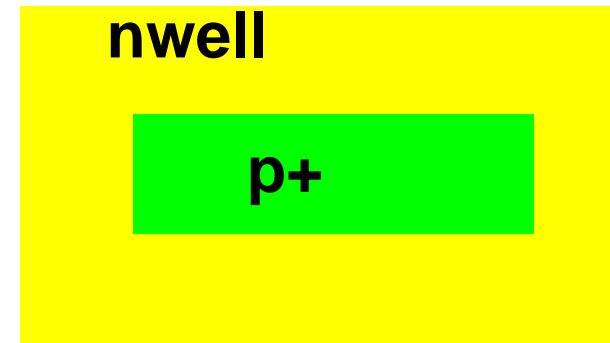


p-type

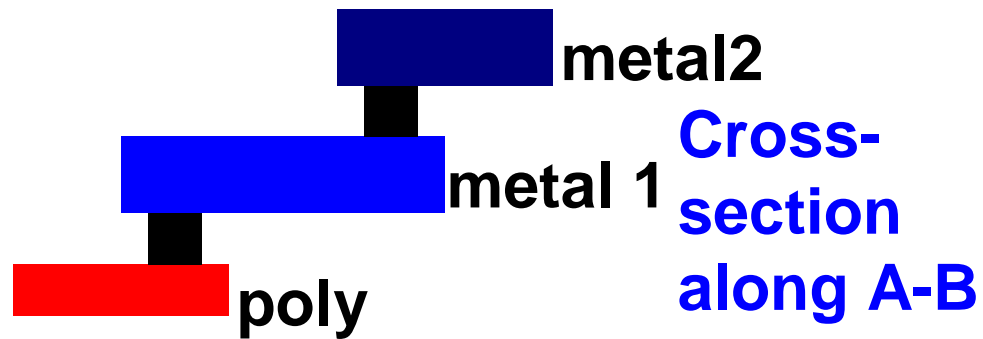
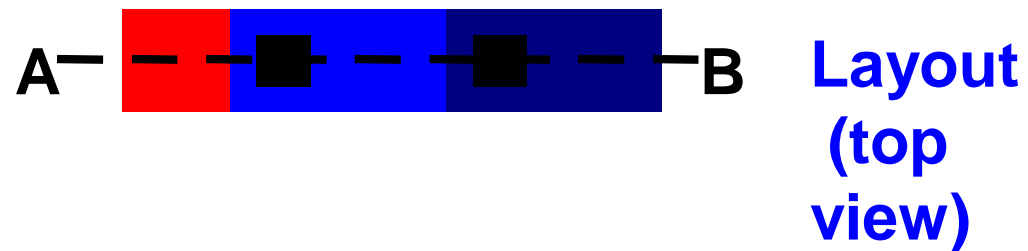
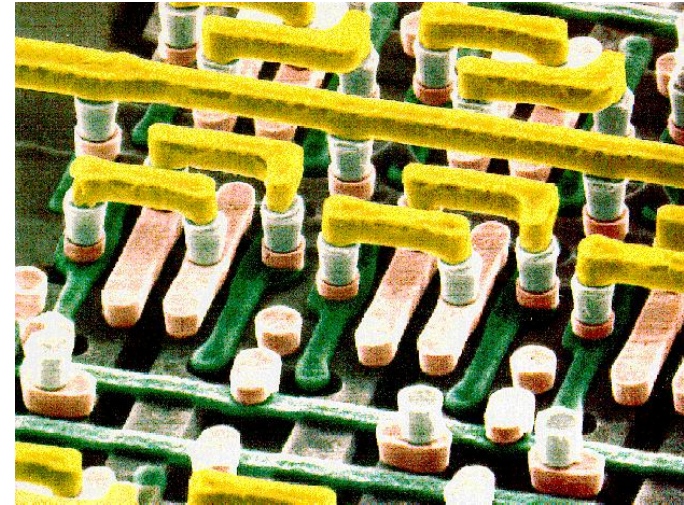


Polarity of Active Area

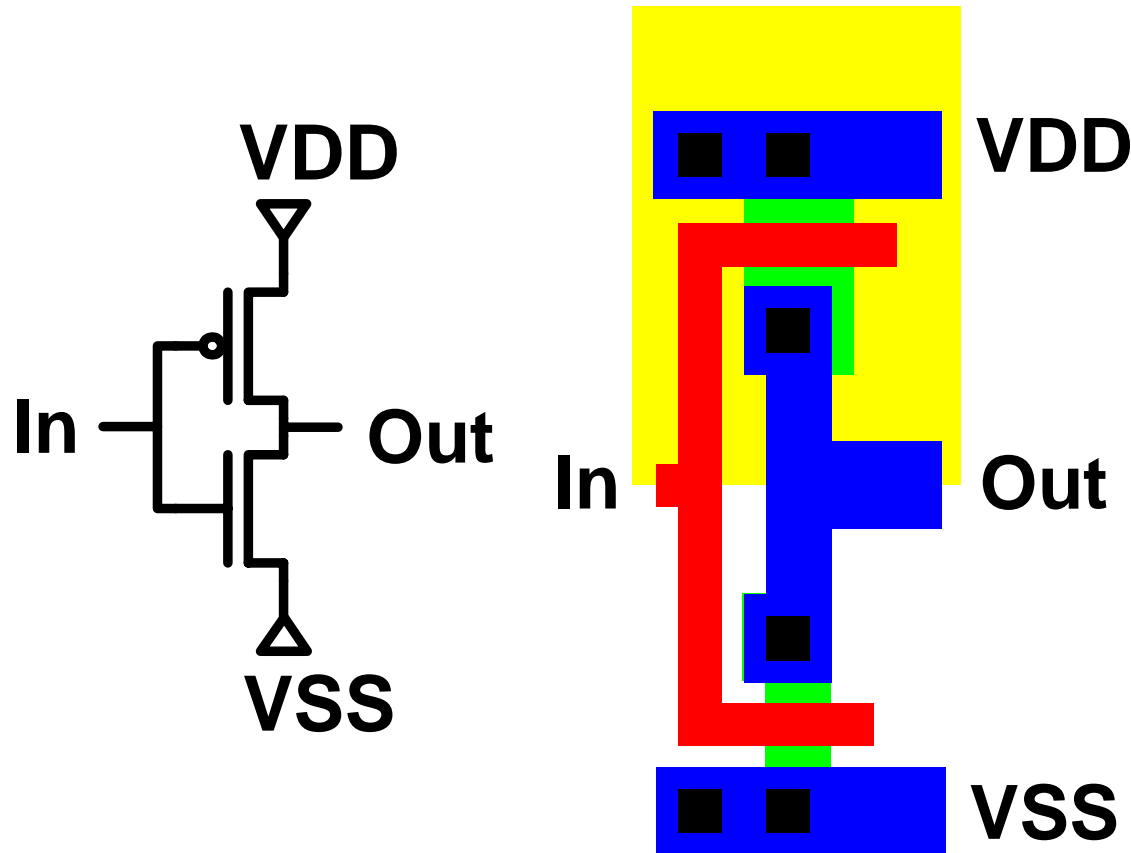
- **Active layer** or active area is the source/drain implant layer (area). Usually abbreviated as '**active**' only.
- Normally, a so-called **select** mask determines polarity of **active**
- See color plate 5
- We will implicitly define polarity of **active** by **n-well**
- Or we will even omit the **nwell** and use the context



Contact Holes and Vias



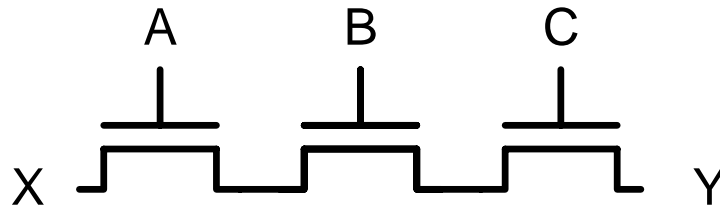
Inverter Layout



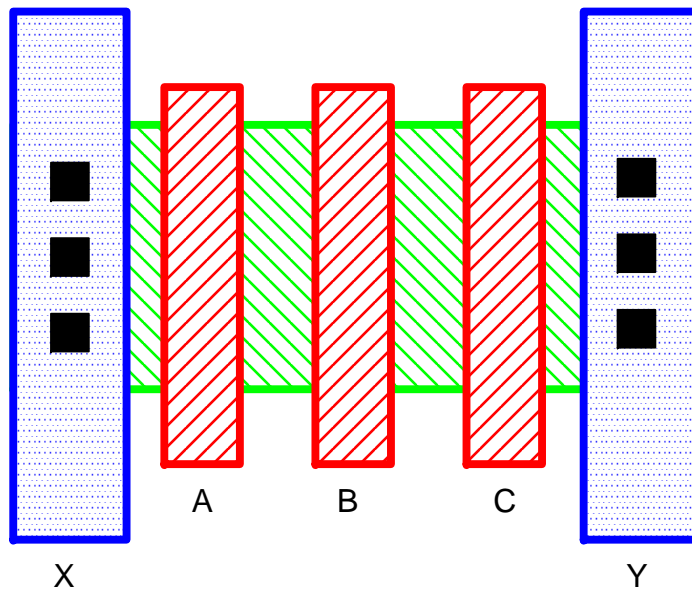
Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

Given such a layout, you should be able to draw the circuit on the left, as well as the different cross-sections

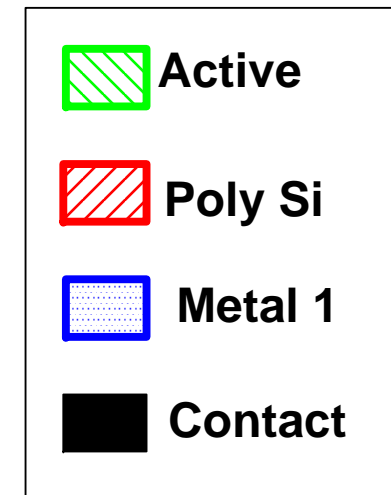
From Schematic to Layout



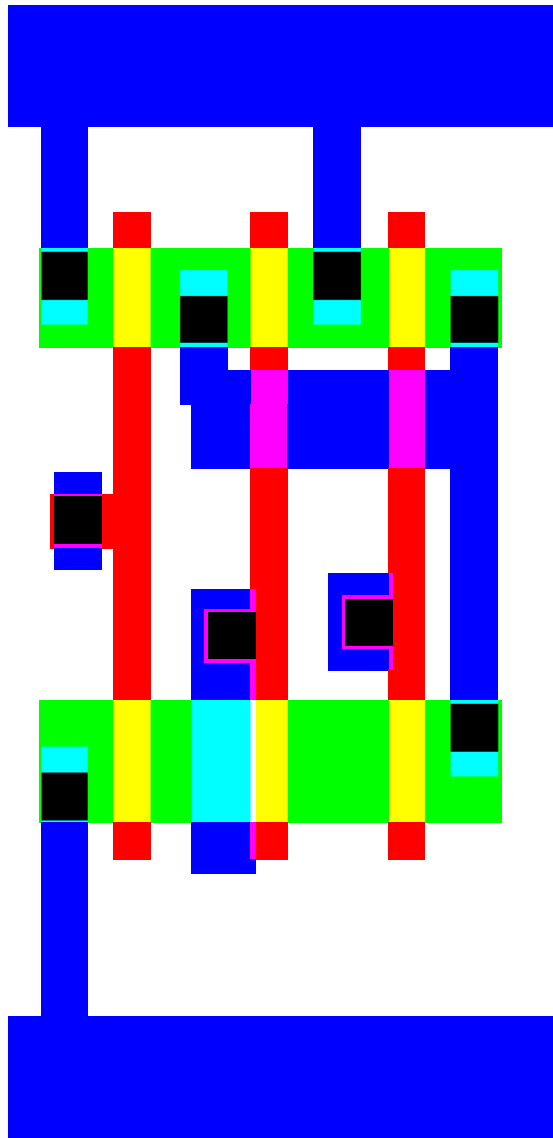
Transistor schematic



Layout



NAND3_X1 (45nm)



**Standard cell:
Fixed pitch and width of VDD
and VSS traces**

Exercise

Zie onderstaande lay-out van een transistor.

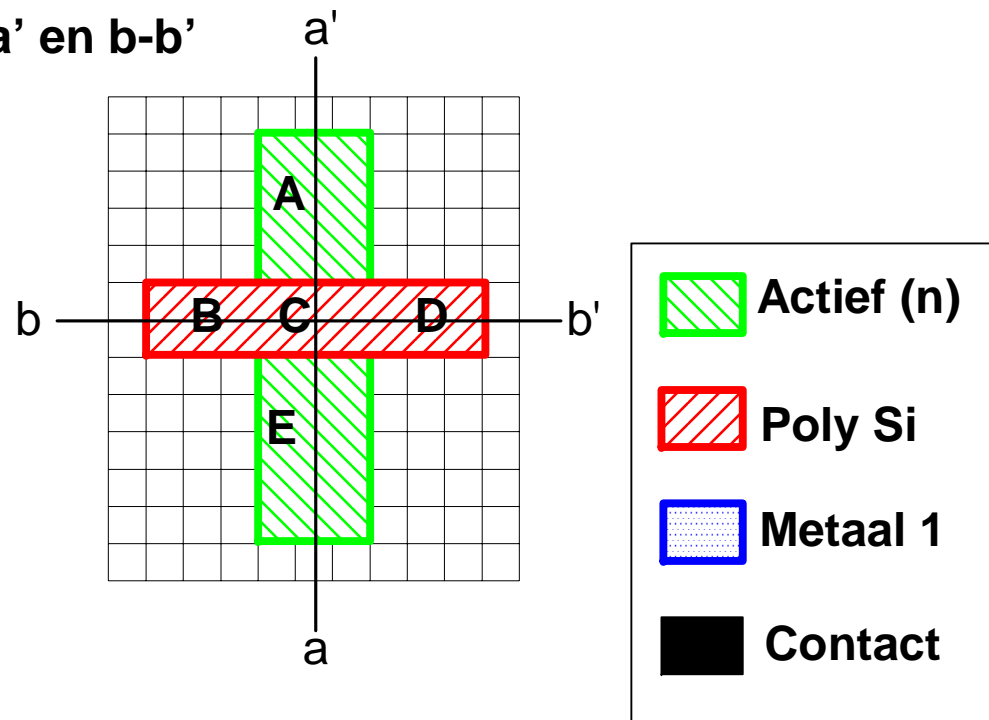
Geef voor ieder van de aansluitingen gate, source, drain aan uit welke letters A-E (zie de layout) het gebied bestaat.

G:

S:

D:

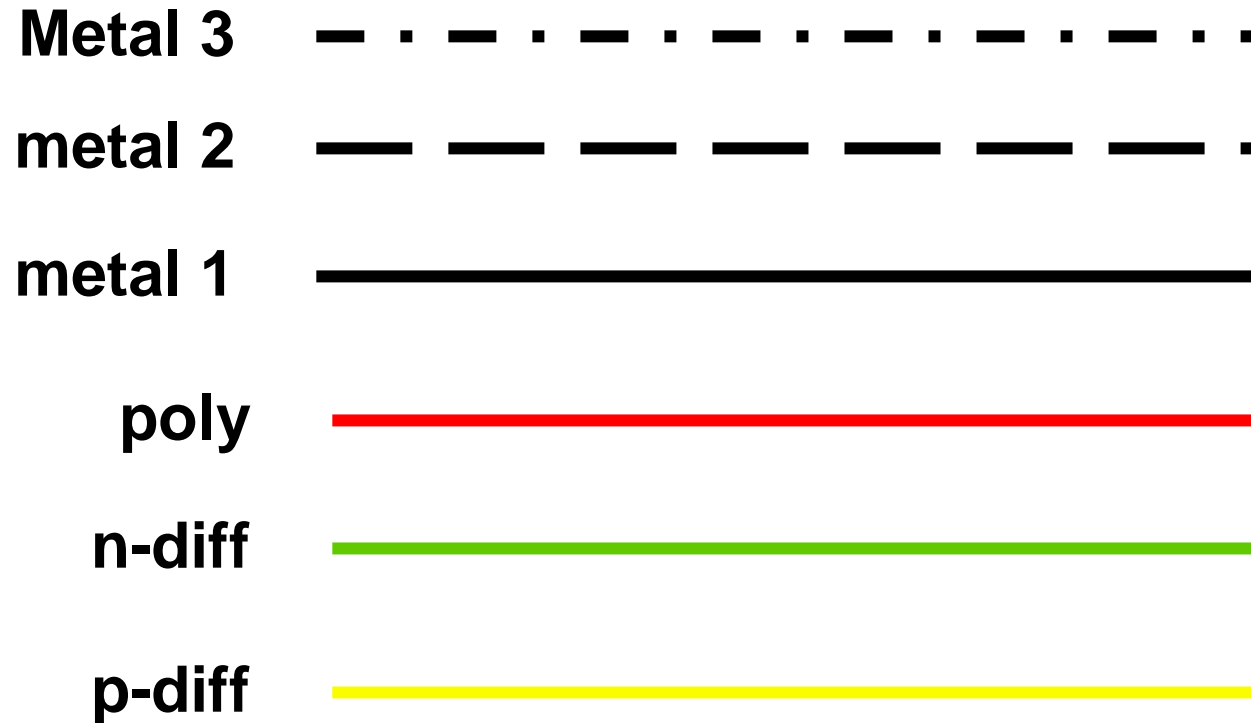
Teken een doorsnede langs a-a' en b-b'



Stick diagrams

- A stick diagram is a **cartoon** of a layout.
- Does show components/vias but only **relative placement**.
- Does **not** show **exact placement**, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.

Stick layers

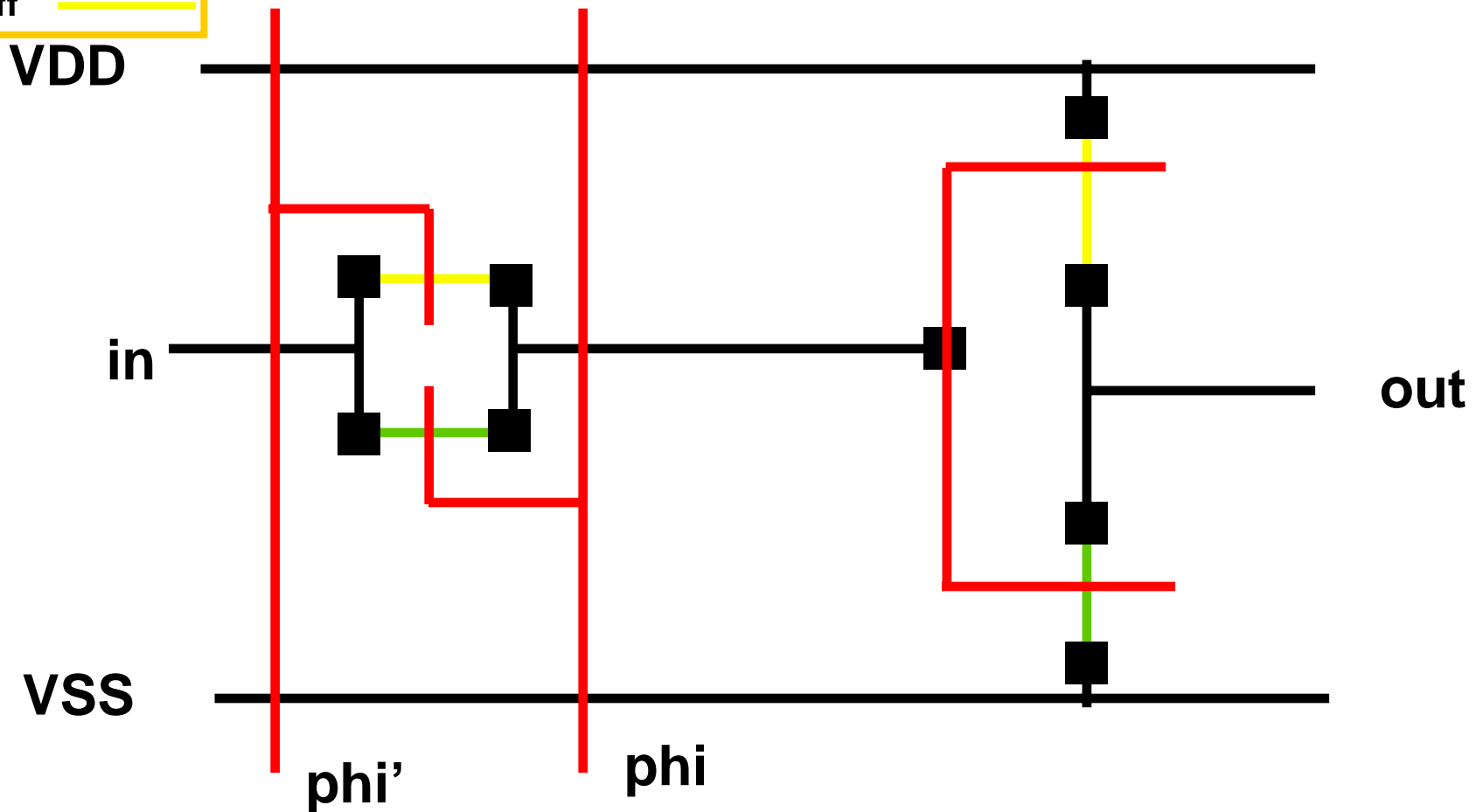


- **Caution: stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff**

Dynamic latch stick diagram

Metal 3	- . - .
metal 2	- - -
metal 1	—
poly	— (red)
n-diff	— (green)
p-diff	— (yellow)

Circuit diagram?

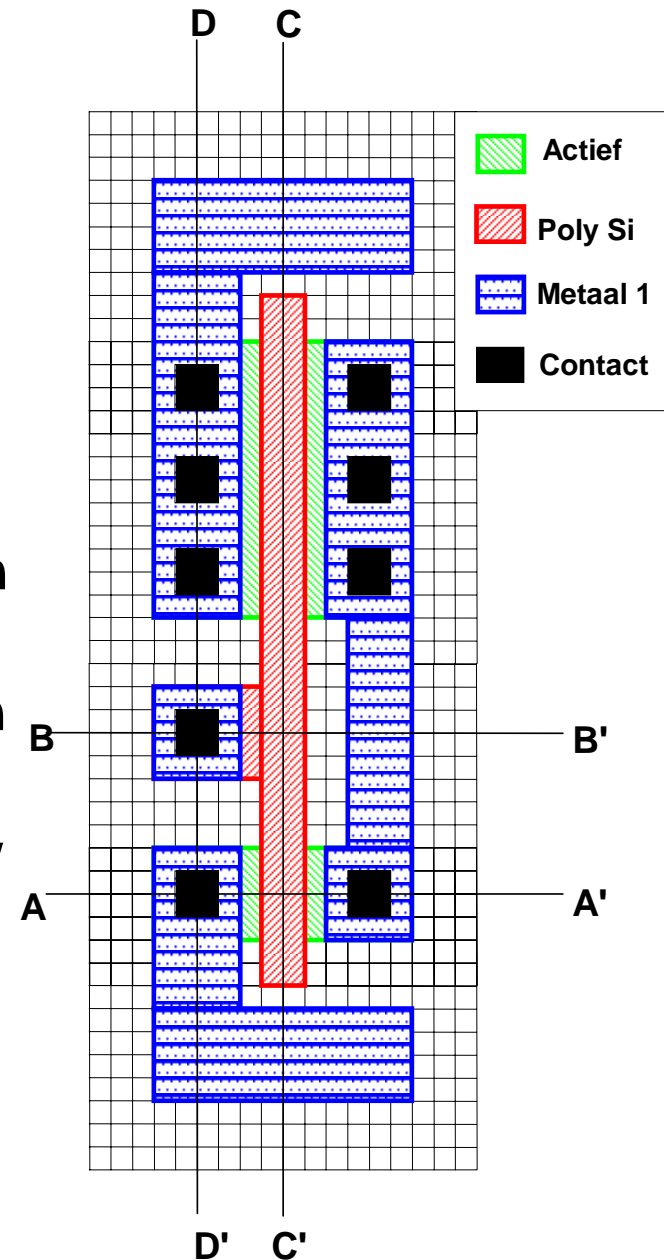


Design Rules

- The fabrication process will suffer from **tolerances**
- Chip features will have a practical **minimum size** to allow them to be fabricated reliably enough (with high enough **yield**)
- This is captured into a set of precise **Design Rules**
- Modern processes have terribly complex set of design rules as a compromise between **flexibility** and **manufacturability**
- We will **ignore** this subject
- But you will have to understand it during **OP** next year.

Zie bijgaande layout van een CMOS inverter

- Teken doorsnedes langs A-A', B-B' en C-C'
- Welke van de twee transistoren is (vermoedelijk) de P-MOS transistor (waarom?)
- Teken voor deze keuze de layout van de N-well.
- Geef in de layout aan waar de Vss en Vdd aansluitingen zitten.
- Teken het transistor schema, met l/w ratio's



Summary

- **CMOS Processing**
 - **Photolithography**
 - **Material Deposition & Removal**
 - **Oxide Growth & Removal**
- **CMOS Process Outline**
- **Layout Design**
 - **Layer map**
 - **Layout examples**
 - **Stick diagrams**
- **Design Rules**
 - **Why we need design rules**