



Module 1: Devices

Diodes, MOS transistors, models

Goal of this chapter

- **Present intuitive understanding of device operation**
- **Introduction of basic device equations**
- **Introduction of models for manual analysis**
- **Introduction of models for SPICE simulation**
- **Analysis of secondary and deep-sub-micron effects**
- **Future trends**

Outline

- **Semiconductor Physics**
- **The diode**
 - **Depletion, I-V relations, capacitance,**
- **The MOS transistor**
 - **First glance, threshold, I-V relations, models**
 - **Dynamic behavior (capacitances), resistances,**
- **Process variations**

Course Material for Devices

Chapter 3

P = primair, I = Illustratie, O = overslaan

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(1) Vervangend studiemateriaal voor dynamisch gedrag in syllabus

Modeling

- An **abstraction** of (the properties) of something to help **understanding** and **predicting** its behavior
- **Domain Specific**: weather, climate, economy, stock market, ...
- Different models for something to **answer different questions**
- **Black-Box** modeling vs. **Physically Based**

- **After Einstein: a model should be as simple as possible, but not simpler**

Semiconductor Physics

- All electrical behavior is determined by underlying physics
- This course is not about the physics
- But some small amount of background information helps built intuition
- Intuition is what an engineer/designer needs most

Periodic System

H ¹																	He ²
Li ³	Be ⁴											B ⁵	C ⁶	N ⁷	O ⁸	F ⁹	Ne ¹⁰
Na ¹¹	Mg ¹²											Al ¹³	Si ¹⁴	P ¹⁵	S ¹⁶	Cl ¹⁷	Ar ¹⁸
K ¹⁹	Ca ²⁰	Sc ²¹	Ti ²²	V ²³	Cr ²⁴	Mn ²⁵	Fe ²⁶	Co ²⁷	Ni ²⁸	Cu ²⁹	Zn ³⁰	Ga ³¹	Ge ³²	As ³³	Se ³⁴	Br ³⁵	Kr ³⁶
Rb ³⁷	Sr ³⁸	Y ³⁹	Zr ⁴⁰	Nb ⁴¹	Mo ⁴²	Tc ⁴³	Ru ⁴⁴	Rh ⁴⁵	Pd ⁴⁶	Ag ⁴⁷	Cd ⁴⁸	In ⁴⁹	Sn ⁵⁰	Sb ⁵¹	Te ⁵²	I ⁵³	Xe ⁵⁴
Cs ⁵⁵	Ba ⁵⁶	La ⁵⁷	Hf ⁷²	Ta ⁷³	W ⁷⁴	Re ⁷⁵	Os ⁷⁶	Ir ⁷⁷	Pt ⁷⁸	Au ⁷⁹	Hg ⁸⁰	Tl ⁸¹	Pb ⁸²	Bi ⁸³	Po ⁸⁴	At ⁸⁵	Rn ⁸⁶
Fr ⁸⁷	Ra ⁸⁸	Ac ⁸⁹	Rf ¹⁰⁴	Db ¹⁰⁵	Sg ¹⁰⁶	Bh ¹⁰⁷	Hs ¹⁰⁸	Mt ¹⁰⁹	Uun ¹¹⁰								

Ce ⁵⁸	Pr ⁵⁹	Nd ⁶⁰	Pm ⁶¹	Sm ⁶²	Eu ⁶³	Gd ⁶⁴	Tb ⁶⁵	Dy ⁶⁶	Ho ⁶⁷	Er ⁶⁸	Tm ⁶⁹	Yb ⁷⁰	Lu ⁷¹
Th ⁹⁰	Pa ⁹¹	U ⁹²	Np ⁹³	Pu ⁹⁴	Am ⁹⁵	Cm ⁹⁶	Bk ⁹⁷	Cf ⁹⁸	Es ⁹⁹	Fm ¹⁰⁰	Md ¹⁰¹	No ¹⁰²	Lr ¹⁰³

Legend

Li Solid	Cs Liquid	Ar Gas	No Synthetic
Alkali metals	Alkali earth metals	Transition metals	Rare earth metals
Other metals	Noble gases	Halogens	Other nonmetals

<http://www.chemicool.com/>

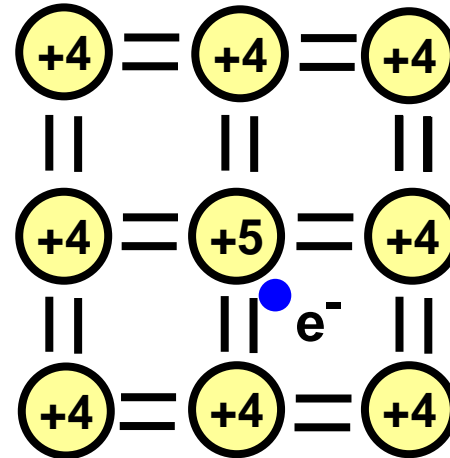
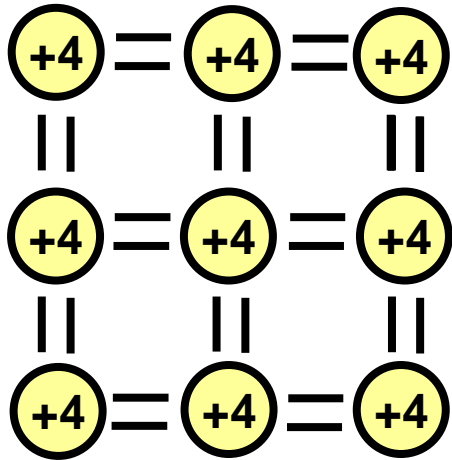
Periodic System

	B ⁵	C ⁶	N ⁷	O ⁸
	Al ¹³	Si ¹⁴	P ¹⁵	S ¹⁶
30 n	Ga ³¹	Ge ³²	As ³³	Se ³⁴
48 d	In ⁴⁹	Sn ⁵⁰	Sb ⁵¹	Te ⁵²
80 g	Tl ⁸¹	Pb ⁸²	Bi ⁸³	Po ⁸⁴

Name	Symbol	#	Valence
Silicon	Si	14	4
Boron	B	5	3
Phosphor	P	15	5
Arsenic	As	33	5
Germanium	Ge	32	4

Semiconductor Physics

See also Tipler (BKV) 38.5



- Intrinsic Si
- Ideal crystal structure
- Valence 4
- almost no free carriers
- almost no conduction

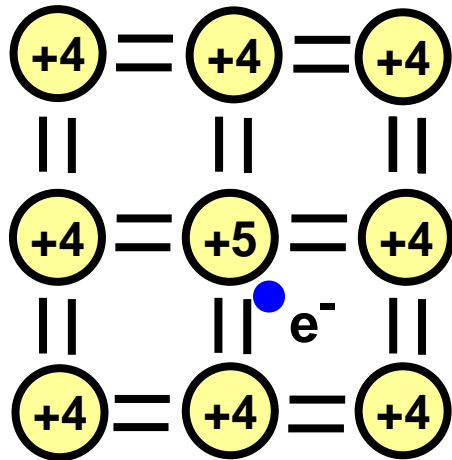
$$[n] = [p] = n_i = 1,5 \cdot 10^{10} / \text{cm}^3$$

at 300 K for silicon

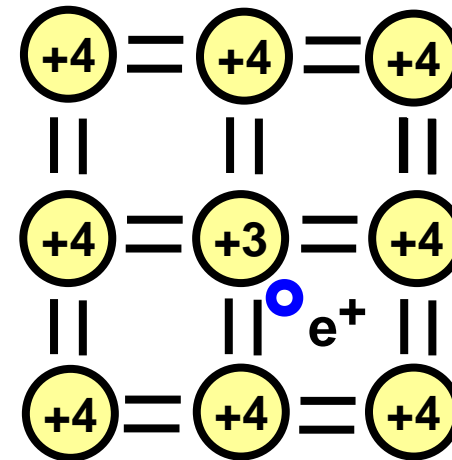
- doping with valence 5 atoms (Phosphor, Arsenic) introduces "loose electrons"
- electron donor
- conductivity depends on doping level

$$n \cdot p = n_i^2 \text{ (in equilibrium)}$$

Semiconductor Physics



- doping with valence 5 atoms (Phosphor, Arsenic) introduces "loose electrons"
- electron donor
- conductivity depends on doping level



- doping with valence 3 atoms (Boron) introduces "loose holes"
- electron acceptors
- hole conductivity lower than electron conductivity

Semiconductor Physics

Si in equilibrium : $n \cdot p = n_i^2 = 2.25 \times 10^{20}$ at 300K
Intrinsic Si : $n = p = n_i$

$$N_D \gg N_A$$

Electron donors: As, P
n-type Si

$$n \approx N_D, p = n_i^2 / n$$

Electrons: majority carriers

Holes: minority carriers

Resistive material

**Conductivity depends
on N_D**

$$N_A \gg N_D$$

Electron acceptors: B
p-type Si

$$p \approx N_A, n = n_i^2 / p$$

Holes: majority carriers

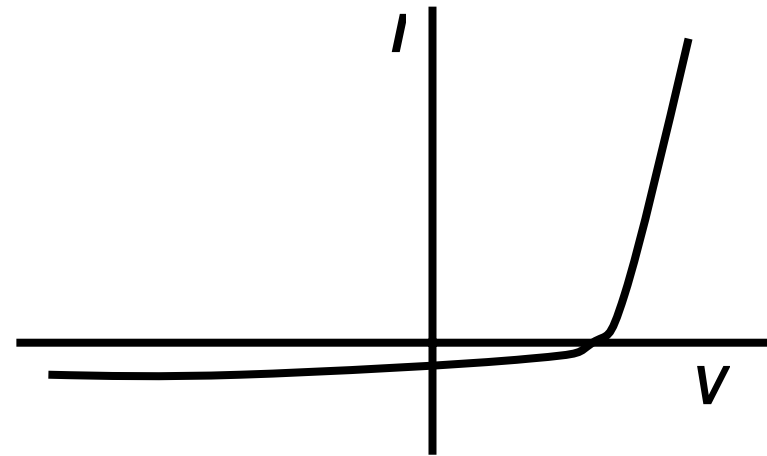
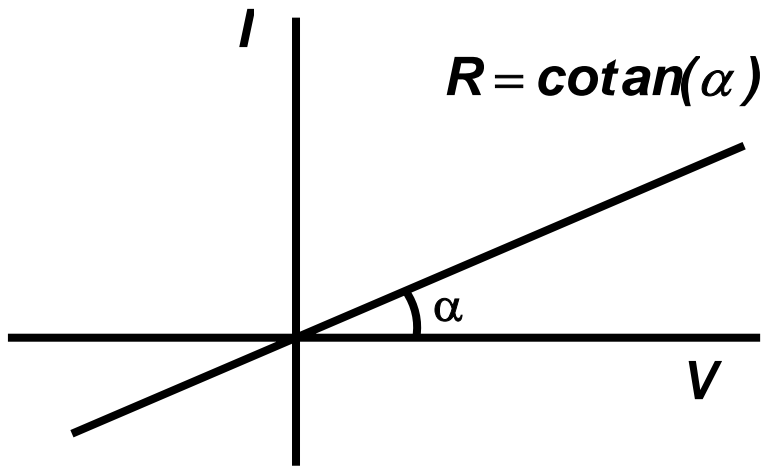
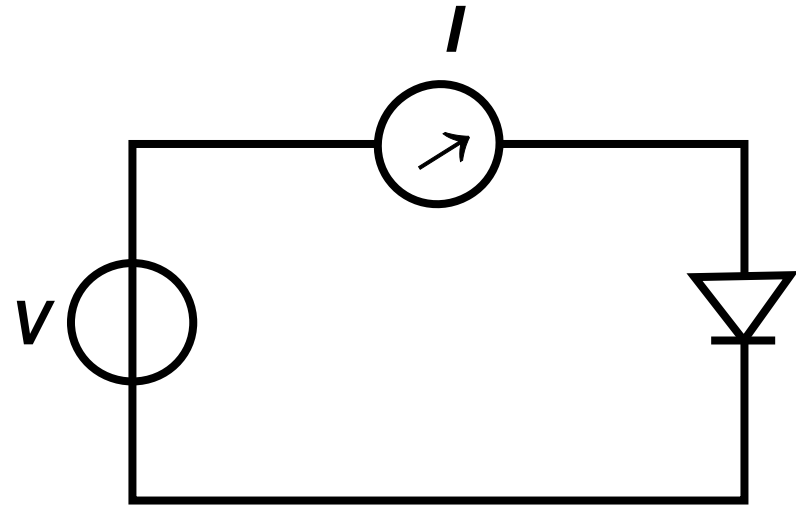
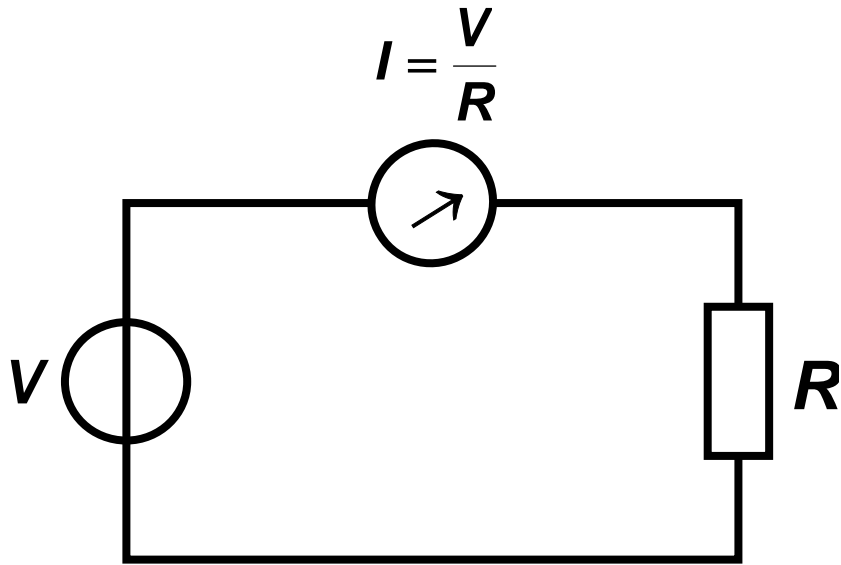
Electrons: minority carriers

**Hole conductivity lower
than electron conductivity**

The diode

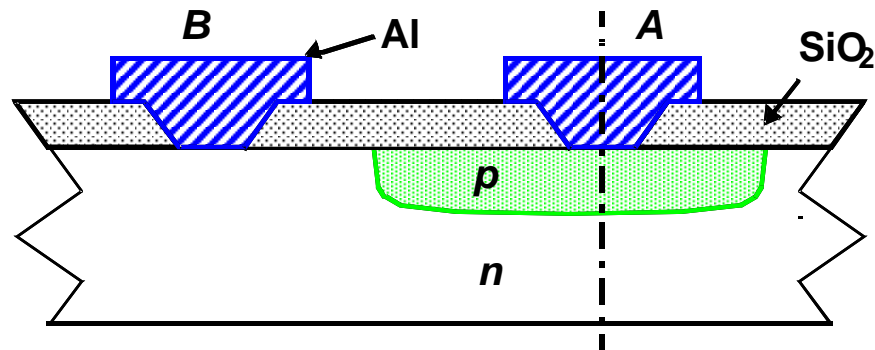
- Depletion, I-V relations, capacitance,

The diode: non-linear resistance

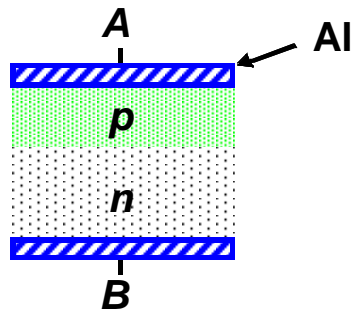


The Diode

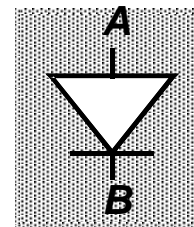
See also Tipler (BKV) 38.6



Cross-section of *pn*-junction in an IC process



One-dimensional representation



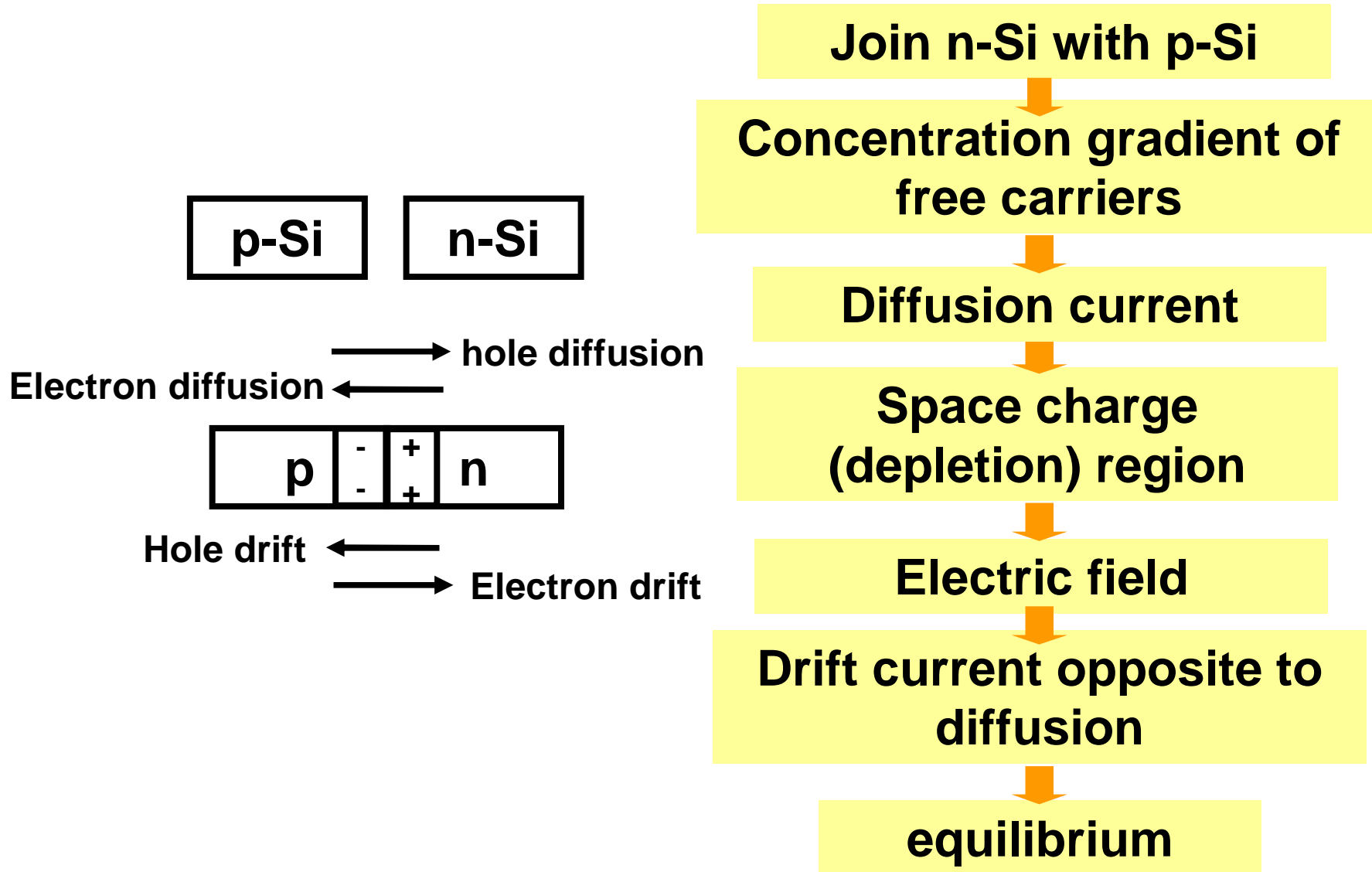
Anode

Cathode

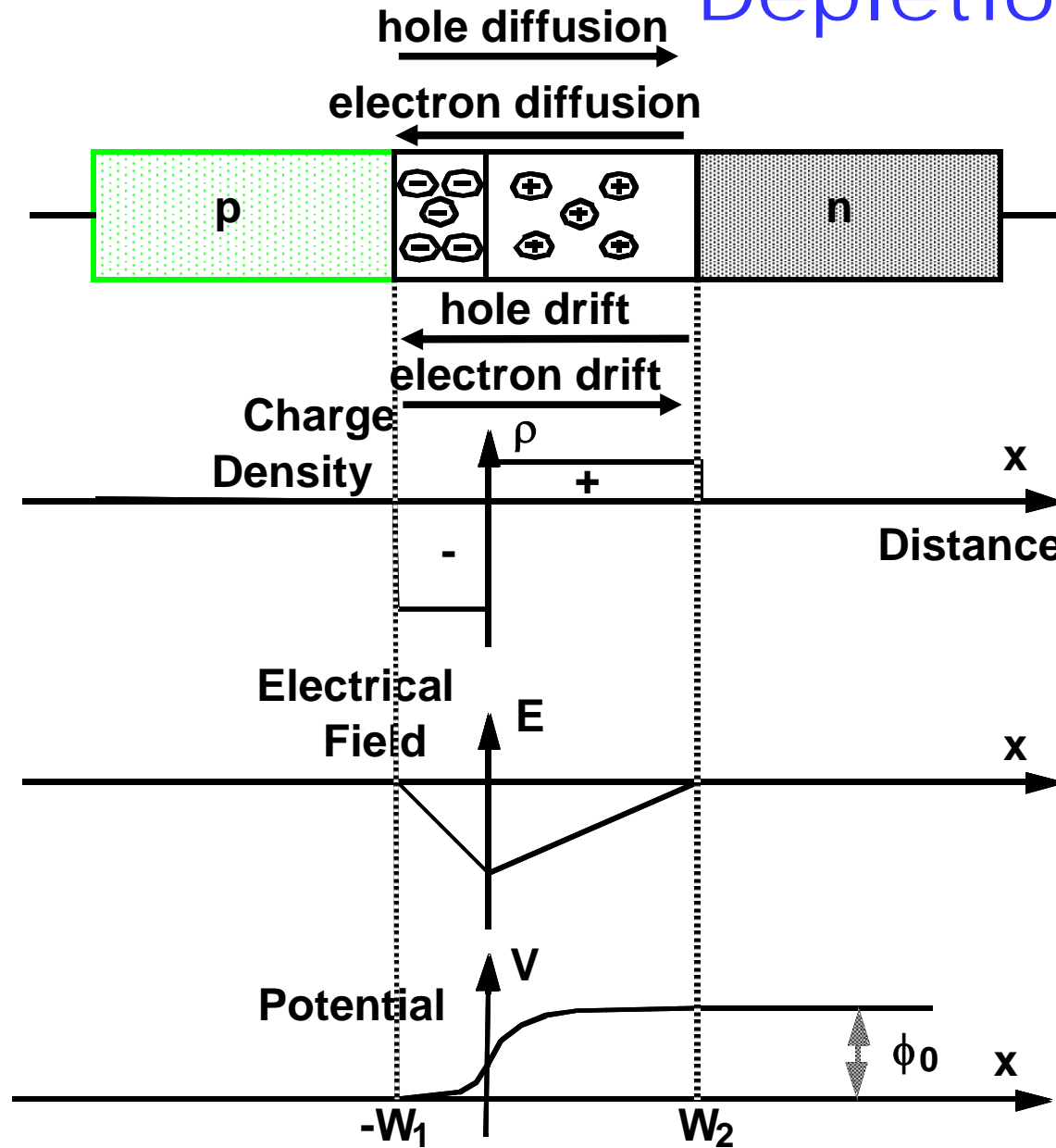
diode symbol

Diode is abundant as MOS source/drain

Ideal Diode, Abrupt pn junction Intuitive Description



Depletion Region



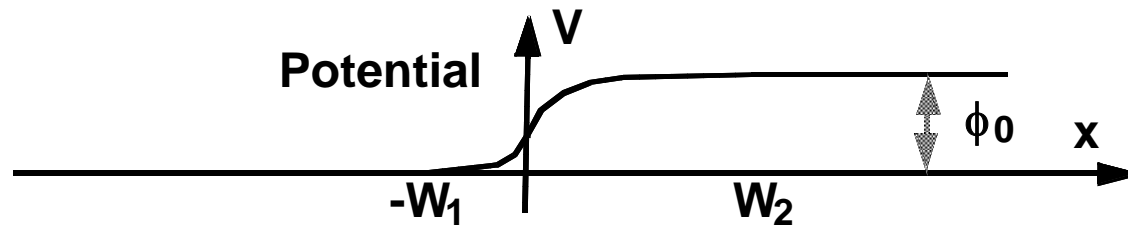
(a) Current flow.

(b) Charge density.

(c) Electric field.

(d) Electrostatic potential.

Conduction



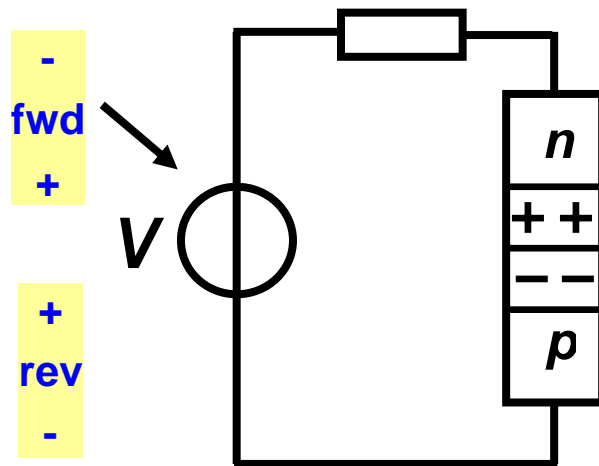
Typical N_A, N_D :
 $10^{15} \dots 10^{17}/\text{cm}^3$,
 ϕ_0 around 0.6 V

Built-in Potential

$$\phi_0 = \phi_T \ln \left[\frac{N_A N_D}{n_i^2} \right]$$

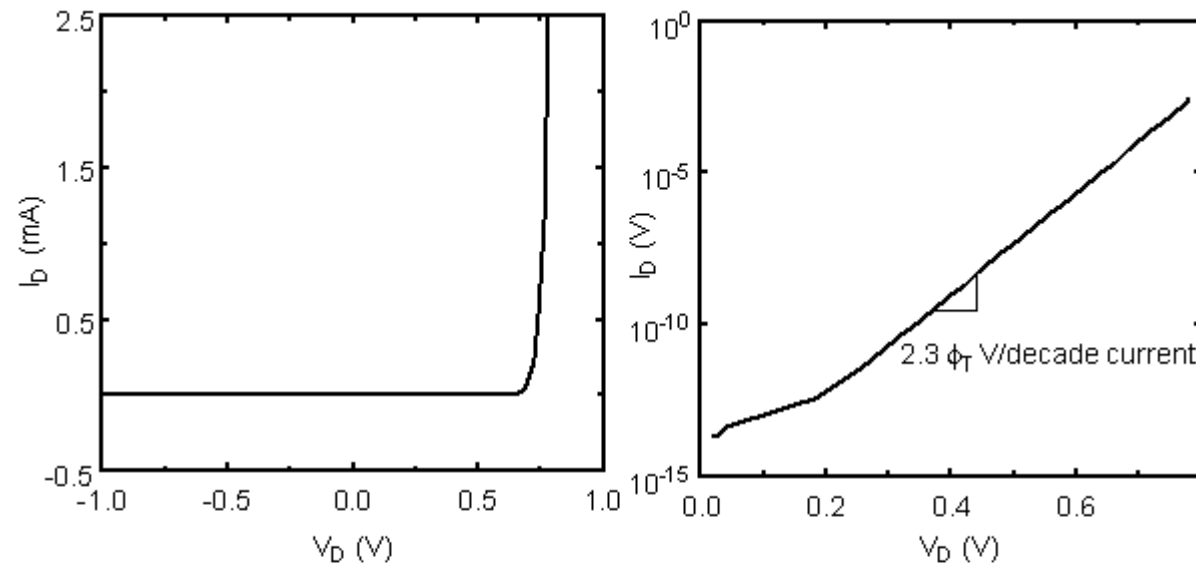
Thermal voltage

$$\phi_T = \frac{kT}{q} = 26 \text{ mV at } 300 \text{ K}$$



- By applying an external voltage, width of depletion region can be changed
- Forward: becomes smaller and smaller, finally conduction
- Reverse: becomes wider and wider => no conduction

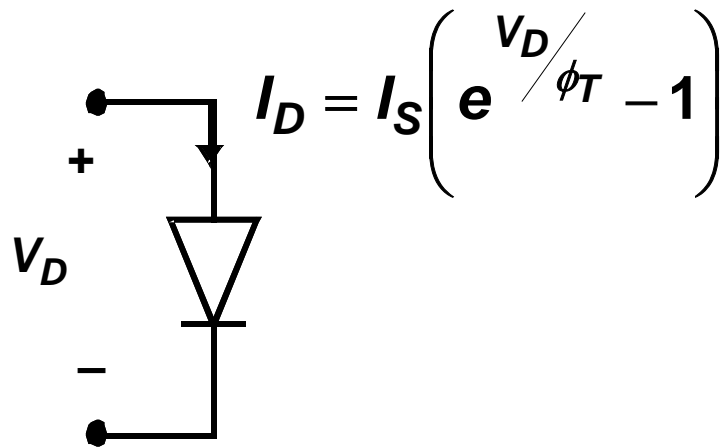
Diode Current



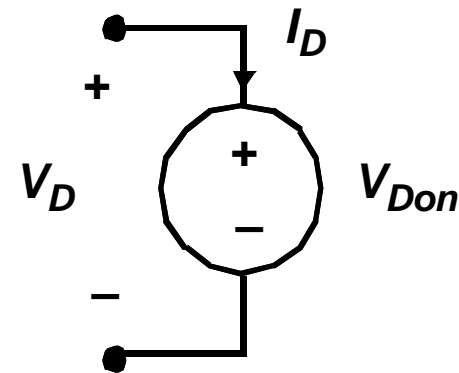
$$I_D = I_S (e^{V_D/\phi_T} - 1)$$

- I_S : Saturation current
- Proportional to diode area
- Depends on doping levels, and widths of neutral regions
- Usually determined empirically

Models for Manual Analysis

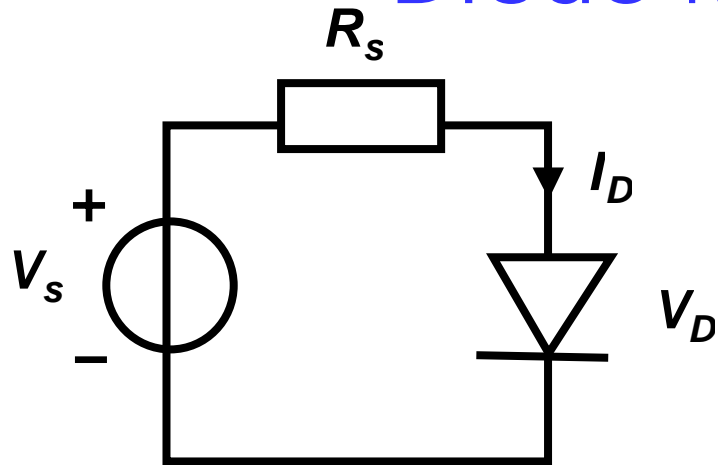


(a) Ideal diode model



(b) First-order diode model

Diode Model Example



Determine I_D

$$I_D = I_S(e^{V_D/\phi_T} - 1) \text{ (diode model)}$$

$$V_s - R_s I_D = V_D \text{ (Kirchhoff)}$$

$$V_s - R_s I_S(e^{V_D/\phi_T} - 1) = V_D \text{ ☹️}$$

Iteration

$$I_S = 0.5e^{-16} \text{ A}$$

$$kT/q = 25 \text{ mV}$$

$$V_s = 1.6 \text{ V}$$

$$R_s = 1 \text{ k}\Omega$$

start:

$$V_D = 1.0 \text{ V}$$

$$\Rightarrow I_D = (V_s - V_D)/R_s = 0.600 \text{ mA}$$

$$\Rightarrow V_D = \phi_T(1 + \ln(I_D/I_S)) = 0.663 \text{ V}$$

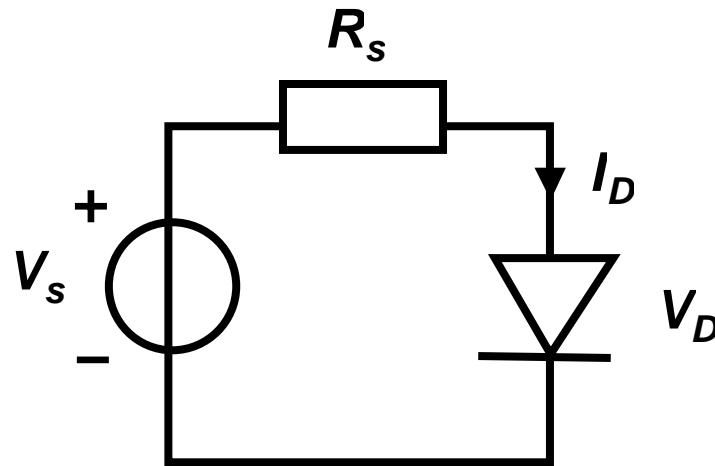
$$\Rightarrow I_D = 0.937 \text{ mA}$$

$$\Rightarrow V_D = 0.674 \text{ V}$$

$$\Rightarrow I_D = 0.926 \text{ mA}$$

$$\Rightarrow V_D = 0.674 \text{ V} \text{ 😊}$$

Diode Model Example



$$I_s = 0.5e^{-16} \text{ A}$$

$$kT/q = 25 \text{ mV}$$

$$V_s = 1.6 \text{ V}$$

$$R_s = 1 \text{ k}\Omega$$

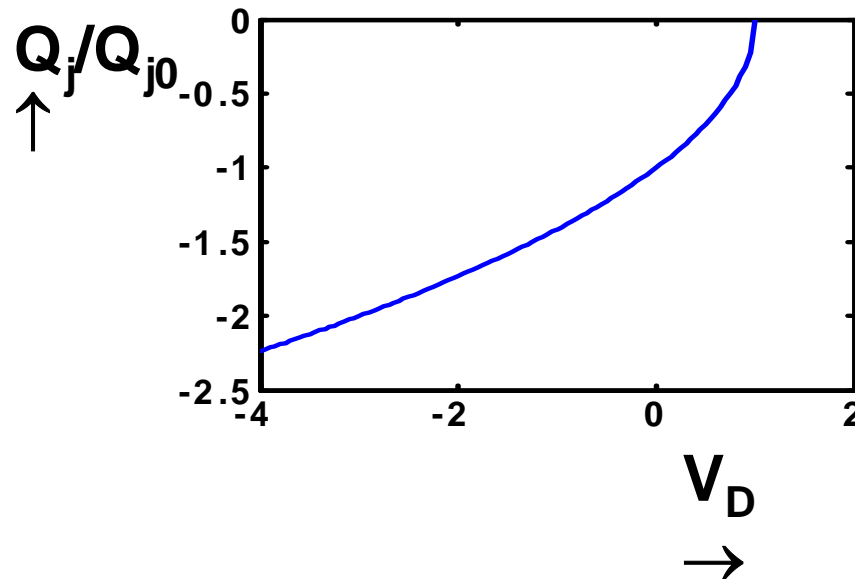
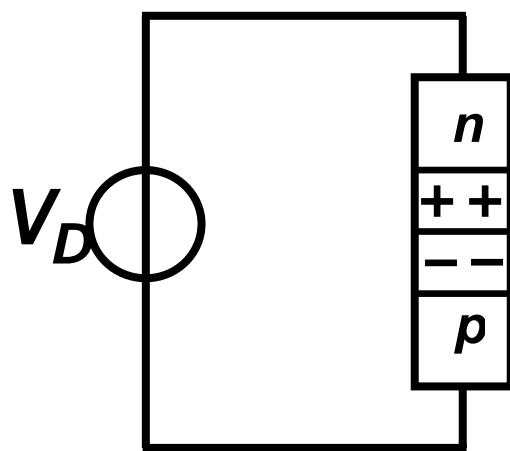
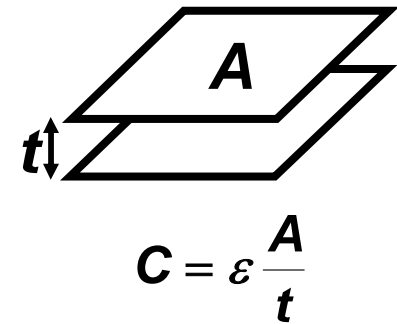
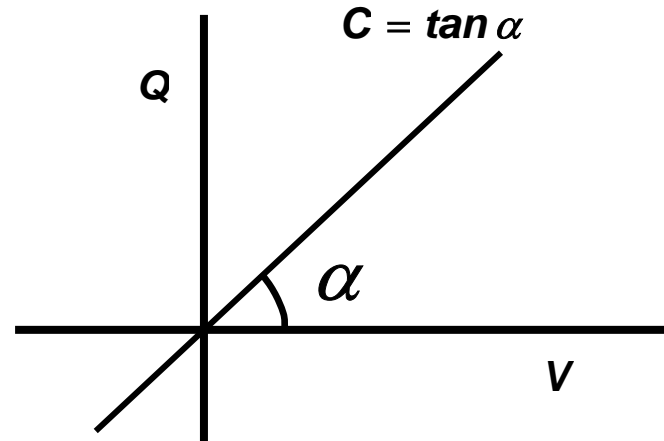
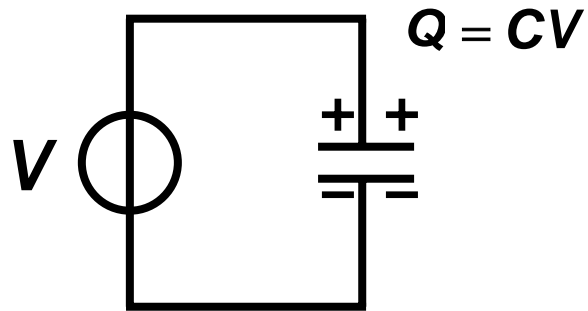
First order solution

$$V_D = 0.6 \text{ V} \Rightarrow I_D = 1 \text{ mA} \quad \text{error} = 8 \%$$

Now, take $V_s = 10.6 \text{ V}$ $R_s = 10 \text{ k}\Omega$

The error will be

Capacitance



Linearized Large-Signal Diode Capacitances

Summary:

- Diode capacitances **highly non-linear**
- Difficult with manual calculation
- We are ultimately interested in **amount of charge** being stored on (or removed from) capacitor
 - Since it takes time for this to happen, this determines the final **switching speed** of the circuit: more charge means more time!
- Linear capacitance: $\Delta Q = C\Delta V$: easy to work with
- Small-signal capacitance: $dQ = CdV$: for **analog** appl.
- Non-linear capacitance: $\Delta Q = f(V_{\text{low}}, V_{\text{high}})$

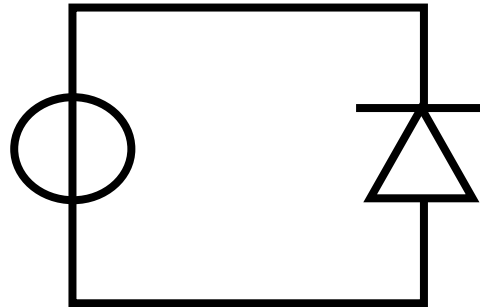


See the syllabus!

Work with C_{eq} for standardized voltage swings

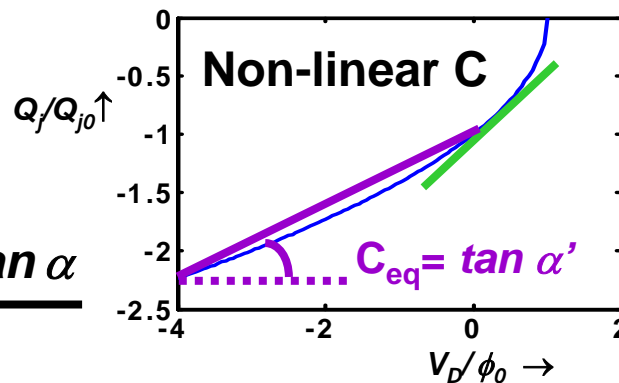
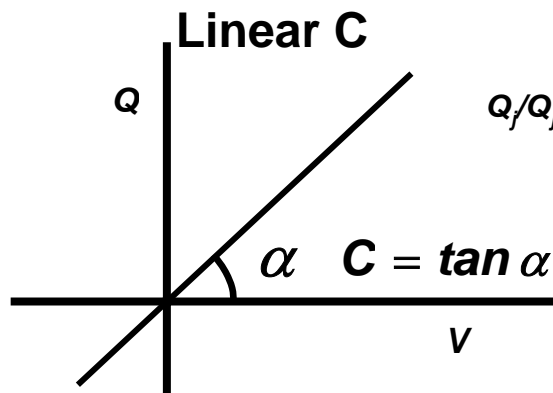
Large Signal Equivalent Diode Capacitance

step voltage

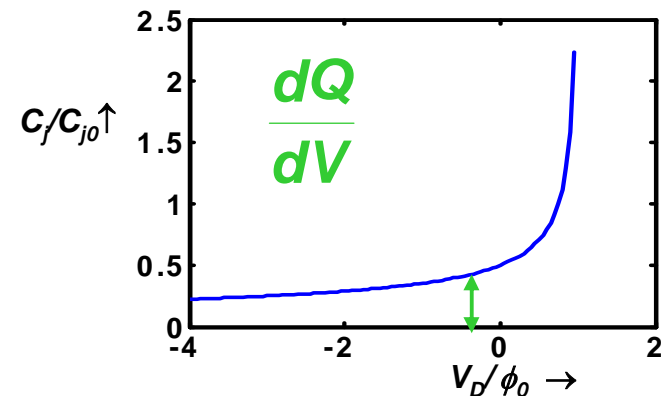



$$C_{eq} = f(V_{high}, V_{low})$$

$$= \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}}$$



Linearized, large signal,
depends on swing



Linearized, small signal,
depends on bias
For analog applications

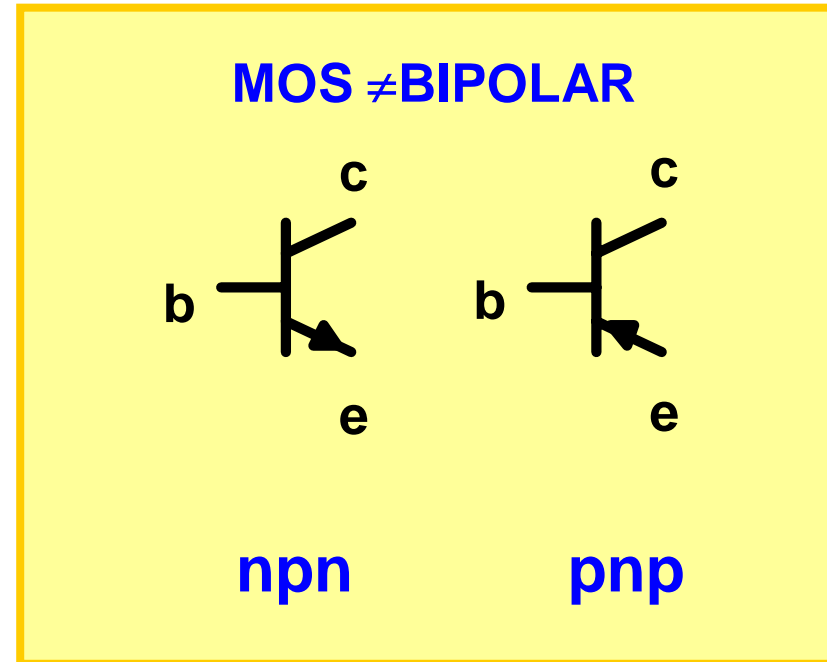
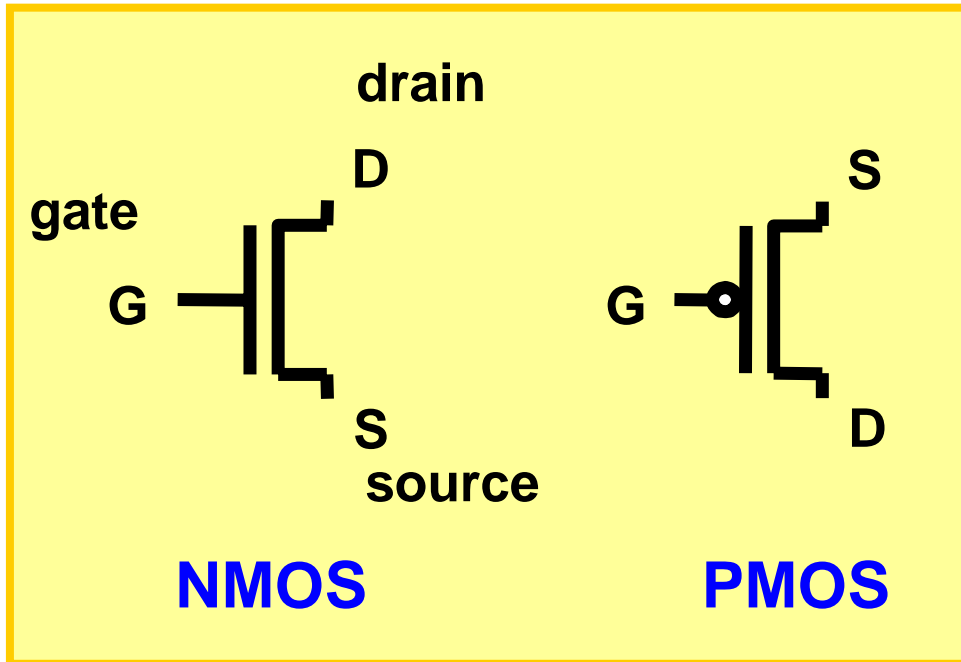
The MOS Transistor

- **First glance, threshold, I-V relations, models**
- **Dynamic behavior (capacitances), resistances, more Second-Order effects, models**

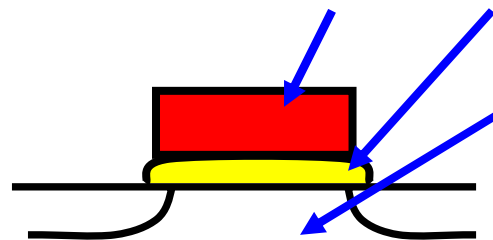
The MOS Field Effect Transistor – compared to Storey

- MOSFET transistor is not a JFET
- **Other operating regions** compared to saturation region (linear, velocity saturation) also important
- Include more effects (channel length modulation)
- **Short-channel** devices
 - bad for some analog circuits,
 - good for (most) digital circuits
- We will develop understanding of basic **device equations**

MOSFET Transistors



MOSFET = “Metal”-Oxide-Semiconductor Field-Effect Transistor



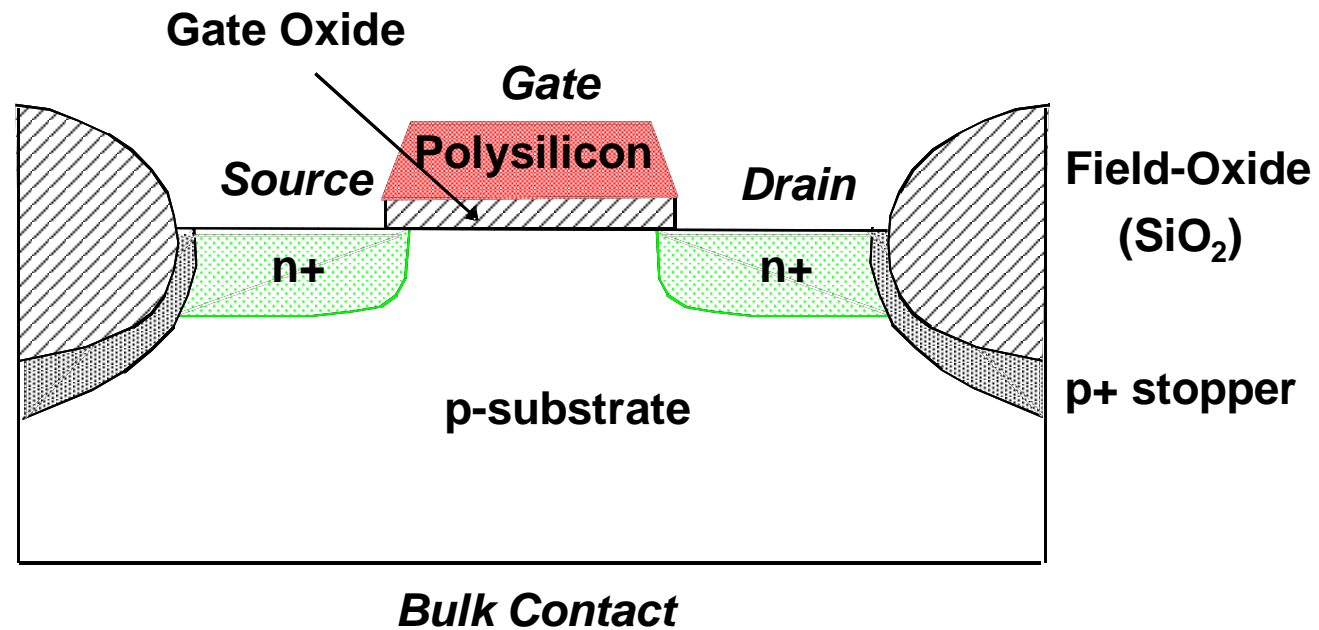
Cross-sectional view of MOSFET

Gate (terminal of MOSFET)

≠

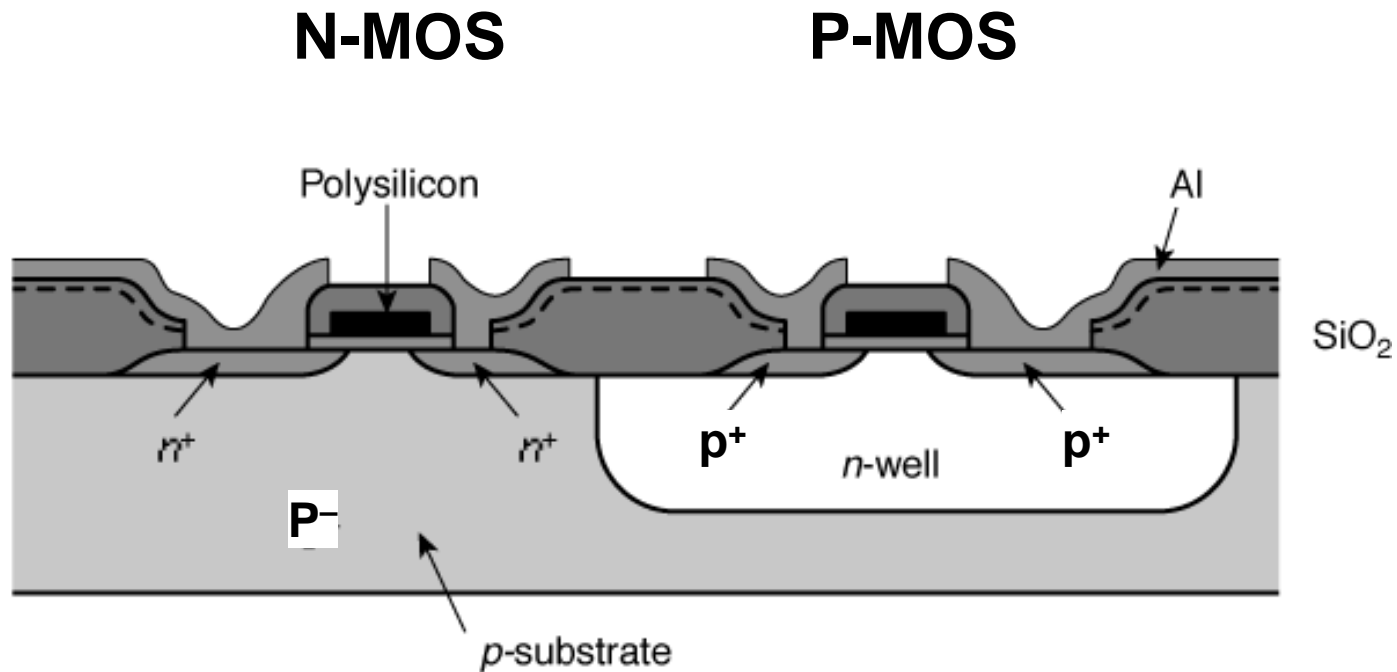
Logic gate

The MOS Transistor

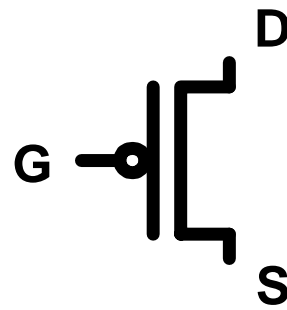
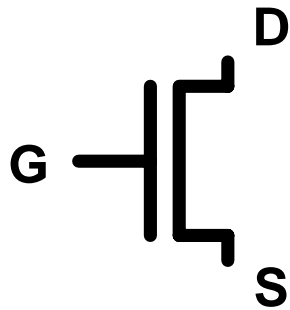


CROSS-SECTION of NMOS Transistor

Cross-Section of CMOS Technology

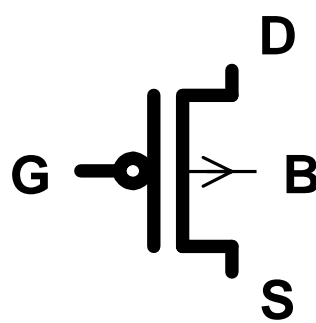
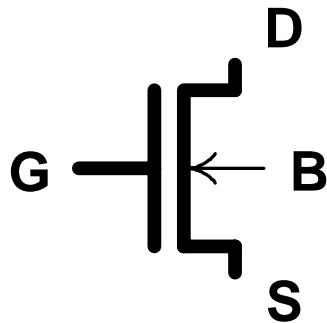


MOS Transistors



3-terminal model

bulk assumed to be connected to appropriate supply



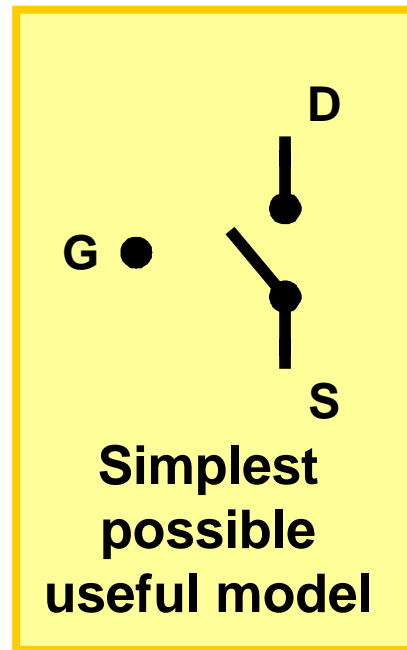
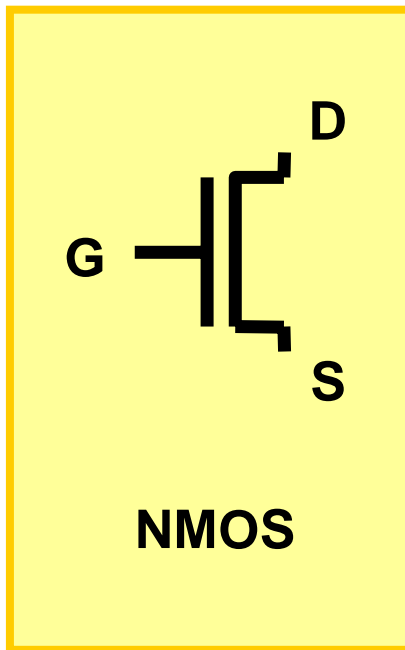
4-terminal model

B = bulk (substrate)

NMOS

PMOS

MOS Transistor Switch Level Models



Position of switch depends on gate voltage

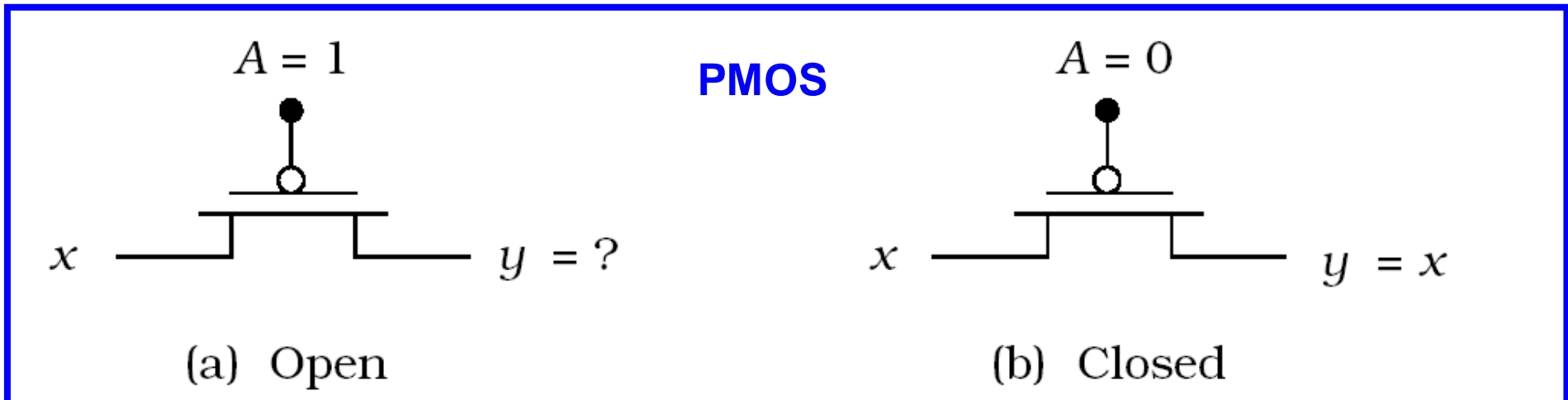
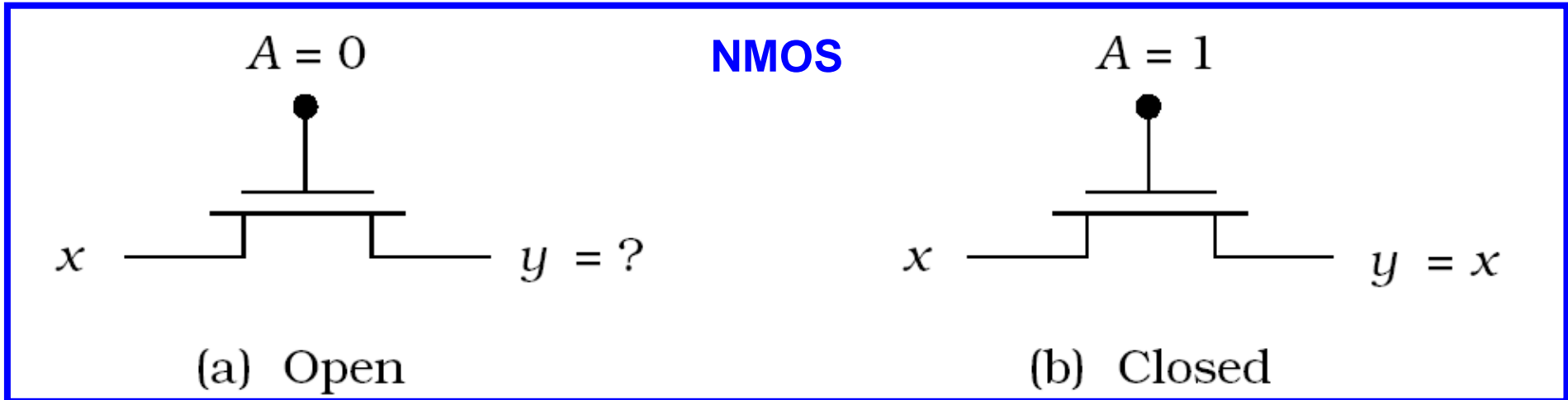
V_G	NMOS	PMOS
hi	closed	open
lo	open	closed

- Connection between source and drain depends on gate voltage, current can flow from **source to drain and vice versa** if closed
- No **static** current flows into gate terminal

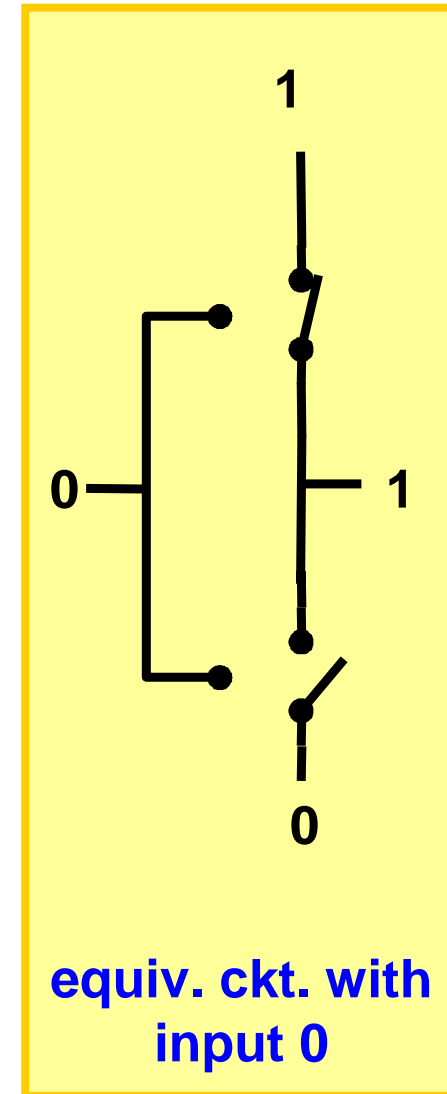
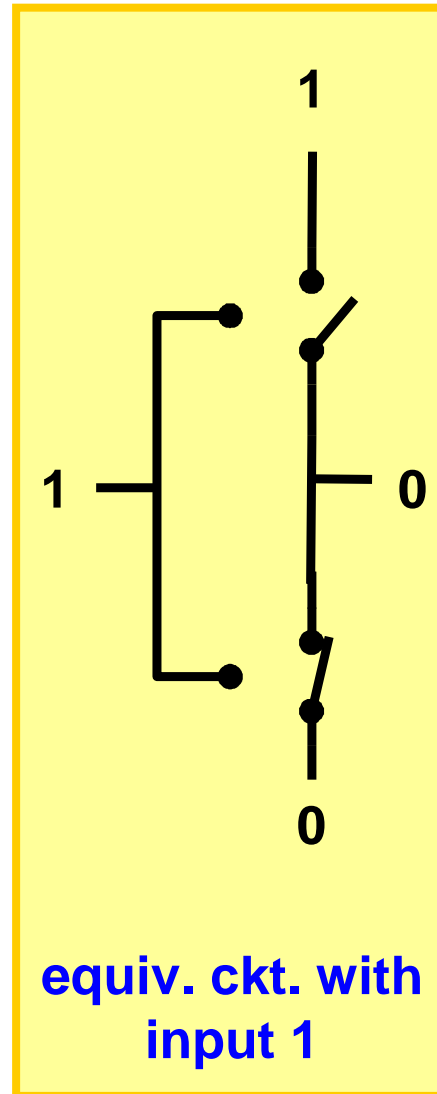
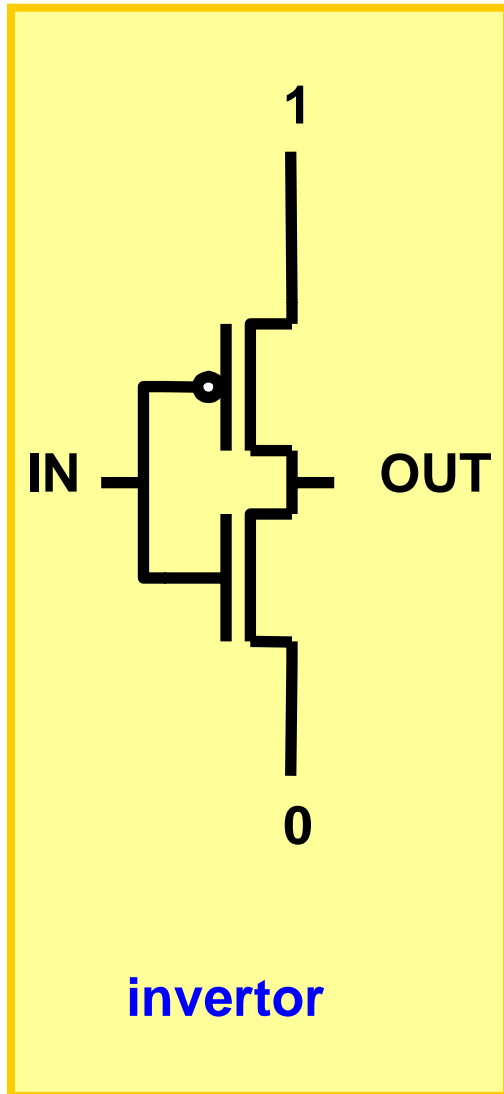
Mos Switch Model (2)

Position of switch depends on gate voltage

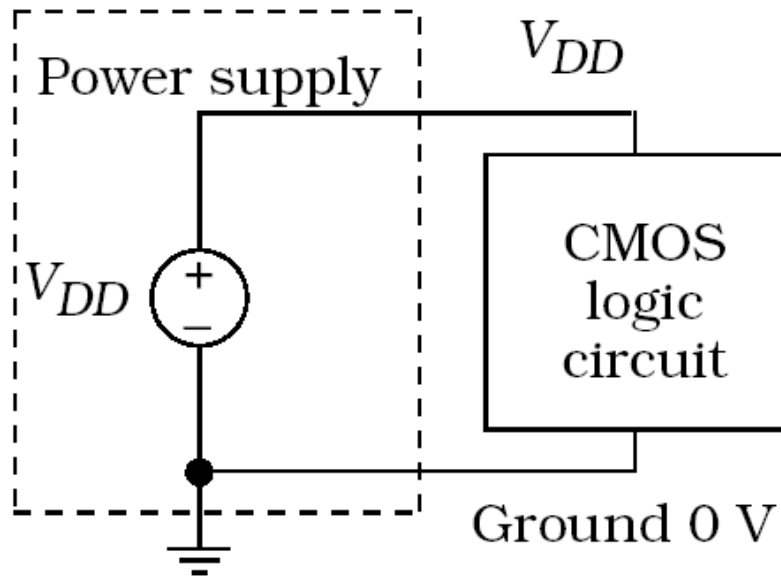
V_G	NMOS	PMOS
hi	closed	open
lo	open	closed



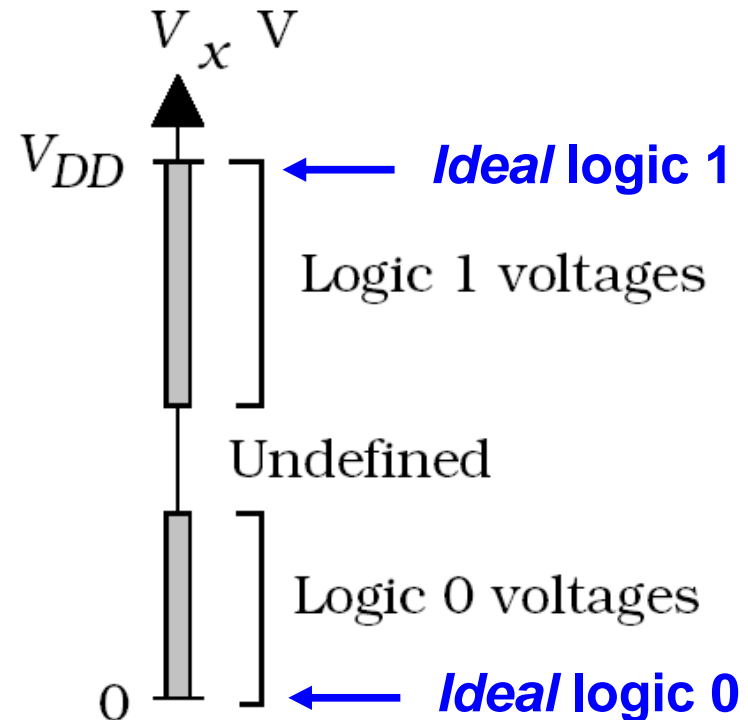
CMOS Inverter Operation Principle



From Logic to Voltages



(a) Power supply connection

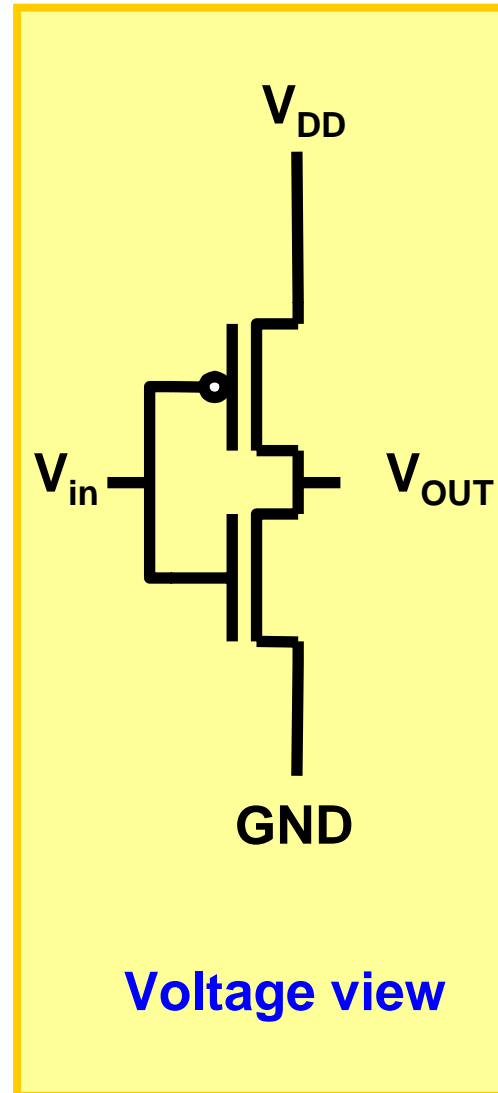
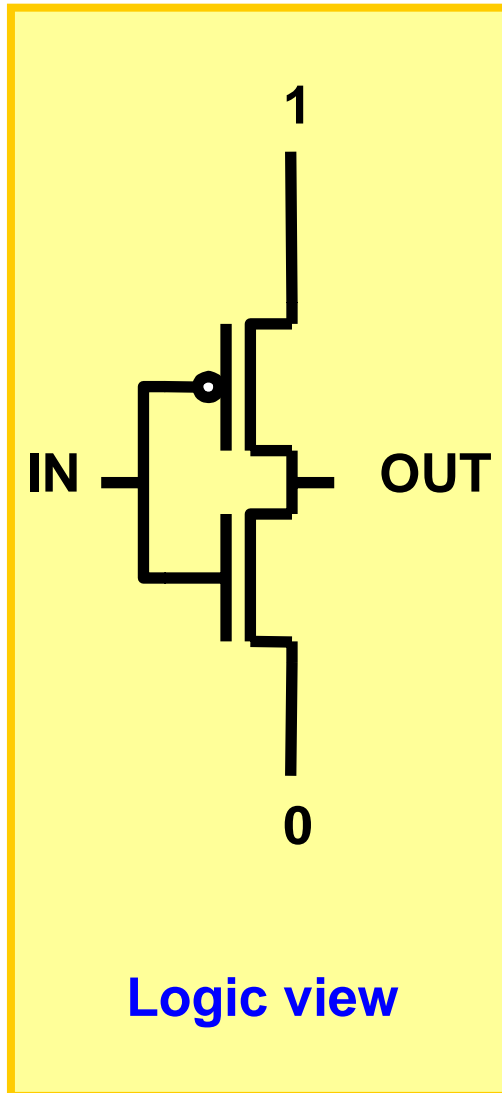


(b) Logic definitions

***Ideal logic 0* corresponds to $V_x = 0V$**
***Ideal logic 1* corresponds to $V_x = V_{DD}$**

Not all actual voltages in circuit necessarily correspond to ideal logic levels, see figure (b) above

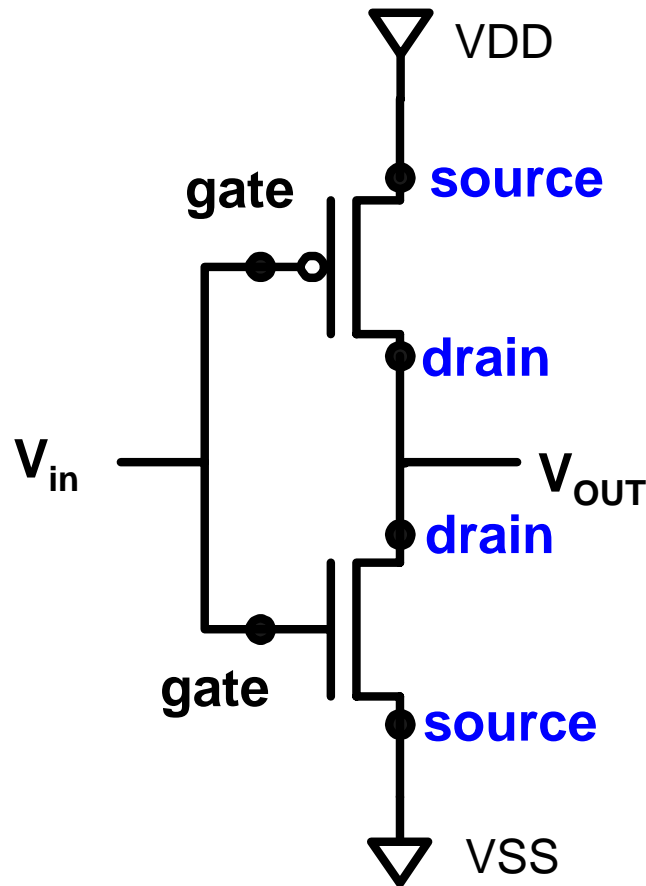
From Logic to Voltages



Note:

- GND = GROUND = 0V
- Sometimes also called V_{SS}
- V_{DD} is highest voltage level in circuit
- V_{DD} value depends on technology, has been reduced from 5V to 1V and lower over the years
- All voltages V_x in ckt: $0 \leq V_x \leq V_{DD}$

Source and Drain Terminals



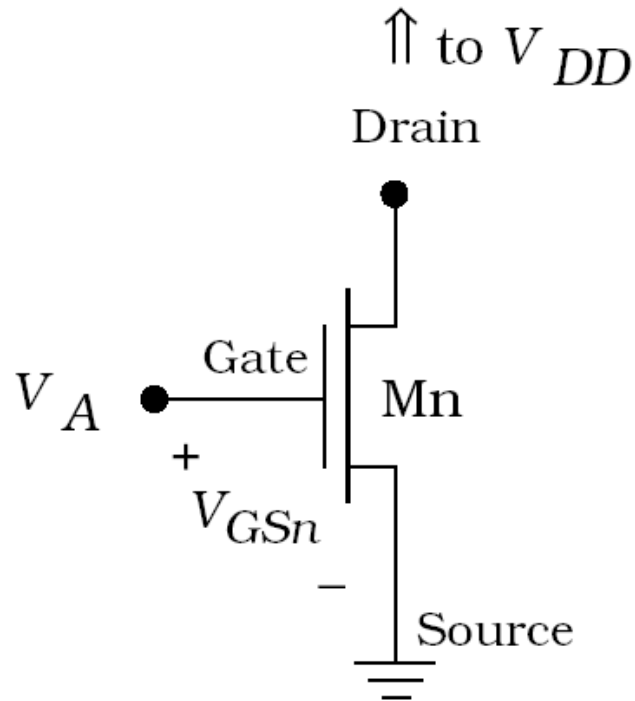
	NMOS	PMOS	PMOS
Source	Lowest potential	Highest potential	Lowest potential
Drain	Highest potential	Lowest potential	Highest potential

Note 1: Polarities of PMOS voltage reversed when compared to NMOS

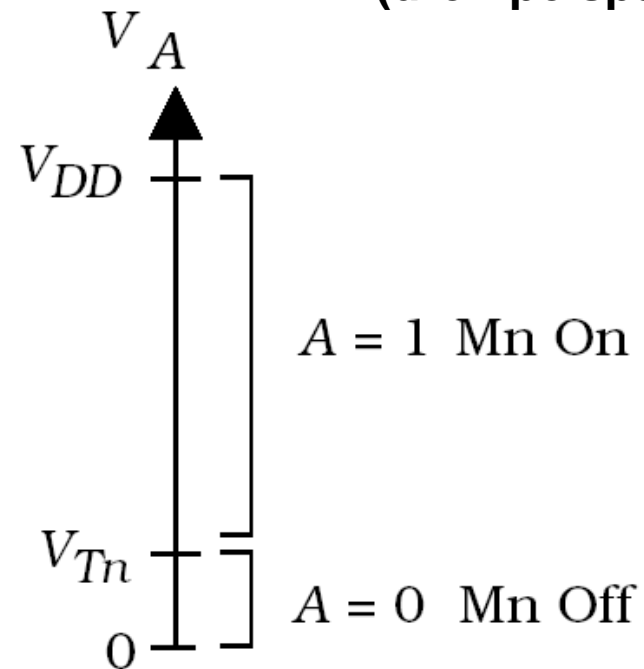
Note 2: MOS transistor is **completely symmetrical!** Can interchange source and drain, without any effect. Source/drain is only a **naming convention.**

nFET Threshold Voltage

(drempelspanning)



(a) Gate-source voltage

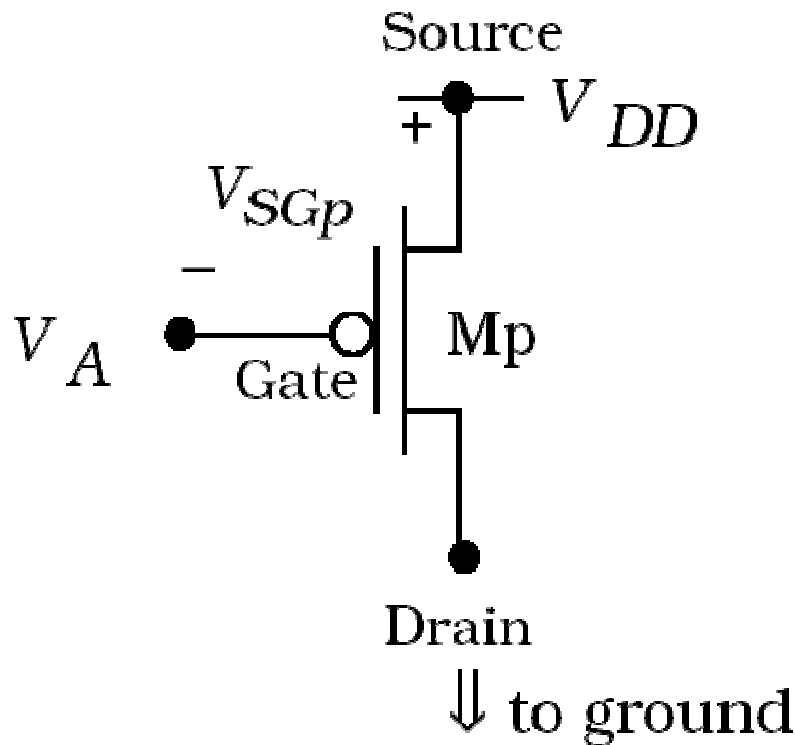


(b) Logic translation

nFET is off when $V_{GSn} \leq V_{Tn}$
nFET is on when $V_{GSn} > V_{Tn}$

$V_{Tn} \sim 0.5 \dots 0.7V$

pFET Threshold Voltage



nFET is off when $V_{GSn} \leq V_{Tn}$
nFET is on when $V_{GSn} > V_{Tn}$

pFET and nFET behave complementary

Equivalent conditions

pFET is off when $V_{GSp} \geq V_{Tp}$
pFET is on when $V_{GSp} < V_{Tp}$

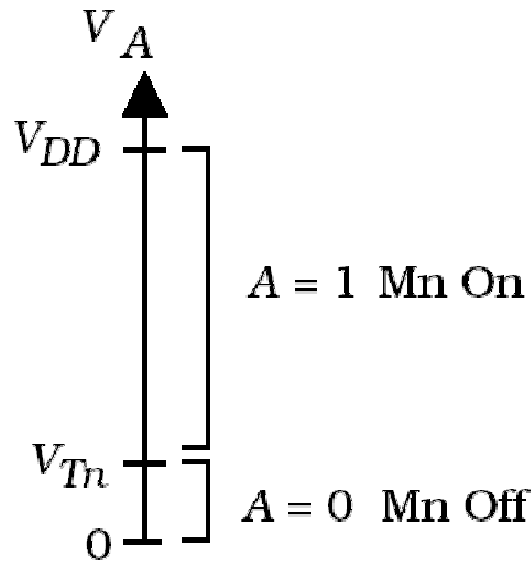
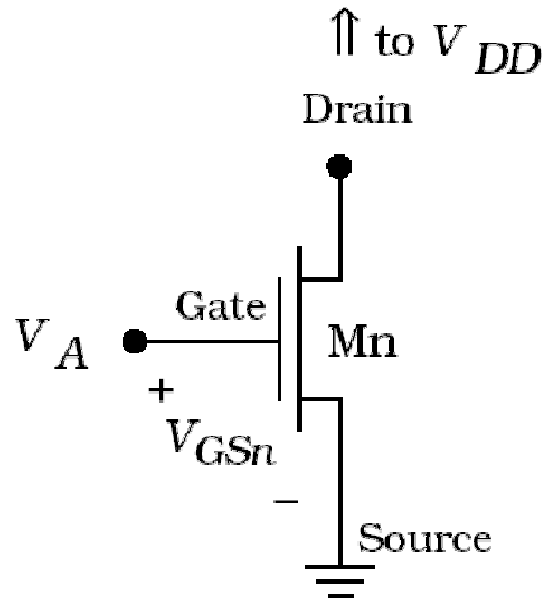
pFET is off when $-V_{GSp} \leq -V_{Tp}$
pFET is on when $-V_{GSp} > -V_{Tp}$

pFET is off when $|V_{GSp}| \leq |V_{Tp}|$
pFET is on when $|V_{GSp}| > |V_{Tp}|$

$V_{Tp} \sim -0.5 \dots -0.7V$ (negative!)

Often most useful

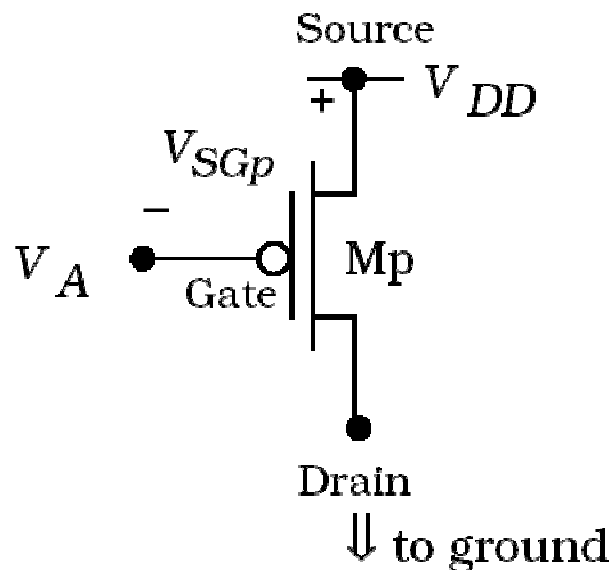
Excercise



transistor on the left using

nFET is off when $V_{GSn} \leq V_{Tn}$
 nFET is on when $V_{GSn} > V_{Tn}$

corresponds to diagram on right

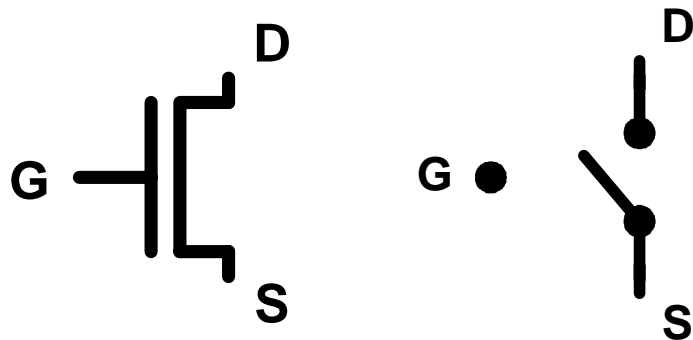


Draw same diagram for PMOS using

pFET is off when $-V_{GSp} \leq -V_{Tp}$
 pFET is on when $-V_{GSp} > -V_{Tp}$

MOS Transistor Threshold Voltage

Threshold voltage V_T : point at which transistor turns on



Position of switch depends on gate voltage (relative to source)

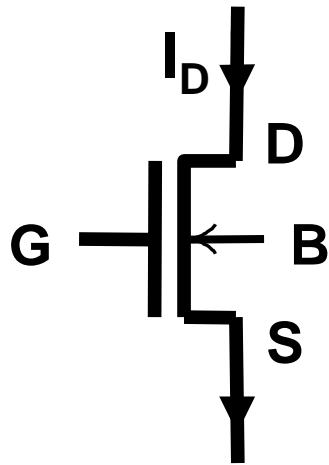
V_{GS}	NMOS	PMOS
$V_{GS} > V_T$	closed	open
$V_{GS} < V_T$	open	closed

Is this all there is?



- You don't believe that (CMOS) life can be so simple, do you?
- Think of some of the things that you would expect to be non-idealities of CMOS as a switch
- Discuss with your neighbor
- Share with us
- Since we want to design CMOS circuits, we need a deeper understanding of CMOS circuits
- Next slide shows where we are going

MOS Models for Manual Analysis



determined by circuit

$$V_{DS}, V_{GS}, V_{SB}$$

determined by technology

$$k, \lambda, V_{DSAT}, V_{T0}, \gamma, \phi_F$$

MOS model for manual analysis

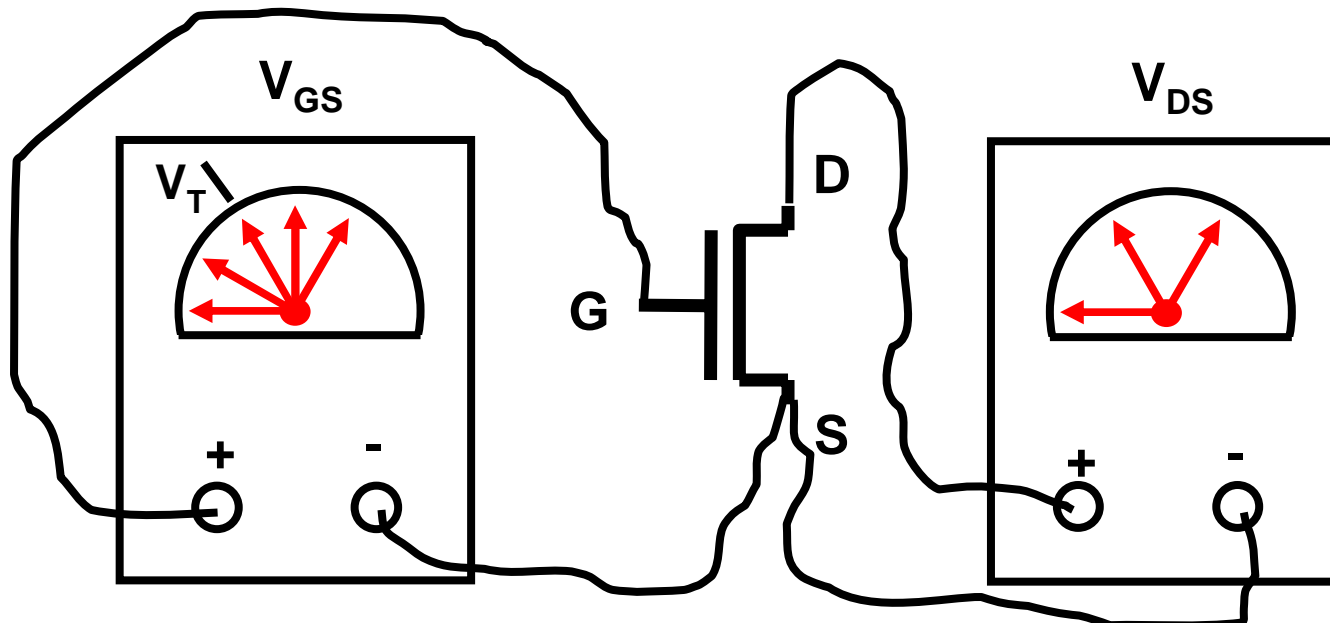
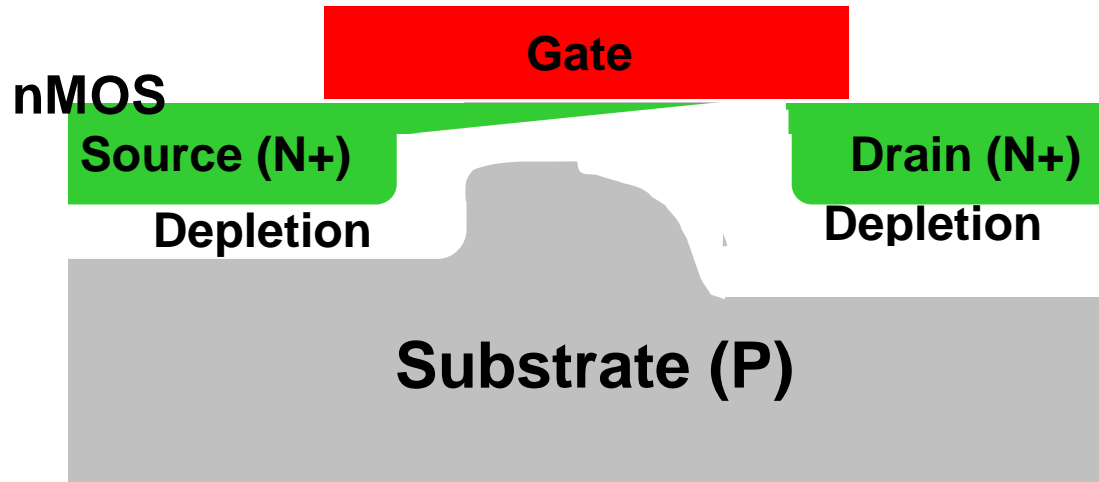
$$I_D = k(V_{GT}V_{MIN} - 0.5V_{MIN}^2)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$

$$= 0 \quad \text{for } V_{GT} \leq 0$$

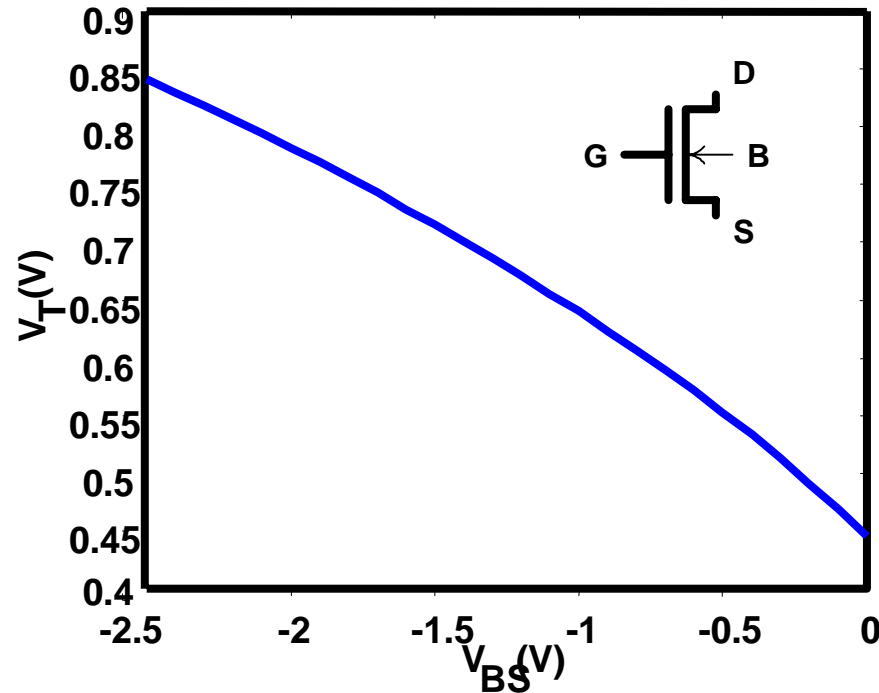
$$V_{MIN} = \text{MIN}(V_{DS}, V_{GT}, V_{DSAT})$$

$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

nMOS Transistor Operation



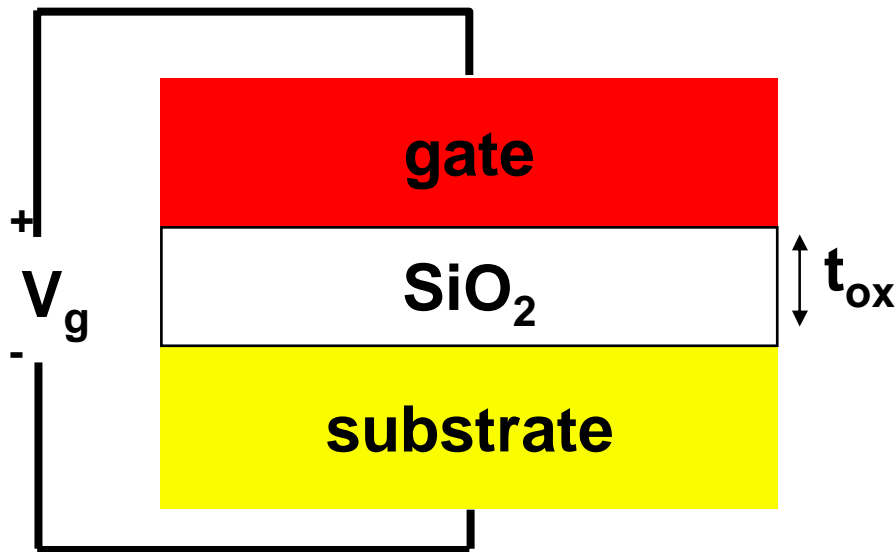
Body Effect



- V_T is **not constant**
- Depends on V_S vs V_B
- Our wish is to understand & predict behavior of CMOS devices
- We will start with V_T

MOSFET gate as capacitor

- Gate capacitance helps determine charge in channel which forms **inversion region**.
- Basic structure of gate is **parallel-plate capacitor**:



$$C_{ox} = \epsilon_{ox} / t_{ox}$$

$$\epsilon_{ox} = \epsilon_0 \epsilon_r$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$$

$$\epsilon_r = 3.9 \text{ (SiO}_2\text{)}$$

Note: [F] vs. [F/m²]

The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Contact Potential
 Fermi Potential
 Depletion Layer Charge
 Surface Charge
 Implants

$$Q_B = \gamma(\sqrt{-2\phi_F + V_{SB}})$$

with

$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_A}}{C_{ox}}$$

↑
Body Effect Coefficient

Forget all this

$$V_T = V_{T0} + \gamma(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F})$$

But be able to use this

with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and this

$$I_D(V_{GS}, V_{DS}, V_{BS})$$

MOS model for manual analysis

$$I_D = k(V_{GT}V_{MIN} - 0.5V_{MIN}^2)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$

$= 0$

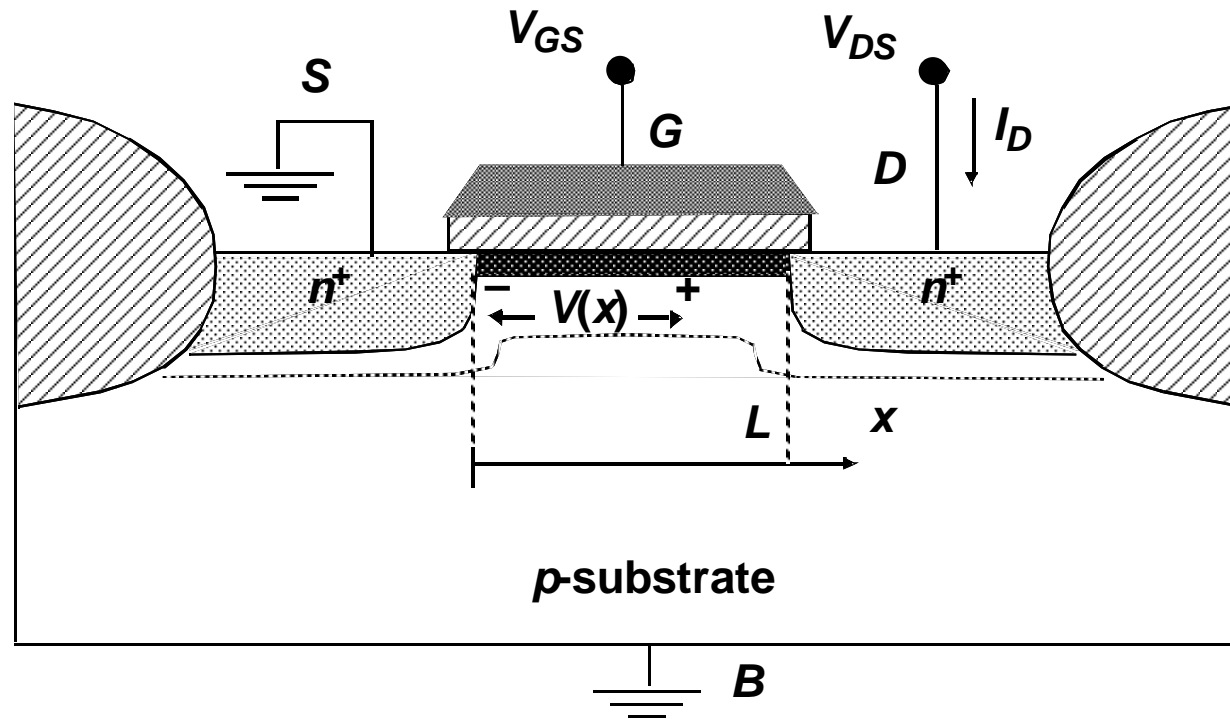
$$\text{for } V_{GT} \leq 0$$

$$V_{MIN} = \text{MIN}(V_{DS}, V_{GT}, V_{DSAT})$$

- Different operation regions
- Different behavior for each region:
 - off
 - resistive
 - saturation
 - velocity saturation

← NEXT

Current-Voltage Relations



MOS transistor and its bias conditions

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

I-V In Resistive Region

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T] \quad \text{Inversion Charge}$$

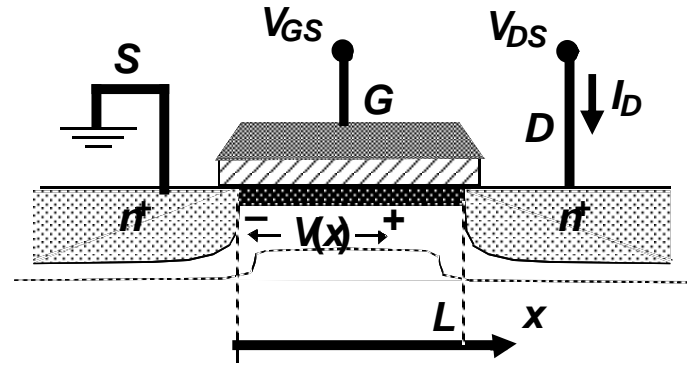
$$I_D = -\mu_n \frac{dV}{dx} Q_i(x) W$$

I_D Drain Current
 μ_n mobility (n-Si)

$$\int_0^L I_D dx = -\mu_n \epsilon_{ox} W \int_0^L \frac{dV}{dx} [V_{GS} - V(x) - V_T] dV$$

$$I_D L = \mu_n C_{ox} W \left[(V_{GS} - V_T)V - \frac{1}{2} V^2 \right]_0^{V_{DS}}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$



Process Gain and Device Gain

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$k'_n = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}}$$

Process transconductance parameter

$$k = k'_n \frac{W}{L}$$

Gain factor of device

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (\text{resistive regime})$$

Storey uses $K = \frac{1}{2}k$

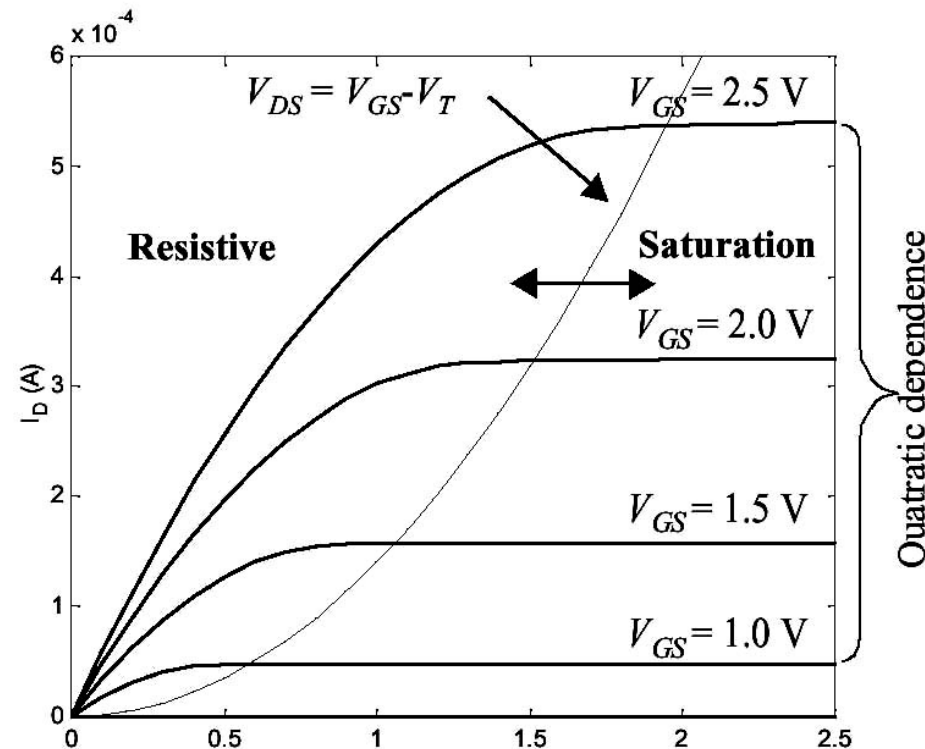
■ Note 1: we use k , many others β , but $k = \beta$

■ Note 2: **resistive** regime a.k.a. **triode** regime

Storey: Ohmic region

I-V Relation

This and similar graphs to follow are from the book

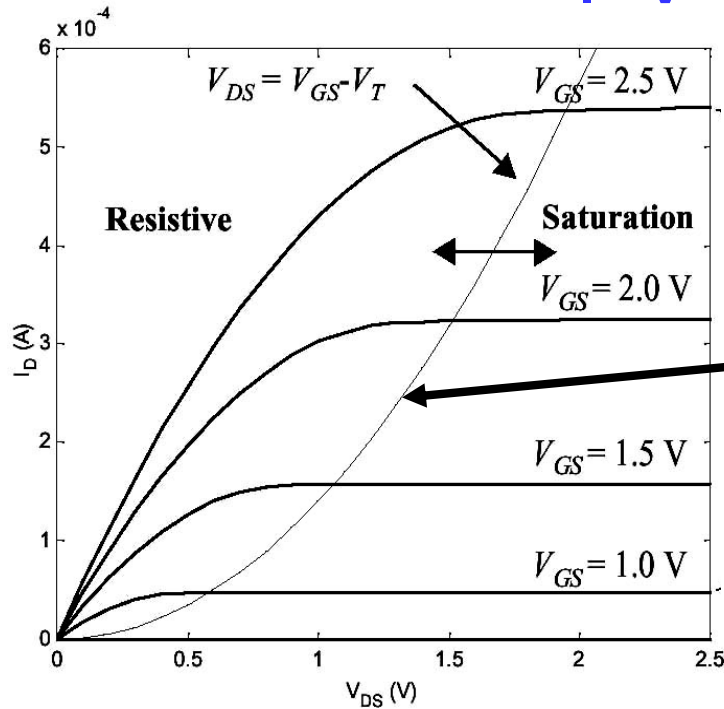


$L_d = 10 \mu\text{m}$,
 $W = 15 \mu\text{m}$

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]^{V_{DS} (V)} \quad \text{(resistive regime)}$$

This formula **only valid in resistive regime**. This corresponds to the region to the left of the $V_{DS} = V_{GS} - V_T$ curve. There is **another regime** called 'saturation'. See following slides.

I-V Relation



This curve is where I_D curves begin to run flat: I_D does not anymore depend on V_{DS}

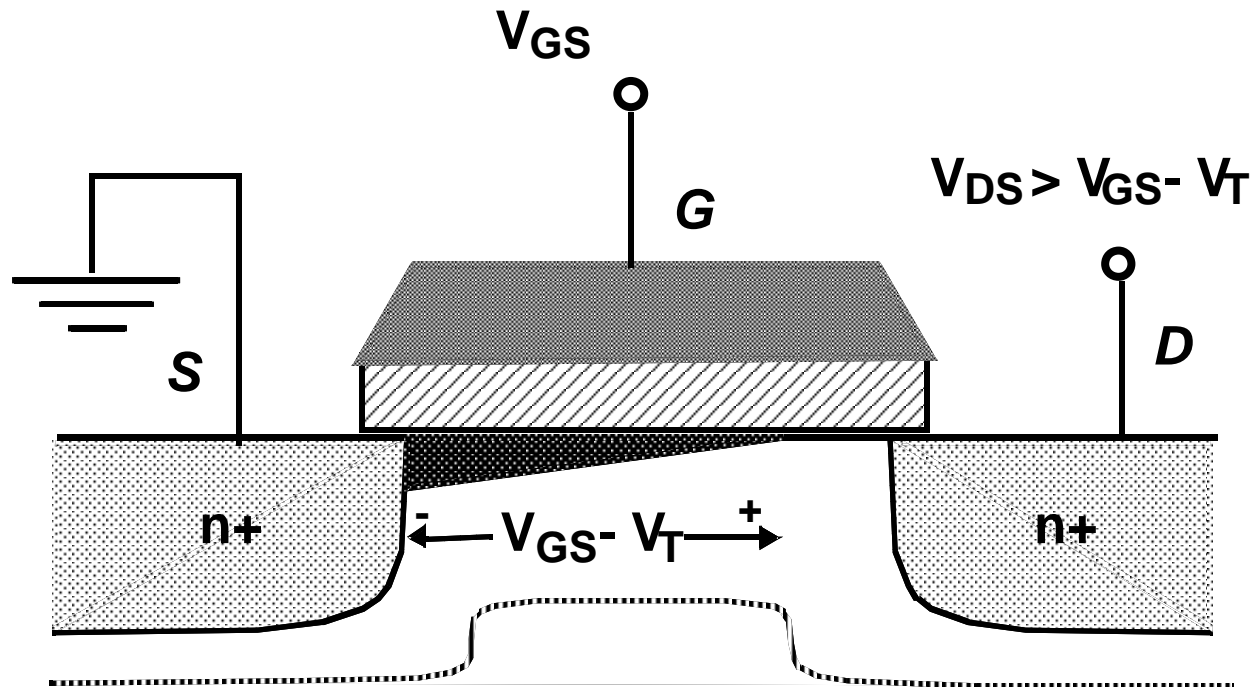
$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

The curve is given by

$$\frac{dI_D}{dV_{DS}} = k \left[(V_{GS} - V_T) - V_{DS} \right] = 0 \Rightarrow V_{DS} = V_{GS} - V_T$$

The value $V_{DS} = V_{GS} - V_T$ is special: it is the boundary between resistive regime and saturation regime (pinch-off)

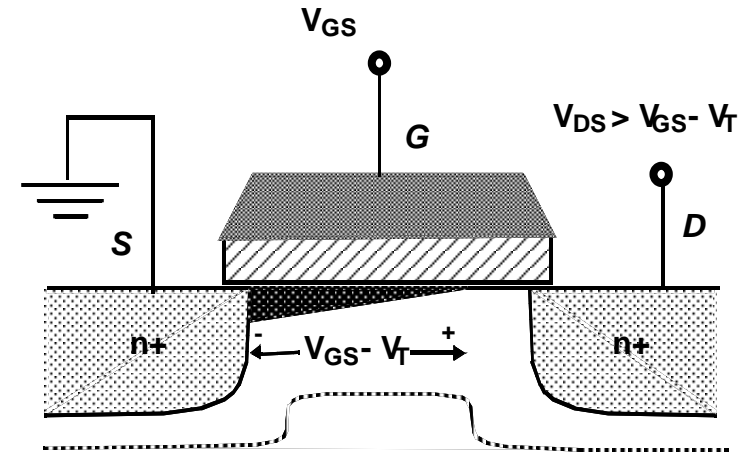
Transistor in Saturation



I-V in saturation

$$V_{DS} < V_{GS} - V_T:$$

$$I_D = k \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$



Saturation: $V_{DS} > V_{GS} - V_T$

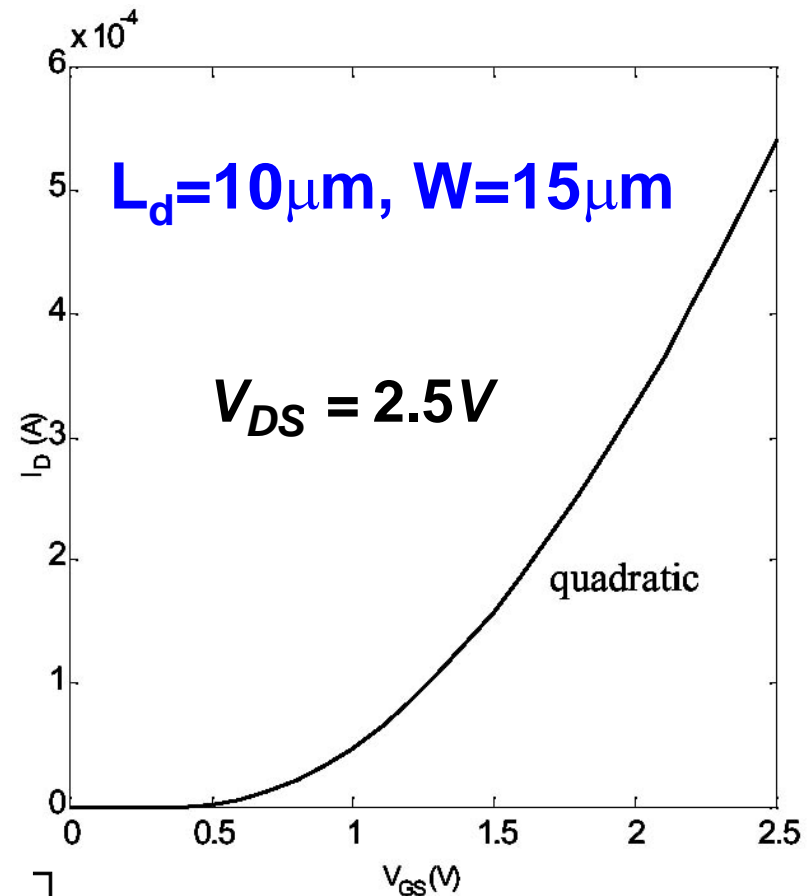
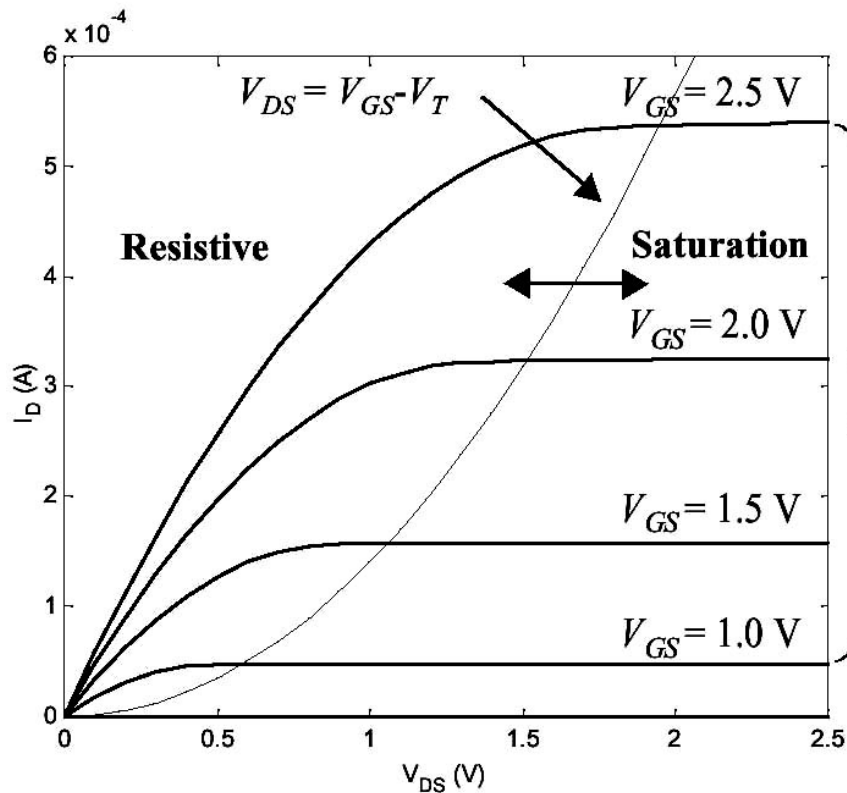
Current does not increase when $V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = I_D \Big|_{V_{DS} = V_{GS} - V_T}$$

Saturation current

$$\begin{aligned} I_{DSAT} &= k \left[(V_{GS} - V_T)(V_{GS} - V_T) - \frac{1}{2}(V_{GS} - V_T)^2 \right] \\ &= \frac{1}{2} k (V_{GS} - V_T)^2 \end{aligned}$$

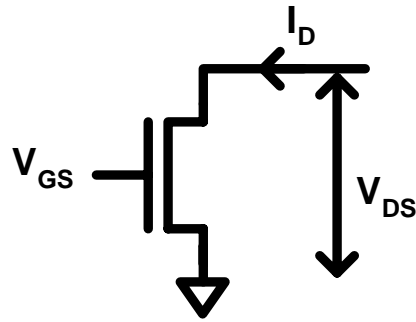
I-V Relation



$$I_D = k \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \quad \text{(resistive regime)}$$

$$= \frac{1}{2}k(V_{GS} - V_T)^2 \quad \text{(saturation)}$$

Output Impedance



Definition: $Z_{out} = \frac{dV_{ds}}{dI_d}$

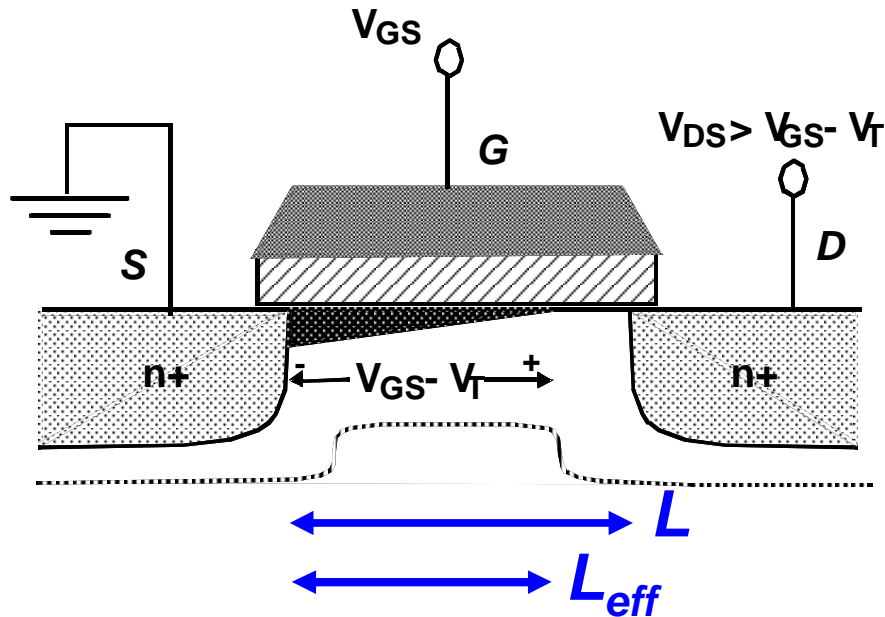
$$I_D = \frac{1}{2} k (V_{GS} - V_T)^2$$

What is the output impedance?

Is this plausible?

What is happening?

Channel Length Modulation



Empirical Model for Effective Channel Length

$$L_{eff} = \frac{L}{1 + \lambda V_{DS}}$$

$$\begin{aligned} I_{DSAT} &= \frac{1}{2} k'_n \frac{W}{L_{eff}} (V_{GS} - V_T)^2 \\ &= \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \\ &= \frac{1}{2} k (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \end{aligned}$$

Velocity Saturation (1)

1. Still model not complete: need to include effects of limited carrier velocity

2. Carrier velocity (ideal model):
Linear with field

$$v_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

4. Simple v_{sat} Model:

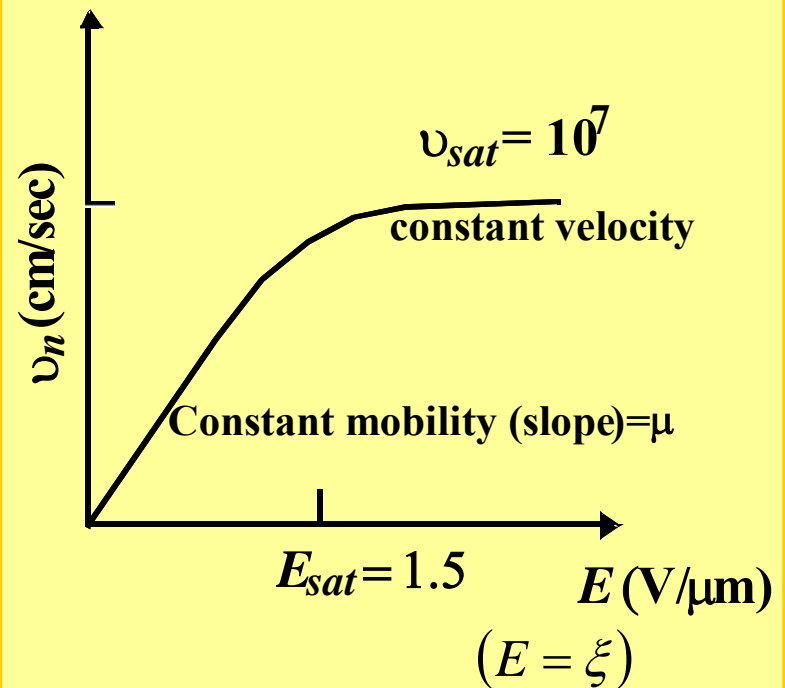
$$v_n = \mu_n \xi \quad \text{for } \xi \leq \xi_c$$

$$= \mu_n \xi_c = v_{sat} \quad \text{for } \xi \geq \xi_c$$

ξ_c **Critical Field**

v_{sat} **Saturation Velocity**

3. Reality



Velocity Saturation (2)

Onset of velocity saturation can be translated into a critical voltage V_{DS} : V_{DSAT} . This value depends on L .

Velocity saturation parameters

$$V_{DSAT} = L \xi_c = \frac{L v_{sat}}{\mu_n}$$

voltage

velocity

L	V_{DSAT}
2	3
1	1.5
0.25	0.375
0.18	0.27
...	...

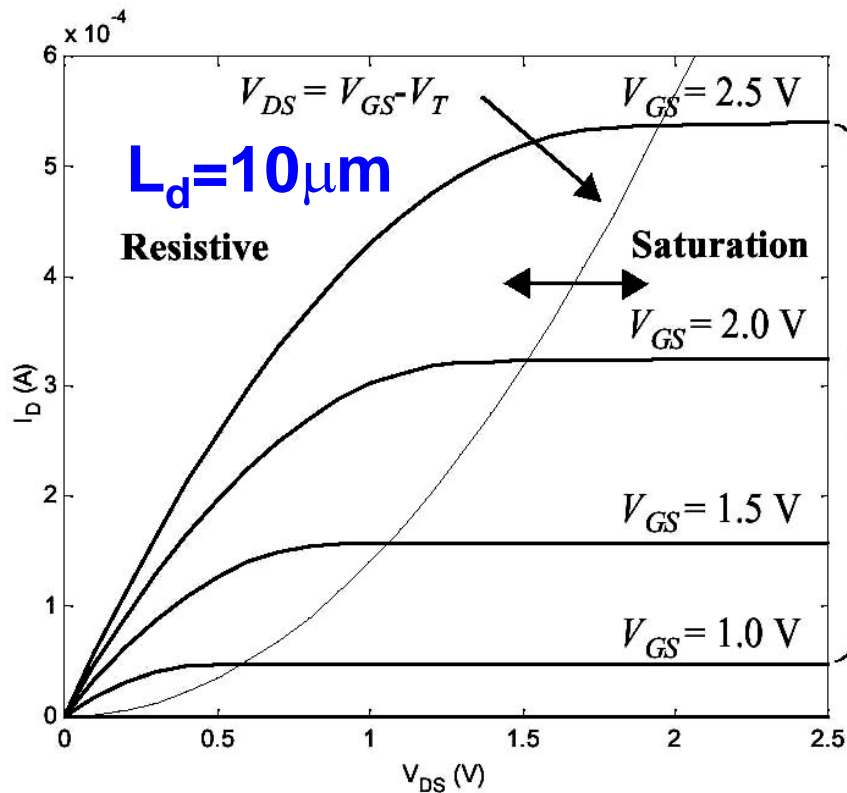
First order, empirical model

$$I_{DSAT} = I_D(V_{DS} = V_{DSAT})$$

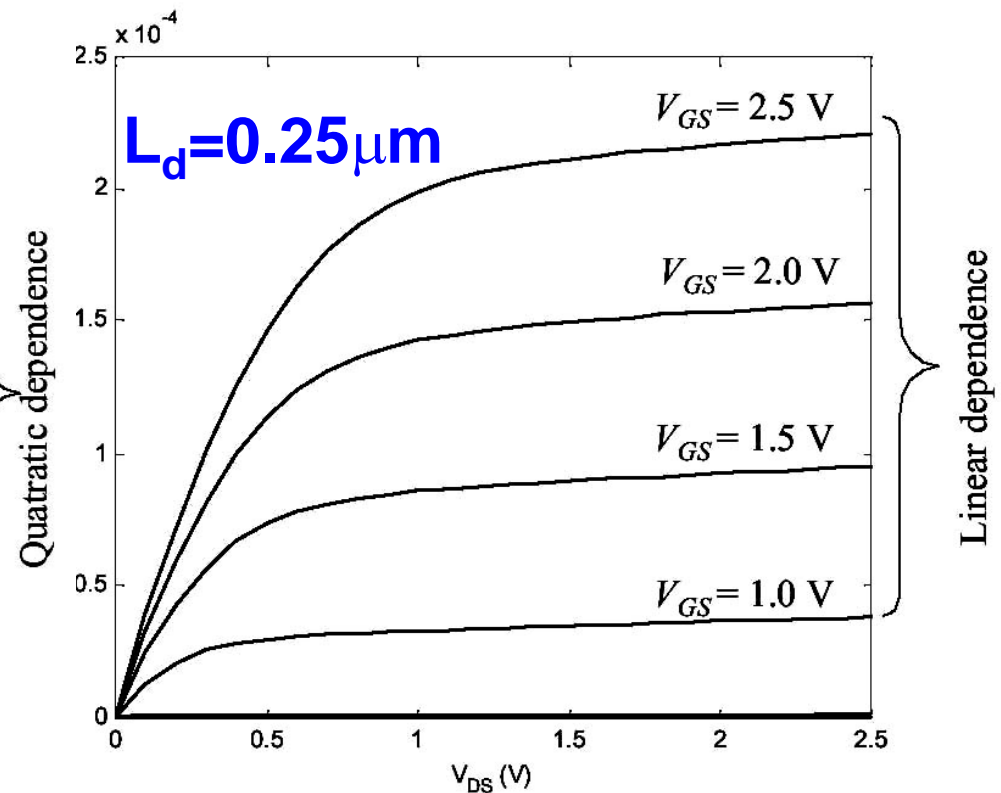
$$= k \left[(V_{GS} - V_T) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 \right]$$

Velocity Saturation

I_D as a function of V_{DS}



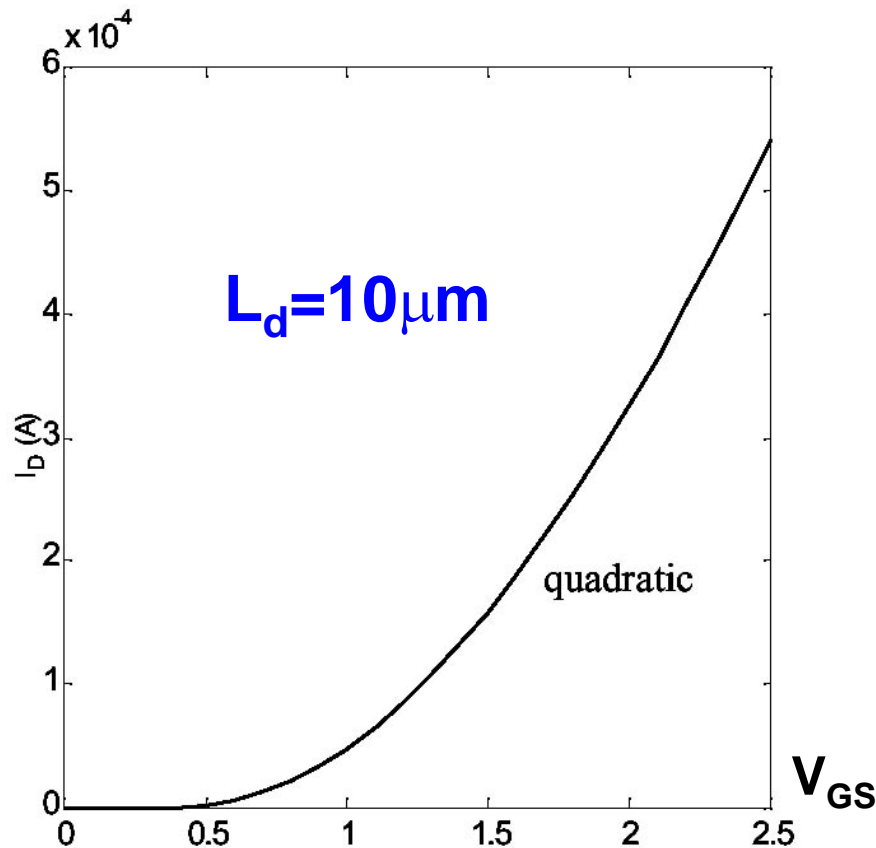
Long channel device w/o velocity saturation



Short channel device with velocity saturation

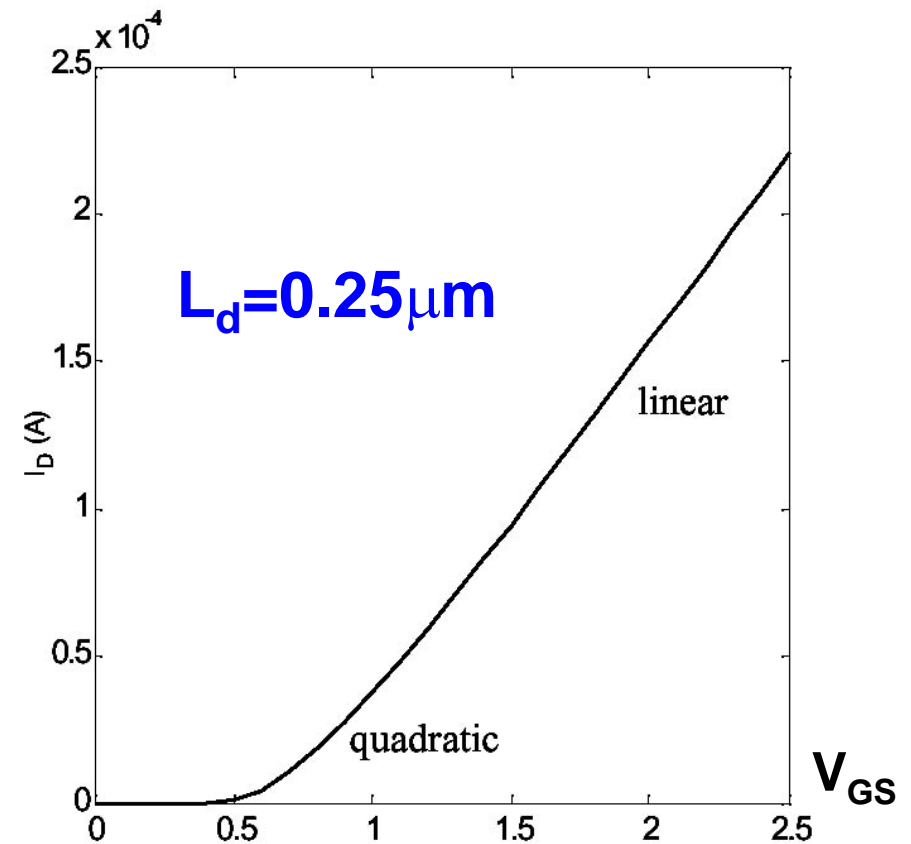
$$W = 1.5L$$

I_D as a function of V_{GS}



Long channel device w/o velocity saturation

$$I_D = \frac{1}{2} k (V_{GS} - V_T)^2$$



Short channel device with velocity saturation

$$I_D = k \left[(V_{GS} - V_T) V_{DSAT} - 0.5 V_{DSAT}^2 \right]$$

Overview

$$I_D' = \begin{cases} k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & \text{resistive regime} \\ & \text{base equation} \\ \\ \frac{1}{2} k (V_{GS} - V_T)^2 & \text{when } V_{DS} > V_{GS} - V_T: \text{ saturation} \\ & \text{replace } V_{DS} \text{ by } V_{GS} - V_T \text{ in base equation} \\ \\ k \left[(V_{GS} - V_T) V_{DSAT} - \frac{1}{2} V_{DSAT}^2 \right] & \text{when } V_{DS} > V_{DSAT}: \text{ velocity saturation} \\ & \text{replace } V_{DS} \text{ by } V_{DSAT} \text{ in base equation} \end{cases}$$

$$I_D = I_D' (1 + \lambda V_{DS})$$

Channel Length Modulation

Smallest of V_{DS} , $V_{GS} - V_T$, V_{DSAT} determines operating region



MOS Models for Manual Analysis

Region Specific Models

$$I'_D = k(V_{GT} V_{DS} - 0.5V_{DS}^2)$$

$$I'_D = k(V_{GT} V_{GT} - 0.5V_{GT}^2)$$

$$I'_D = k(V_{GT} V_{DSAT} - 0.5V_{DSAT}^2)$$

$$I_D = I'_D (1 + \lambda V_{DS})$$

Channel length modulation
added to resistive region, in order
to enforce continuity

Resistive region

Saturation

Velocity Saturation

Channel Length Modulation

Comprehensive model

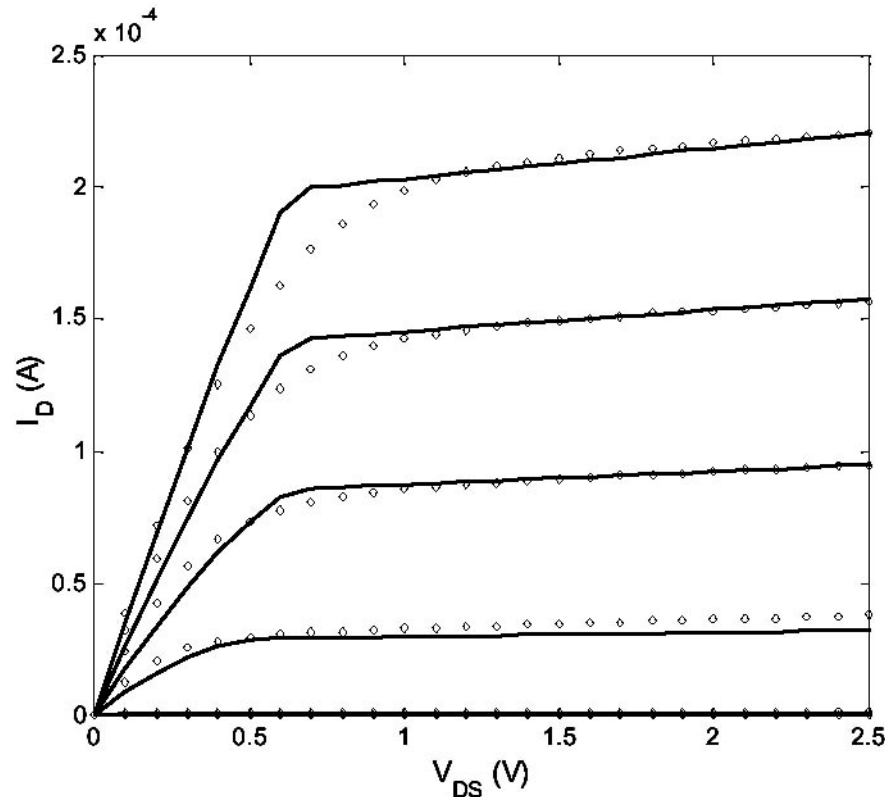
$$I_D = k(V_{GT} V_{MIN} - 0.5V_{MIN}^2)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$

$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = \text{MIN}(V_{DS}, V_{GT}, V_{DSAT})$$

$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

MOS Model Comparison

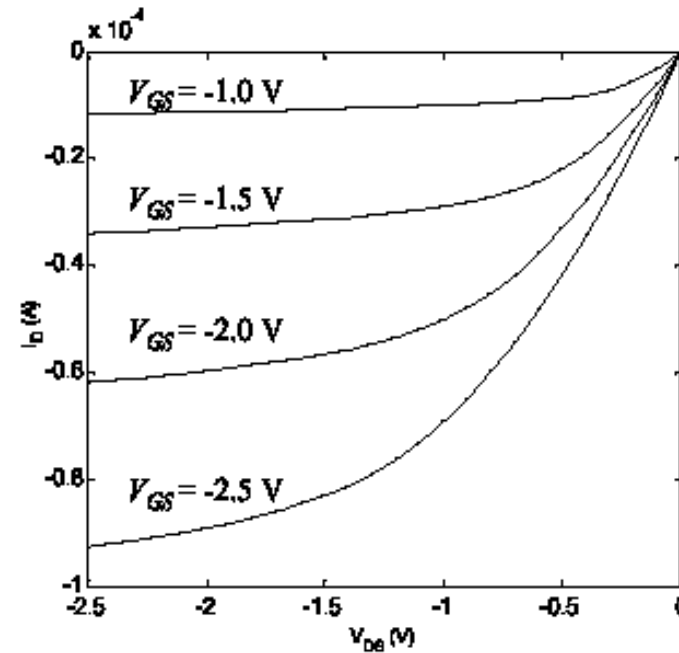
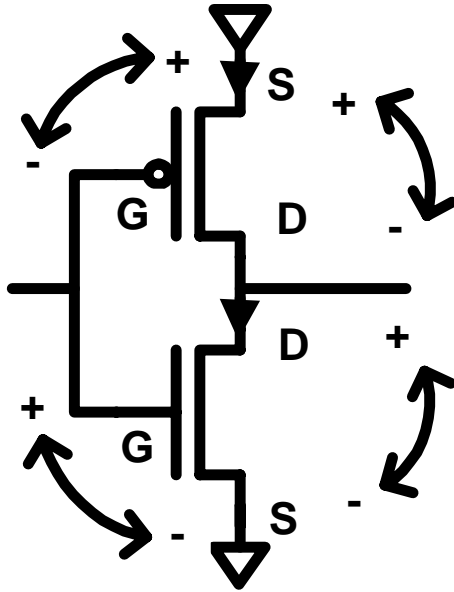


- Many more far more advanced models do exist (BSIM4 ~ 20k lines of C)
- Are only suited for computer simulation
- The SPICE simulator is the 'good old' workhorse of the industry
- Reliable, but low speed

Solid line: simple model

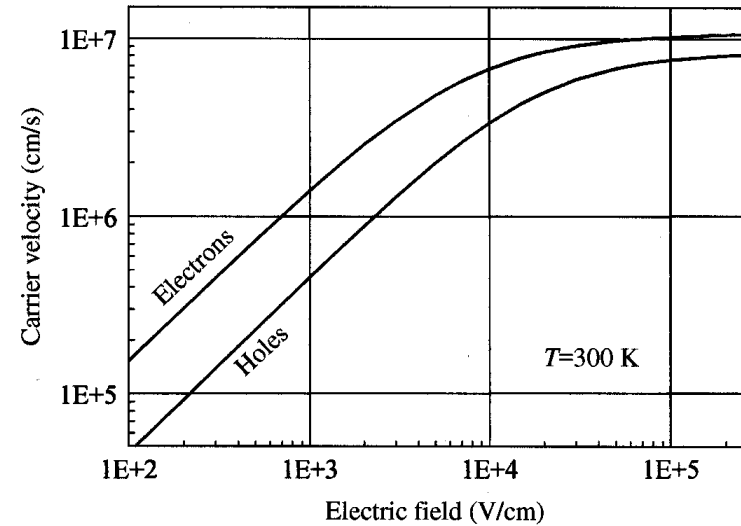
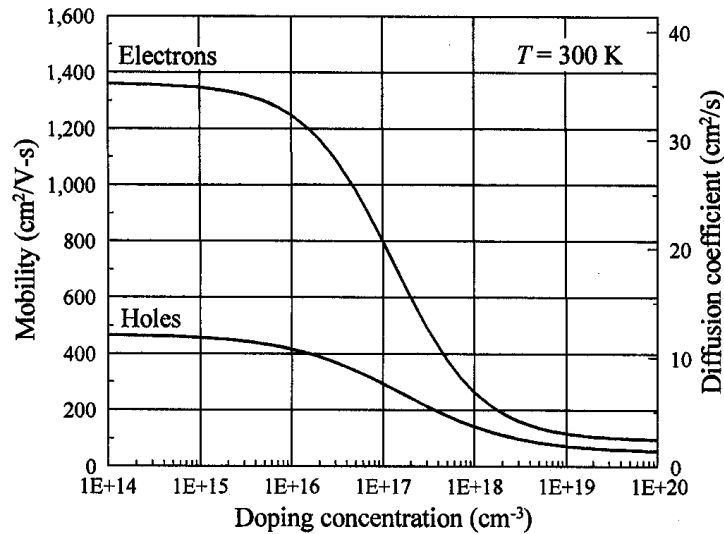
Dotted line: SPICE simulation

NMOS vs. PMOS



- PMOS (V_{DS} , V_{GS} , I_D , V_T) < 0
- Can calculate as if NMOS using absolute values
- PMOS device not as strong as NMOS

NMOS vs. PMOS (2)



Zero-field mobility (bulk!)

Velocity vs. Field

$$\mu_p < \mu_n \Rightarrow k'_p < k'_n \quad \text{👎}$$

$$V_{sat_p} \approx V_{sat_n} \Rightarrow |V_{DSAT_p}| > |V_{DSAT_n}| \quad \text{👍}$$

	V_{T0} (V)	γ (V ^{0.5})	V_{DSAT} (V)	k' (A/V ²)	λ (V ⁻¹)
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

Alternative Saturation Expression

- **Saturation if** $V_{DS} > V_{GS} - V_T$
- **Show that** $V_{DS} > V_{GS} - V_T \Leftrightarrow V_{GD} < V_T$
- **Proof:**
 - $V_{DS} > V_{GS} - V_T$
 - $\Leftrightarrow V_D - V_S > V_G - V_S - V_T$
 - $\Leftrightarrow V_D > V_G - V_T$
 - $\Leftrightarrow V_G - V_T < V_D$
 - $\Leftrightarrow V_G - V_D < V_T$
 - $\Leftrightarrow V_{GD} < V_T$

Physically this relates to 'amount of inversion' at drain side
If inversion at drain side disappears: pinch-off

- **This is an alternative expression for the saturation region**
- **Can be handy**

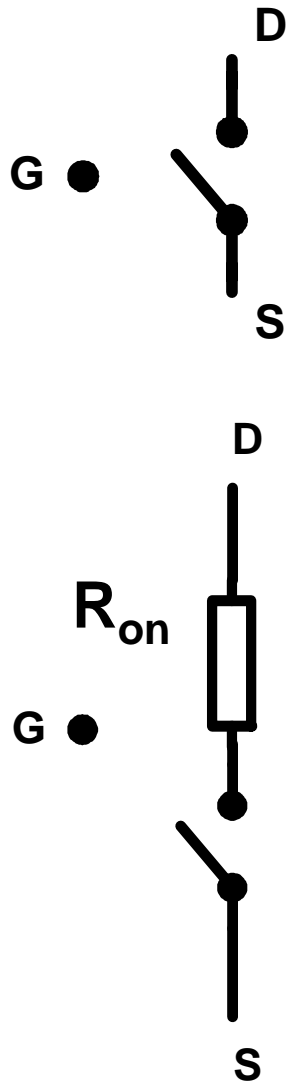
MOS Device Symmetry

- MOS transistors are **symmetrical**
 - Strong inversion at source if $V_{GS} > V_T$
 - Strong inversion at drain if $V_{GD} > V_T$
- } **Independent!**
- **You** should check the I-V relations when interchanging drain and source
 - Identification of source drain only by **convention**
 - Determined by circuit-environment

	NMOS	PMOS	General
Source	V_{SS} -side	V_{DD} -side	Strongest inversion
Drain	V_{DD} -side	V_{SS} -side	Weakest inversion

V_{SS} : low supply voltage, V_{DD} = high supply voltage

Improved MOS Transistor Switch Level Model



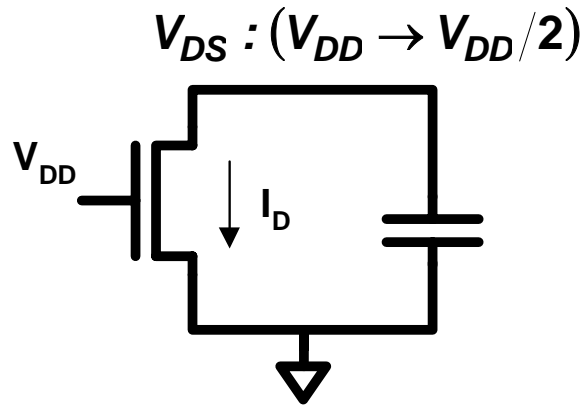
Position of switch depends on gate to source voltage

V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

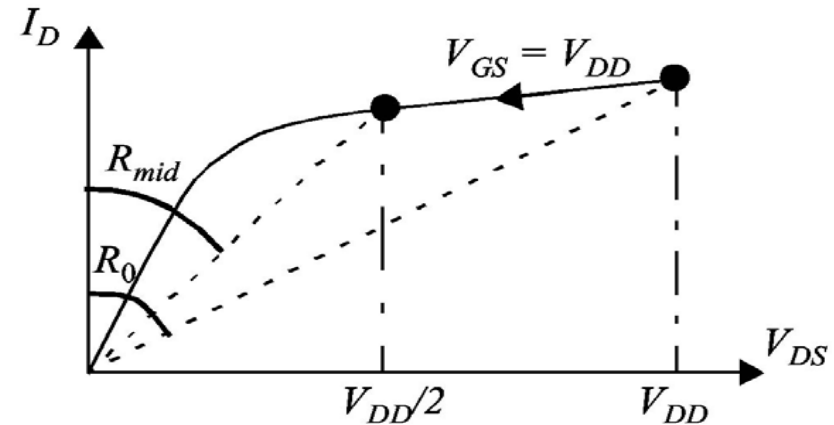
More detailed model may include R_{on}

- R_{on} is highly non-linear
- Make linear approximation R_{eq}
- Model with (linear) R_{eq} less detailed than previous equation based model, but often useful for first estimates of behavior

Switch Model R_{on}



(a) Schematic



(b) trajectory traversed on ID-VDS curve.

$$R_{eq} = \frac{1}{2} \left[\frac{V_{DD}}{I_{DSAT} (1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT} (1 + \lambda V_{DD}/2)} \right]$$

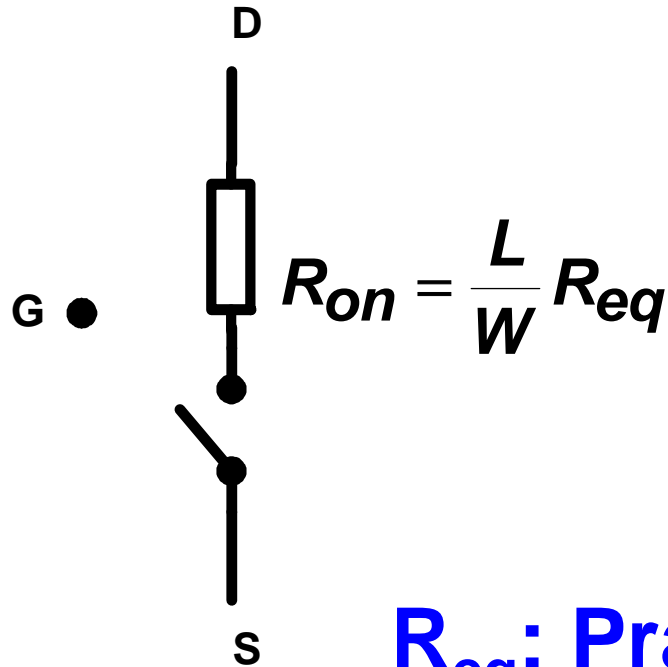
$$\frac{1}{1 + \lambda V_{DD}} \approx 1 - \lambda V_{DD} + O(\lambda^2 V_{DD}^2) \quad \text{2.3\% error with } \lambda = 0.06 \text{ V}^{-1}, V_{DD} = 2.5 \text{ V}$$

$$R_{eq} \approx \frac{1}{2} \frac{V_{DD}}{I_{DSAT}} \left[\left(1 - \lambda V_{DD} + \frac{1}{2} (1 - \lambda V_{DD}/2) \right) \right]$$

$$= \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left[1 - \frac{5}{6} \lambda V_{DD} \right]$$

Theory!

MOS Transistor Switch Level Model (Empirical).



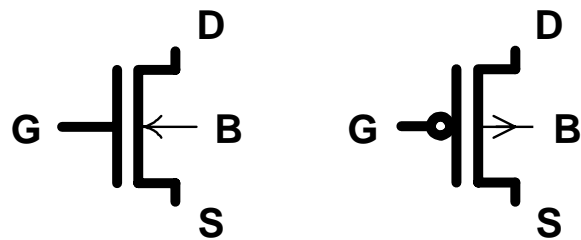
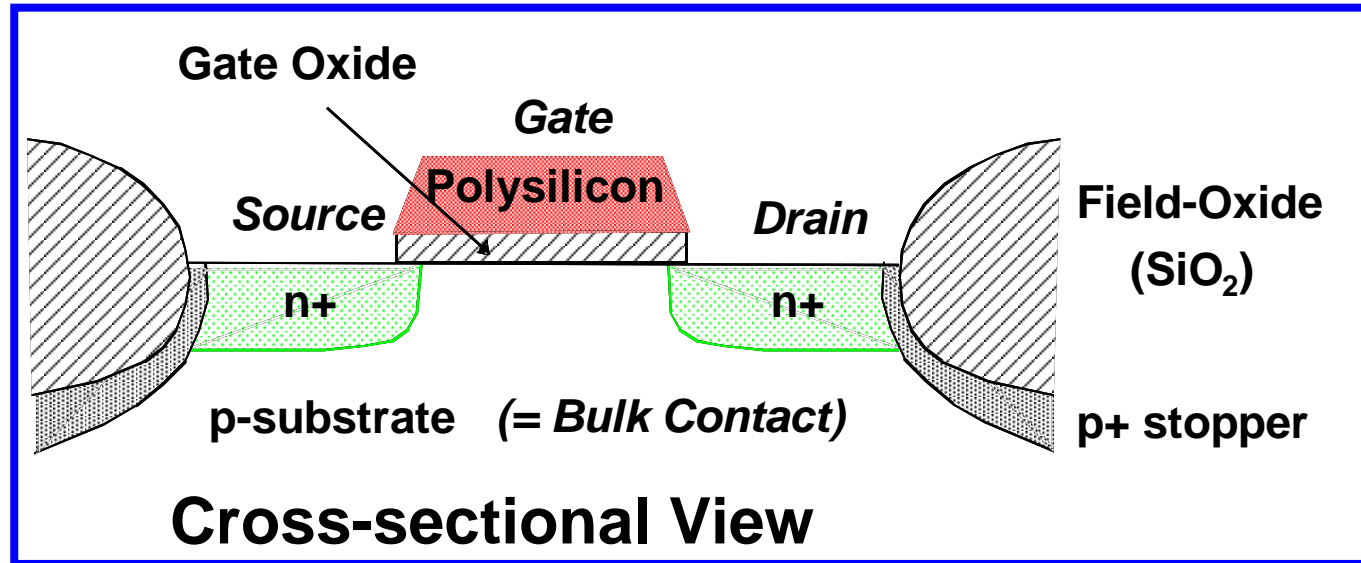
Position of switch depends on gate to source voltage

V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

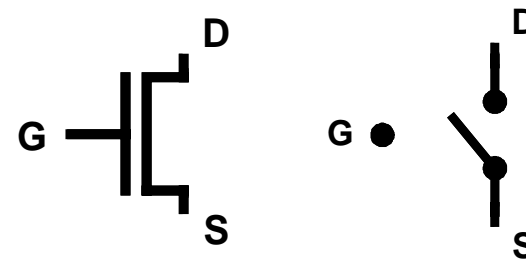
R_{eq} : Practice!

$R_{eq} \setminus V_{dd} (V)$	1	1.5	2	2.5
NMOS (k Ω)	35	19	15	13
PMOS (k Ω)	115	55	38	31

The MOS Transistor Summary



**Schematic symbols,
 very often w/o bulk
 contact**

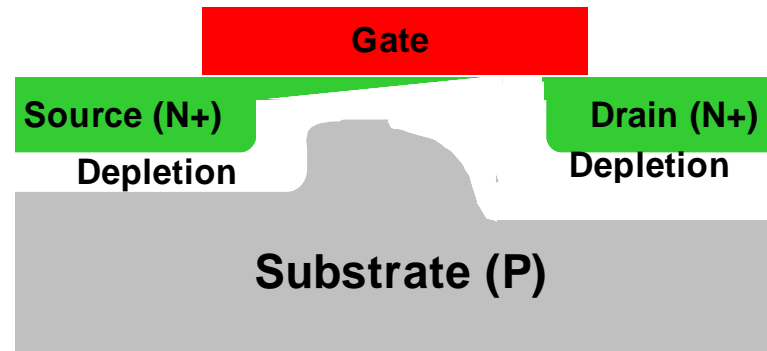


Switch closed if $V_{GS} > V_T$

Simplest possible equiv. ckt.

The MOS Transistor Summary ctd.

- Need to **analyze** speed, power, noise etc of MOS circuits
- Simple switch-level model **not sufficient**
- Study exact operation to derive **more precise IV relations**



$$I_D = k(V_{GT}V_{MIN} - 0.5V_{MIN}^2)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$
$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = \text{MIN}(V_{DS}, V_{GT}, V_{DSAT})$$

$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Summary

- **Semiconductor Physics**
- **The diode**
 - **Depletion, I-V relations, capacitance, secondary effects, models**
- **The MOS transistor**
 - **First glance, threshold, I-V relations, models**
 - **Dynamic behavior (capacitances), resistances, more Second-Order effects, models**