

Chapter 7 PROBLEMS

1. [M, None, 7.4] Figure 1 shows a practical implementation of a pulse register. Clock Clk is ideal with 50% duty cycle.

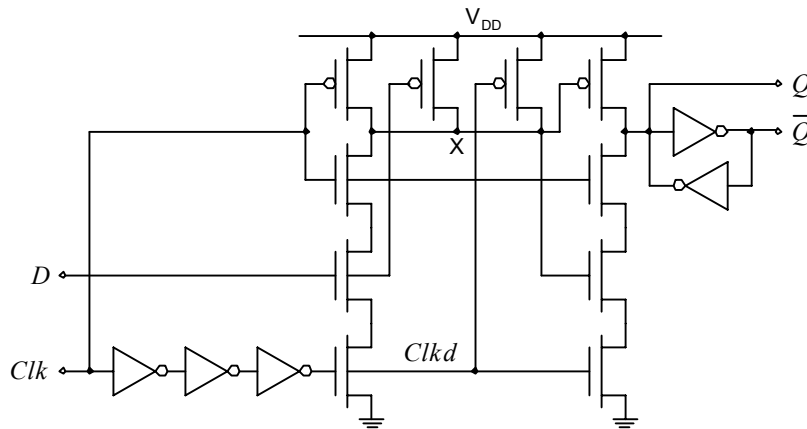


Figure 0.1 Pulse register.

Data : $V_{DD} = 2.5\text{V}$, $t_{p,inv} = 200\text{ps}$, node capacitances are $C_{Clkd} = 10\text{fF}$, $C_x = 10\text{fF}$, both true and complementary outputs node capacitances are 20fF .

- Draw the waveforms at nodes Clk , $Clkd$, X and Q for two clock cycles, with $D = 0$ in one cycle and $D = 1$ in the other.
- What is the approximate value of setup and hold times for this circuit?
- If the probability that D will change its logic value in one clock cycle is α , with equal probability of being 0 or 1, what is the power consumption of this circuit? (exclude the power consumption in the clock line) $f_{clk} = 100\text{ MHz}$.

2. [M, None, 7.4] Figure 2 shows a register that attempts to statistically reduce power consumption using a data-transition look-ahead technique.

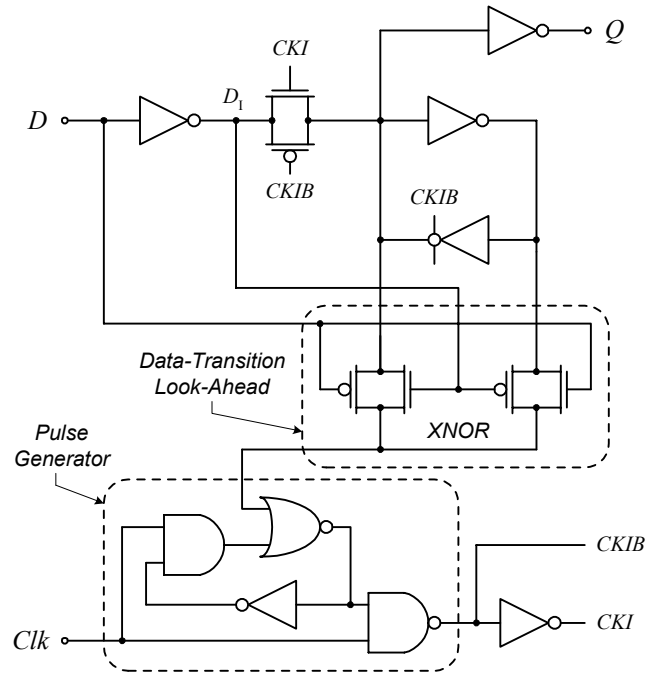


Figure 0.2 Pulse register.

- Briefly describe the operation of the circuit.
 - If all the NMOS transistors are of the same size, and all of the PMOS transistors are of the same size, two times wider than the NMOS, roughly determine the input switching probability under which this flip-flop reduces power, compared to an equivalent flip-flop without data-transition look-ahead circuitry.
3. [E, None, 7.6] Shown in Figure 3 is a novel design of a Schmitt trigger. Determine the W/L ratio of transistor M_1 such that $V_{M^+} = 3V_{Tn}$. $V_{DD} = 2.5\text{V}$. The W/L ratios of other transistors are shown in figure. You may ignore the body effect in this question. The other transistor parameters are as given in Chapter 3.

NMOS: $V_{Tn} = 0.4\text{V}$, $k_n' = 115\mu\text{A}/\text{V}^2$, $V_{DSAT} = 0.6\text{V}$, $\lambda = 0$, $\gamma = 0\text{V}^{1/2}$

PMOS: $V_{Tp} = -0.4\text{V}$, $k_p' = -30\mu\text{A}/\text{V}^2$, $V_{DSAT} = -1\text{V}$, $\lambda = 0$, $\gamma = -0\text{V}^{1/2}$

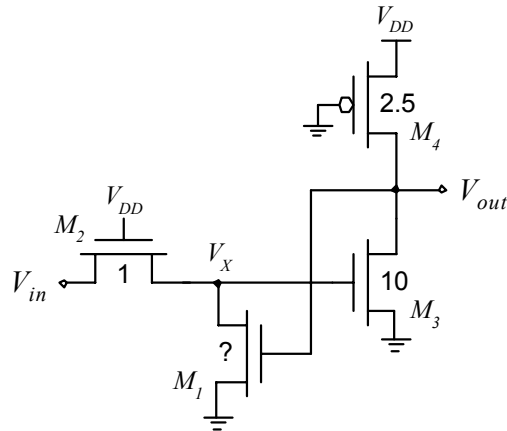


Figure 0.3 Schmitt trigger.

4. [M, None, 7.6] Consider the circuit in Figure 4. The inverter is ideal, with $V_M = V_{DD}/2$ and infinite slope. The transistors have $V_{T-} = 0.4\text{V}$, $k_n' = 120\mu\text{A}/\text{V}^2$ and $k_p' = 40\mu\text{A}/\text{V}^2$. M_1 has $(W/L)_1 = 1$. Ignore all other parasitic effects in the transistors.

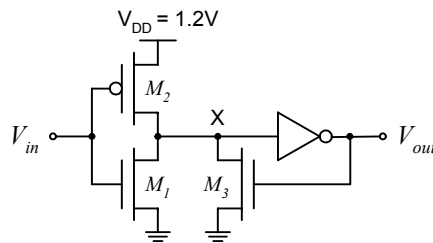


Figure 0.4 Schmitt trigger.

- As V_{IN} goes from 0 to V_{DD} and back to 0 explain the sequence of events which makes this circuit operate as a Schmitt Trigger.
- Find the value of $(W/L)_2$ such that when V_{IN} increases from 0 to V_{DD} the output will switch at $V_{in} = 0.8\text{V}$.
- Find the value of $(W/L)_3$ such that when V_{in} decreases from V_{DD} to 0 the output will switch at $V_{in} = 0.4\text{V}$. If you don't trust your value from b., you may use $(W/L)_2 = 5$.

5. [M, None, 7.6] Figure 5 shows an astable multivibrator. Calculate and draw voltage waveforms at the capacitor V_C and at the output V_{out} . What is the oscillation frequency of the multivibrator?

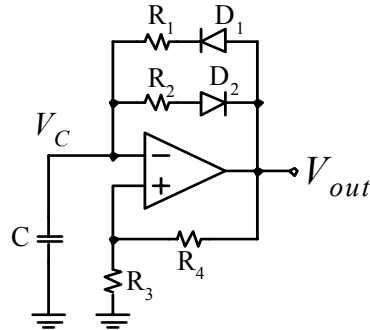


Figure 0.5 Astable multivibrator.

Assume that the amplifier is ideal, with symmetric supplies ($V_{out}^{max} = V_{DD}$, $V_{out}^{min} = -V_{SS}$) $R_1 = 1\text{k}\Omega$, $R_2 = 3\text{k}\Omega$, $R_3 = R_4 = 4\text{k}\Omega$, $C = 1\text{nF}$, $V_{DD} = -V_{SS} = 5\text{V}$, diode voltage $V_D = 0.6\text{V}$ (ideal diode), $V_{out}(t=0) = -V_{SS}$.

6. [E, None, 7.6] An oscillator is shown in Figure 6. Draw the signal waveforms for this circuit at nodes X, Y, Z, A, and B. Determine the oscillation frequency. You may assume that the delay of the inverters, the resistances of the MOS transistors, and all internal capacitors can be ignored. The inverter switch point is set at 1.25V . Assume that nodes Y and Z are initially at 0V and 2.5V , respectively.

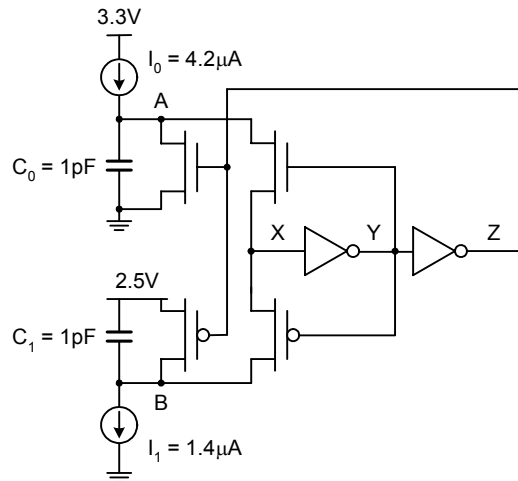


Figure 0.6 Oscillator.

7. [E, None, 7.6] Consider the oscillator in Figure 7. Assume that the “n” switches turn “on” for voltages above $V_{DD}/2$, and the “p” switches turn “on” for voltages below $V_{DD}/2$. Assume that the current sources stop when the node voltage charges to either V_{DD} or ground.

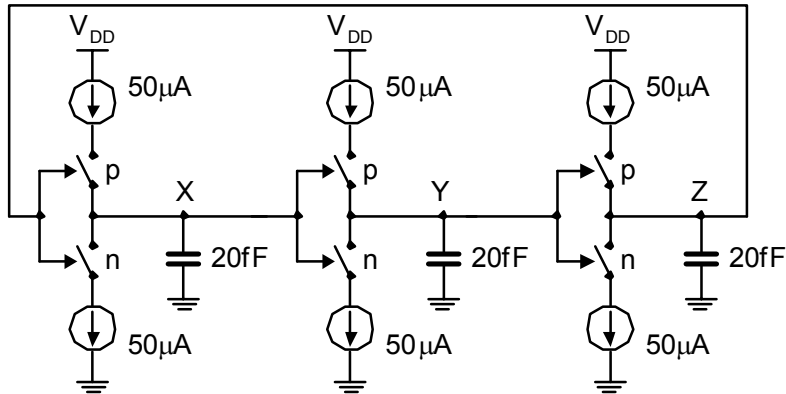


Figure 0.7 Oscillator.

- Find the oscillation period for $V_{DD} = 3V$.
 - Draw the waveforms at nodes X, Y, and Z for two periods.
 - Find the oscillation period.
8. [M, None, 7.6] The circuit in Figure 8 operates at a supply voltage of 3V and uses two Schmitt triggers with the following threshold voltages: $V_{M+} = 2V$, $V_{M-} = 1V$.

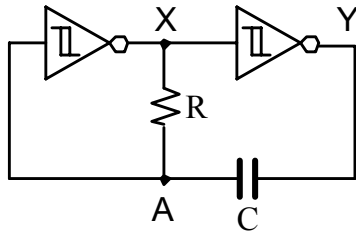


Figure 0.8 A circuit composed of Schmitt triggers.

- Identify whether the circuit is monostable, bistable, or astable?
- Draw the waveforms at nodes X, Y, and A. Mark all important voltage levels.
- Calculate the key timing parameter for this circuit (propagation delay for bistable, pulse width for monostable, and time period for astable) in terms of R and C. You can assume that gate delays are negligible compared to the delay of the RC network.