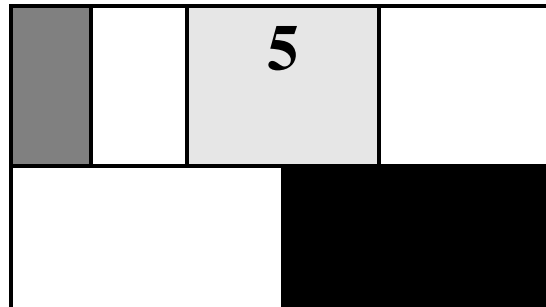


CHAPTER



THE CMOS INVERTER

Quantification of integrity, performance, and energy metrics of an inverter
Optimization of an inverter design

- 5.1 Exercises and Design Problems
- 5.2 The Static CMOS Inverter — An Intuitive Perspective
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5.1 Exercises and Design Problems

1. [M, SPICE, 3.3.2] The layout of a static CMOS inverter is given in Figure 5.1. ($\lambda = 0.125 \mu\text{m}$).
 - a. Determine the sizes of the NMOS and PMOS transistors.
 - b. Plot the VTC (using HSPICE) and derive its parameters (V_{OH} , V_{OL} , V_M , V_{IH} , and V_{IL}).
 - c. Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates?.

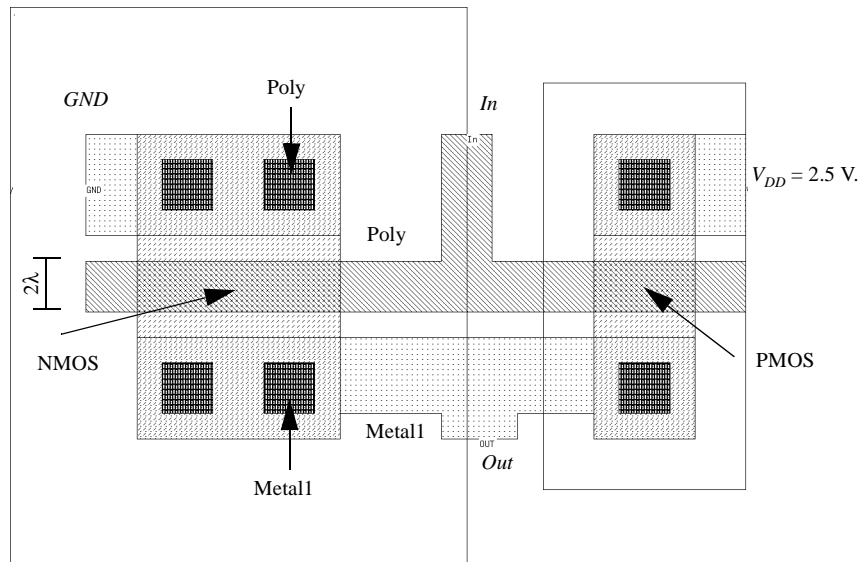


Figure 5.1 CMOS inverter layout.

- d. Resize the inverter to achieve a switching threshold of approximately 0.75 V. Do not layout the new inverter, use HSPICE for your simulations. How are the noise margins affected by this modification?
2. Figure 5.2 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at V_M . The intersection of this line with the V_{OH} and the V_{OL} lines defines V_{IH} and V_{IL} .
 - a. The noise margins of a CMOS inverter are highly dependent on the sizing ratio, $r = k_p/k_n$, of the NMOS and PMOS transistors. Use HSPICE with $V_{tn} = |V_{tp}|$ to determine the value of r that results in equal noise margins? Give a qualitative explanation.
 - b. Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for NM_H and NM_L in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at V_M . For what range of r is this assumption valid? What is the resulting range of V_M ?
 - c. Derive expressions for the inverter gain at V_M for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region: $r_{o,sat} = 1/(\lambda I_D)$.

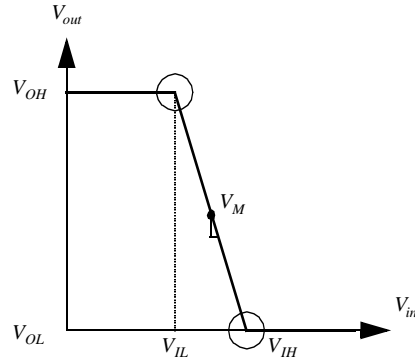


Figure 5.2 A different approach to derive V_{IL} and V_{IH} .

3. [M, SPICE, 3.3.2] Figure 5.3 shows an NMOS inverter with resistive load.
 - a. Qualitatively discuss why this circuit behaves as an inverter.
 - b. Find V_{OH} and V_{OL} calculate V_{IH} and V_{IL} .
 - c. Find NM_L and NM_H , and plot the VTC using HSPICE.
 - d. Compute the average power dissipation for: (i) $V_{in} = 0$ V and (ii) $V_{in} = 2.5$ V

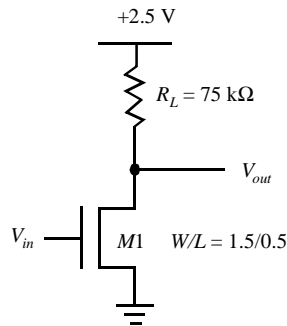


Figure 5.3 Resistive-load inverter

- e. Use HSPICE to sketch the VTCs for $R_L = 37k$, $75k$, and $150k$ on a single graph.
- f. Comment on the relationship between the critical VTC voltages (i.e., V_{OL} , V_{OH} , V_{IL} , V_{IH}) and the load resistance, R_L .
- g. Do high or low impedance loads seem to produce more ideal inverter characteristics?
4. [E, None, 3.3.3] For the inverter of Figure 5.3 and an output load of 3 pF:
 - a. Calculate t_{plh} , t_{phl} , and t_p .
 - b. Are the rising and falling delays equal? Why or why not?
 - c. Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible.
5. The next figure shows two implementations of MOS inverters. The first inverter uses only NMOS transistors.

- a. Calculate V_{OH} , V_{OL} , V_M for each case.

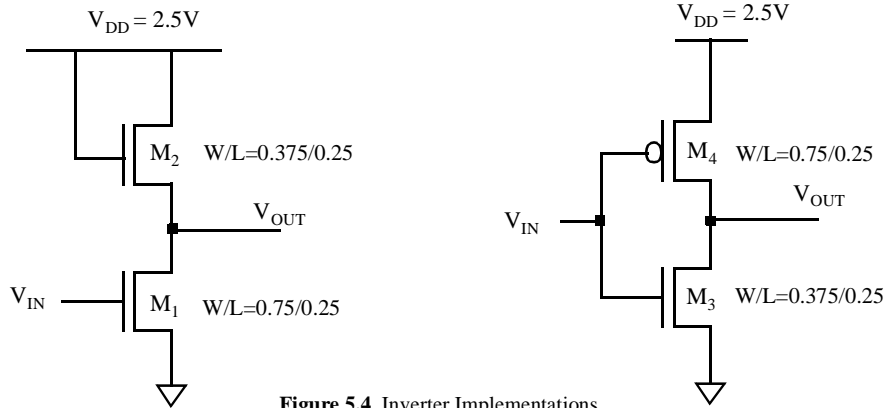
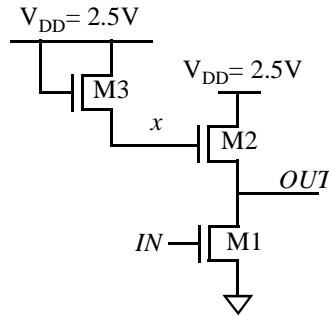


Figure 5.4 Inverter Implementations

- b. Use HSPICE to obtain the two VTCs. You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0.125 \mu\text{m}$, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are $5\lambda \times 5\lambda$.
- c. Find V_{IH} , V_{IL} , NM_L and NM_H for each inverter and comment on the results. How can you increase the noise margins and reduce the undefined region?
- d. Comment on the differences in the VTCs, robustness and regeneration of each inverter.
6. Consider the following NMOS inverter. Assume that the bulk terminals of all NMOS device are connected to GND. Assume that the input IN has a 0V to 2.5V swing.



- a. Set up the equation(s) to compute the voltage on node x . Assume $\gamma=0.5$.
- b. What are the modes of operation of device M2? Assume $\gamma=0$.
- c. What is the value on the output node OUT for the case when $IN=0V$? Assume $\gamma=0$.
- d. Assuming $\gamma=0$, derive an expression for the switching threshold (V_M) of the inverter. Recall that the switching threshold is the point where $V_{IN} = V_{OUT}$. Assume that the device sizes for M1, M2 and M3 are $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ respectively. What are the limits on the switching threshold?

For this, consider two cases:

- i) $(W/L)_1 \gg (W/L)_2$

ii) $(W/L)_2 \gg (W/L)_1$

7. Consider the circuit in Figure 5.5. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of $-0.4V$. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input IN has a $0V$ to $2.5V$ swing.

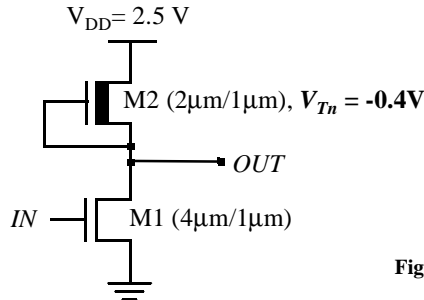


Figure 5.5 A depletion load NMOS inverter

- Device M2 has its gate terminal connected to its source terminal. If $V_{IN} = 0V$, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?
 - Compute the output voltage for $V_{IN} = 2.5V$. You may assume that V_{OUT} is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?
 - Assuming $Pr_{(IN=0)} = 0.3$, what is the static power dissipation of this circuit?
8. [M, None, 3.3.3] An NMOS transistor is used to charge a large capacitor, as shown in Figure 5.6.
- Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to $2.5V$ at the input node.
 - Assume that a resistor R_S of $5\text{ k}\Omega$ is used to discharge the capacitance to ground. Determine t_{pHL} .
 - Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1. How much is dissipated in the pull-down resistance during discharge? How does this change when R_S is reduced to $1\text{ k}\Omega$.
 - The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

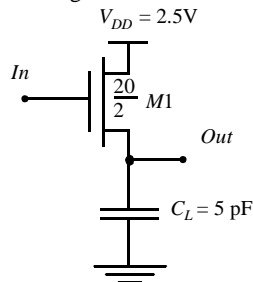


Figure 5.6 Circuit diagram with annotated W/L ratios

9. The circuit in Figure 5.7 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0 . Assume $x_d=0$, $\gamma=0.4$, $2|\phi_f|=0.6V$, $V_{T0}=0.43V$, $k_n'=115\mu A/V^2$ and $\lambda=0$.

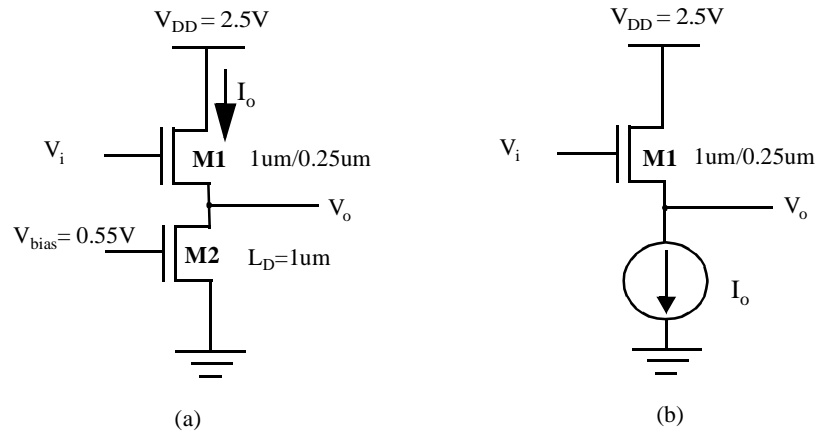


Figure 5.7 NMOS source follower configuration

- a. Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Figure 5.7 (a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate V_i to V_o in terms of I_o).
 - b. Now assume that an ideal current source replaces M2 (Figure 5.7 (b)). The NMOS transistor M1 experiences a shift in V_T due to the backgate effect. Find V_T as a function of V_o for V_o ranging from 0 to 2.5V with 0.5V intervals. Plot V_T vs. V_o .
 - c. Plot V_o vs. V_i as V_o varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter?
 - d. At $V_o(\text{with body effect}) = 2.5\text{V}$, find $V_o(\text{ideal})$ and thus determine the maximum error introduced by the body effect.
10. For this problem assume:
 $V_{DD} = 2.5\text{V}$, $W_p/L = 1.25/0.25$, $W_n/L = 0.375/0.25$, $L=L_{eff}=0.25\mu\text{m}$ (i.e. $x_d=0\mu\text{m}$), $C_L=C_{inv-gate}$, $k_n' = 115\mu\text{A}/\text{V}^2$, $k_p' = -30\mu\text{A}/\text{V}^2$, $V_{m0} = |V_{tp0}| = 0.4\text{V}$, $\lambda = 0\text{V}^{-1}$, $\gamma = 0.4$, $2|\phi_j|=0.6\text{V}$, and $t_{ox} = 58\text{\AA}$. Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gd0} , C_j , C_{jsw}), and assume that $V_{SB}=0\text{V}$ for all problems except part (e).

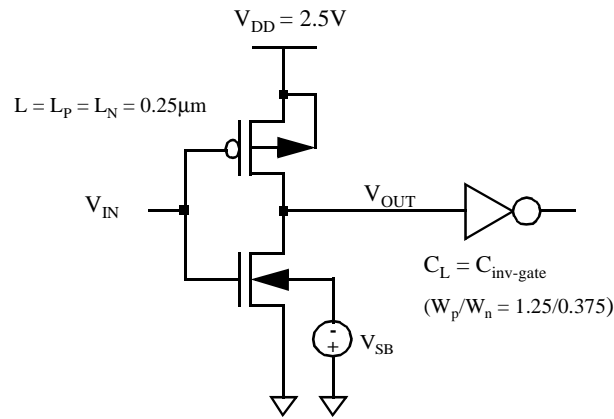


Figure 5.8 CMOS inverter with capacitive

Parasitic Capacitance Parameters (F/m)##

NMOS: $CGDO=3.11 \times 10^{-10}$, $CGSO=3.11 \times 10^{-10}$, $CJ=2.02 \times 10^{-3}$, $CJSW=2.75 \times 10^{-10}$

PMOS: $CGDO=2.68 \times 10^{-10}$, $CGSO=2.68 \times 10^{-10}$, $CJ=1.93 \times 10^{-3}$, $CJSW=2.23 \times 10^{-10}$

- a. What is the V_m for this inverter?
 - b. What is the effective load capacitance C_{Leff} of this inverter? (include parasitic capacitance, refer to the text for K_{eq} and m .) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0.125 \mu\text{m}$, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are $5\lambda \times 5\lambda$.
 - c. Calculate t_{PHL} , t_{PLH} assuming the result of (b) is ' $C_{Leff} = 6.5\text{fF}$ '. (Assume an ideal step input, i.e. $t_{rise}=t_{fall}=0$. Do this part by computing the average current used to charge/discharge C_{Leff} .)
 - d. Find (W_p/W_n) such that $t_{PHL} = t_{PLH}$.
 - e. Suppose we increase the width of the transistors to reduce the t_{PHL} , t_{PLH} . Do we get a proportional decrease in the delay times? Justify your answer.
 - f. Suppose $V_{SB} = 1\text{V}$, what is the value of V_m , V_{tp} , V_m ? How does this qualitatively affect C_{Leff} ?
11. Using Hspice answer the following questions.
- a. Simulate the circuit in Problem 10 and measure t_p and the average power for input V_{in} : `pulse(0 VDD 5n 0.1n 0.1n 9n 20n)`, as V_{DD} varies from 1V - 2.5V with a 0.25V interval. [$t_p = (t_{PHL} + t_{PLH}) / 2$]. Using this data, plot ' t_p vs. V_{DD} ', and ' $\text{Power vs. } V_{DD}$ '.
Specify AS, AD, PS, PD in your spice deck, and manually add $C_L = 6.5\text{fF}$. Set $V_{SB} = 0\text{V}$ for this problem.
 - b. For Vdd equal to 2.5V determine the maximum fan-out of identical inverters this gate can drive before its delay becomes larger than 2 ns.
 - c. Simulate the same circuit for a set of 'pulse' inputs with rise and fall times of $t_{in_rise,fall} = 1\text{ns}, 2\text{ns}, 5\text{ns}, 10\text{ns}, 20\text{ns}$. For each input, measure (1) the rise and fall times t_{out_rise} and

t_{out_fall} of the inverter output, (2) the total energy lost E_{total} , and (3) the energy lost due to short circuit current E_{short}

Using this data, prepare a plot of (1) $(t_{out_rise}+t_{out_fall})/2$ vs. $t_{in_rise,fall}$, (2) E_{total} vs. $t_{in_rise,fall}$, (3) E_{short} vs. $t_{in_rise,fall}$ and (4) E_{short}/E_{total} vs. $t_{in_rise,fall}$.

- d. Provide simple explanations for:
- (i) Why the slope for (1) is less than 1?
 - (ii) Why E_{short} increases with $t_{in_rise,fall}$?
 - (iii) Why E_{total} increases with $t_{in_rise,fall}$?
12. Consider the low swing driver of Figure 5.9:

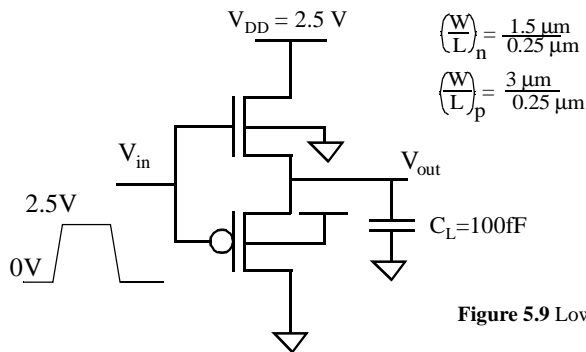


Figure 5.9 Low Swing Driver

- a. What is the voltage swing on the output node (V_{out})? Assume $\gamma=0$.
 - b. Estimate (i) the energy drawn from the supply and (ii) energy dissipated for a 0V to 2.5V transition at the input. Assume that the rise and fall times at the input are 0. Repeat the analysis for a 2.5V to 0V transition at the input.
 - c. Compute t_{pLH} (i.e. the time to transition from V_{OL} to $(V_{OH} + V_{OL})/2$). Assume the input rise time to be 0. V_{OL} is the output voltage with the input at 0V and V_{OH} is the output voltage with the input at 2.5V.
 - d. Compute V_{OH} taking into account body effect. Assume $\gamma = 0.5V^{1/2}$ for both NMOS and PMOS.
13. Consider the following low swing driver consisting of NMOS devices M1 and M2. Assume an NWELL implementation. Assume that the inputs IN and \overline{IN} have a 0V to 2.5V swing and that $V_{IN} = 0V$ when $V_{\overline{IN}} = 2.5V$ and vice-versa. Also assume that there is no skew between IN and \overline{IN} (i.e., the inverter delay to derive \overline{IN} from IN is zero).

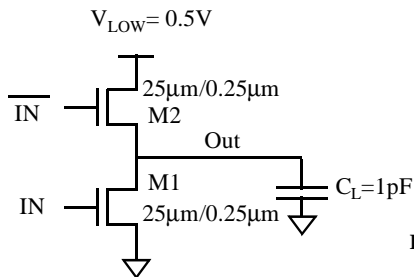
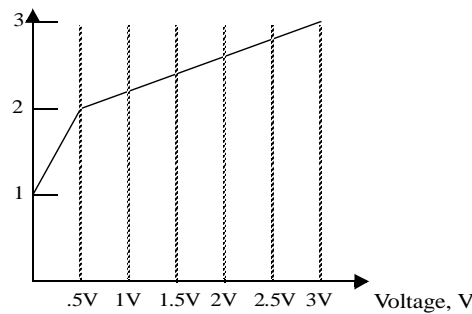


Figure 5.10 Low Swing Driver

- a. What voltage is the bulk terminal of M2 connected to?

- b. What is the voltage swing on the output node as the inputs swing from 0V to 2.5V. Show the low value and the high value.
- c. Assume that the inputs \overline{IN} and $\overline{\overline{IN}}$ have zero rise and fall times. Assume a zero skew between \overline{IN} and $\overline{\overline{IN}}$. Determine the low to high propagation delay for charging the output node measured from the 50% point of the input to the 50% point of the output. Assume that the total load capacitance is 1pF, including the transistor parasitics.
- d. Assume that, instead of the 1pF load, the low swing driver drives a non-linear capacitor, whose capacitance vs. voltage is plotted below. Compute the energy drawn from the low supply for charging up the load capacitor. Ignore the parasitic capacitance of the driver circuit itself.



14. The inverter below operates with $V_{DD}=0.4V$ and is composed of $|V_t|=0.5V$ devices. The devices have identical I_0 and n .
- a. Calculate the switching threshold (V_M) of this inverter.
- b. Calculate V_{IL} and V_{IH} of the inverter.

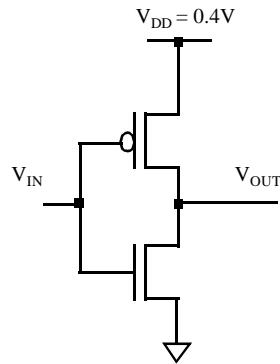


Figure 5.11 Inverter in Weak Inversion Regime

15. Sizing a chain of inverters.
- a. In order to drive a large capacitance ($C_L = 20$ pF) from a minimum size gate (with input capacitance $C_i = 10$ fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume

that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

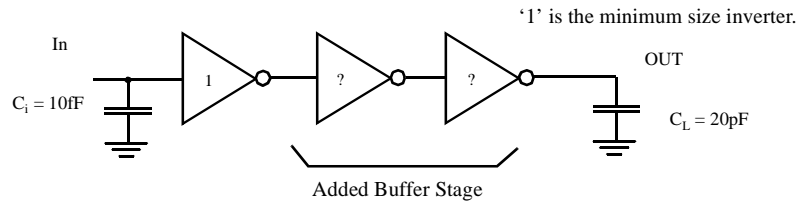


Figure 5.12 Buffer insertion for driving large loads.

- b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?
 - c. Describe the advantages and disadvantages of the methods shown in (a) and (b).
 - d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?
- 16.** [M, None, 3.3.5] Consider scaling a CMOS technology by $S > 1$. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.
- a. In traditional constant voltage scaling, transistor widths scale inversely with S , $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for W . What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).
 - b. How does delay scale under this new methodology?
 - c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

DESIGN PROBLEM

Using the 0.25 μm CMOS introduced in Chapter 2, design a static CMOS inverter that meets the following requirements:

1. Matched pull-up and pull-down times (i.e., $t_{pHL} = t_{pLH}$).
2. $t_p = 5$ nsec (± 0.1 nsec).

The load capacitance connected to the output is equal to 4 pF. Notice that this capacitance is substantially larger than the internal capacitances of the gate.

Determine the W and L of the transistors. To reduce the parasitics, use minimal lengths ($L = 0.25 \mu\text{m}$) for all transistors. Verify and optimize the design using SPICE after proposing a first design using manual computations. Compute also the energy consumed per transition. If you have a layout editor (such as MAGIC) available, perform the physical design, extract the real circuit parameters, and compare the simulated results with the ones obtained earlier.