ET1205 D2 Elektronische Circuits
Onderdeel Geintegreerde Schakelingen

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Inhoud

Syllabus Elektronische Schakelingen
Onderdeel Geïntegreerde Systemen ET1205-D2
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Inleiding

Website: cas.et.tudelft.nl/~nick/courses/gs. Bevat laatste informatie, kopieën van de slides, verwijzingen naar relevante web-sites, etc. Aankondigingen komen op Blackboard, beide sites verwijzen naar elkaar. Er is ook een website die bij het boek hoort, zie het boek of de GS en blackboard sites.

Nota Bene 1

Het boek wat bij deze cursus hoort is de tweede editie (met groen-gele voorkant) van Rabaey, uitgave 2003. Hieronder kortweg aangegeven met “Rabaey” of “het boek”.

Nota Bene 2

Deze syllabus is bedoeld om samen met het web (bovengenoemde site, en Blackboard) gebruikt te worden. Blijf kijken op het web voor de nieuwste informatie, tot vlak voor het tentamen! Registreer je ook voor de cursus op BB, op die manier kun je o.a. de e-mail krijgen die eventueel verstuurd kan worden.

1. Hoe te studeren

Hoe word ik een succesvol (GS) student:

- **Bedenk dat de studielast te groot is om pas tijdens de witte weken te bestuderen**. Je kunt alleen succesvol zijn op het tentamen als je de stof bijhoudt tijdens het college. Maak de oefeningen en de toetsen/tentamens van voorgaande jaren. En vraag hulp als je er niet uitkomt. Hier kun je de instructie op vrijdag voor gebruiken.

- **Weet dat ES geen gemakkelijk vak is.**
  Dat komt niet zozeer door de hoeveelheid stof, of de ingewikkeldheid van de begrippen. Nee, bij ES worden bij de toetsen/tentamens ook vaardigheden verwacht op een hoger niveau. Naast toepassen van kennis (sommetjes maken) wordt ook verwacht dat je tot op zekere hoogte verbanden kan zien in de gepresenteerde stof en deze kan analyseren, en dat je concepten kunt combineren en generaliseren. Je kunt deze vaardigheden alleen ontwikkelen door voldoende tijd te investeren.

- **Het tentamen is gesloten-boek met ‘cheat sheet’ (spiekbriefje).**
  De tentamens/toetsen zullen meer op inzicht toetsen dan op weetjes. De hoofdbegrippen moeten gekend en begrepen worden. In deze syllabus staat voor ieder onderdeel een checklist/samenvatting van deze begrippen. De details hoeven niet onthouden te worden, die kun je noteren op je cheat sheet. Die maak je zelf, maar niet alles zal er op passen. Je kunt de cheat sheet pas effectief maken (en gebruiken) als je

de hoofdbegrippen kent en begrijpt! De formules uit Rabaey van de voorflap en achterflap worden beschikbaar gesteld.

- **Gebruik de studeerhandleiding en voor GS deze syllabus. Gebruik het web. Gebruik het forum.**
  Deze vormen de ***ontsluiting van het studiemateriaal***, een wegwijzer bij de zelfstudie. Op blackboard (blackboard.tudelft.nl) worden aankondigingen en documenten voor ES gepubliceerd. Op blackboard is ook een discussieforum. Er is een aparte site voor GS (cas.et.tudelft.nl/~nick/courses/gs). Blackboard en deze site zijn via elkaar te bereiken. Kijk hier regelmatig, ten minste een of twee keer per week.

- **Weet dat het volgen van de colleges niet toereikend is voor een goed resultaat.**
  Je moet ***zelf studeren***: lezen, herlezen, (proberen te) begrijpen, samenvattingen maken, oefeningen maken, meedenken, ***verbanden leggen***, formules narekenen, schematische overzichten maken, etc. Studeren is een werkwoord. Het college geeft ook geen 100% dekking van de stof, bepaalde zaken kunnen overgeslagen worden om meer aandacht te geven aan andere. Het college presenteert ook vaak andere invalshoeken en verbanden die niet (duidelijk) in het studiemateriaal staan. Deze werken pas echt voor je als je tussen de colleges door de stof bijhoudt, en liefst ook vooruit leest.

- **Wees actief tijdens de colleges: denk zelf en denk mee.**
  De docent weet het wel, hopelijk komt z'n verhaal een beetje logisch over. Dat is gevaarlijk: het lijkt dan gemakkelijk terwijl het misschien juist moeilijk is. Doe serieus mee met de vragen die de docent stelt en de opdrachten die hij geeft. Wees niet bang om een fout antwoord te geven: dat hoort bij leren en is dus normaal.

- **Wees zelf verantwoordelijk voor je voortgang.**
  Zoek geen uitvluchten, bijvoorbeeld gebaseerd op gebrekkig studiemateriaal, late of slechte informatie, de Nederlandse Spoorwegen of de Delftse kamernood of <vul zelf aan>. Er zijn genoeg manieren om feedback te geven (o.a. het forum) en maak daar gebruik van. Wij willen heel graag van jullie leren hoe wij het onderwijs kunnen verbeteren. Laat dat echter geen excuus zijn voor 'niet willen roeien met de riemen die je hebt'. Zo slecht is het allemaal vast niet.

- **Houd je aan de volgende top drie:**

  1. zelf studeren
  2. zelf studeren
  3. zelf studeren

  De rest van de top tien kun je zelf samenstellen aan de hand van deze syllabus.

2. Oefeningen

Er zijn diverse bronnen voor oefeningen:

1. De oefeningen op de college-sheets
2. De oefeningen die losbladig uitgedeeld werden om te maken tijdens het college. Ze worden gebundeld in de reader. Deze oefeningen zijn verder ook (als pdf) te vinden op de GS website.
3. De oefenopgaven die bij het boek horen, op de Rabaey website (met een kopie op de GS website). Bij de verschillende onderdelen hieronder wordt aangegeven wat geschikte oefeningen van de Rabaey set zijn.
4. De 'problems' uit het boek. Deze hebben een uitwerking achterin het boek. Ook hiernaar wordt verwezen in de beschrijvingen per hoofdstuk hieronder.
5. Oude tentamenopgaven. Er zijn veel oude tentamens te vinden op de GS website, in principe allemaal met uitwerkingen.

3. Te bestuderen stof

3.1. Globaal

Het college wordt opgedeeld in 10 modules. Dit wordt samengevat in onderstaande tabel, waarbij de laatste kolom een grof overzicht geeft van de bijbehorende stof uit de gedrukte tweede editie van het boek van Rabaey met groen-gele voorkant.

Module	**Datum**	**Titel**	**BOEK**
0		Introduction	1.1, 1.2, 1.4
1		Devices	3.1 – 3.3 niet 3.3.4, 3.3.5
2		Process	Chapter 2 (gedeeltelijk)
3		Interconnect	4.1 – 4.5, niet 4.3.3, 4.4.5, 4.5.2
4		Inverter	5.1 – 5.5
5		Combinational	6.1 – 6.3 (gedeeltelijk)
6		Sequential	7.1 – 7.4, 7.9
7		Timing	10.1, 10.3, 7.5 (alles gedeeltelijk)
8		Modularity	Chapter 11 (gedeeltelijk)

3.2. Gedetailleerd

Ter wille van de bestudering van de stof zullen wij het materiaal uit het boek in drie categorieën indelen.

Primair – bevat relevante informatie t.a.v. de leerdoelen van het vak.

Illustratie – deze stukjes combineren kennis van verschillende onderwerpen en tonen consequenties, mogelijkheden en/of maatregelen ter optimalisatie van bepaalde eigenschappen. Eventueel nieuwe toegevoegde kennis/theorie behoort in principe niet tot de leerdoelen.

Overslaan – geeft nieuwe kennis die buiten de leerdoelen valt.

De stukjes die als illustratie benoemd worden, kunnen bij een eerste bestudering wellicht overgeslagen worden, maar vormen aan de andere kant zeker een goede voorbereiding op de toetsen/tentamens en zijn behulpzaam bij het verdiepen van je inzicht m.b.t. dit vak in het algemeen. De werkwijzen zoals gepresenteerd in de illustraties horen echter uitdrukkelijk wel tot de leerdoelen, en zijn misschien zelfs wel het belangrijkste, niet alleen voor dit vak maar voor je ontwikkeling tot ingenieur in het algemeen. In principe zijn de meeste "Examples" ook illustratie, maar worden meestal niet expliciet zo benoemd.

Voor sommige onderdelen van het vak, wanneer het boek voor ons doel te diep op de stof ingaat, bevatten deze syllabus en de ppt slides alternatieve beschrijvingen en werkwijzen. Deze alternatieve stof behoort tot de primaire informatie t.a.v. de leerdoelen van het vak.

Ook dient opgemerkt te worden dat grens tussen en "primair" en "illustratie" enerzijds en "illustratie" en "overslaan" anderzijds soms enigszins arbitrair is, zodat het bijvoorbeeld voor kan komen dat in " illustratie" toch enige nieuwe informatie t.a.v. de leerdoelen voorkomt.

Ten slotte dient opgemerkt te worden dat "illustratie" of "overslaan" niet inhoudt dat er geen toets/tentamen vraag gesteld kan worden over een zo geclassificeerd onderwerp. Vragen kunnen juist wel geïnspireerd zijn op iets wat als "illustratie" of soms ook als "overslaan" staat of had kunnen staan. De bedoeling van de vraag is dan dat je laat zien dat je genoeg inzicht hebt om bepaalde 'nieuwe' dingen te doen met de stof.

In het vervolg van deze studeerhandleiding zullen leeswijzers gegeven worden, die in tabelvorm de "primair", "illustratie" en "overslaan" onderdelen aangeven met respectievelijk **P, I** en **O**. Deze leeswijzers worden in principe alleen gegeven voor de modules waar significante aansluitende stukken uit het boek de classificatie **I** of **O** krijgen.

3.3. Samenvatting

De samenvatting die bij de verschillende modules gegeven worden, kun je gebruiken als check-list voor je zelfstudie.

3.4. Oefeningen

- Sommige aanwijzingen hieronder zullen je niets zeggen voordat je de stof bestudeerd hebt. Dit is geen probleem, sla het in eerste instantie over en lees het wanneer je eraan toe bent.

- Oefeningen kun je vinden via de website van het boek, verder in deze syllabus wordt aangegeven welke oefeningen in het bijzonder relevant zijn.

- Zelf bepalen of je een oefening kunt doen, is al een goede oefening op zich.

- **Meestal zul je wel weten wanneer je een opgave begrijpt en wanneer je hem goed gemaakt hebt. Als je twijfelt, is dat een reden om de stof nog eens te bestuderen. Als je er dan nog niet uitkomt, is dat een reden om navraag te doen, bij de docent of op het forum.**

- In de tabellen die gegeven worden bij de verschillende modules volgen enkele suggesties voor opgaven. Cq refereert aan hoofdstuk q (Chapter q). X refereert aan oefening (exercise) op de website en P aan probleem in het boek. Voor de 'problems' worden de uitwerkingen achter in het boek gegeven.

- Ook de collegesheets bevatten regelmatig vragen of suggesties voor zelfstudie. Vergeet deze niet! De antwoorden worden tijdens het college getoond, maar bij de kopieën van de slides op de website zijn ze afgedekt (zwart kader).

- Sommige opgaven worden makkelijker naarmate je meer hoofdstukken bestudeerd hebt. Er kunnen ook opgaven zijn die hieronder niet genoemd worden maar die met een combinatie van kennis uit de verschillende hoofdstukken toch mogelijk worden.

- Het boek bevat geen opgaven, maar ze zijn beschikbaar via de website van het boek. Er staat een kopie van de opgaven op de website van GS, met geselecteerde antwoorden (niet de uitwerkingen). In het algemeen slaan we de onderdelen waar de SPICE simulator gebruikt wordt over.

- Verder bevat het boek een aantal 'problems', deze hebben een volledige uitwerking achterin het boek. Een voorbeeld is Problem 3.1 op bladzijde 111 van het boek. De uitwerking staat op bladzijde 739.

- Op de GS website zijn (bijna) alle oude tentamens verzameld, in principe allemaal met volledige uitwerking.

- Tijdens het college zijn steeds oefenopgaven uitgedeeld, en in het college gemaakt. Deze oefenopgaven zijn ook te vinden op de GS website, en in de reader.

3.5. Literatuur

Extra literatuur wordt aangegeven in het boek (pp. 32-33). Aanbevolen worden ook

- W. Wolf, Modern VLSI Design – Deep Submicron Systems, 3rd edition, Prentice Hall, 2003, ISBN 0-13-061970-1 (of eventueel de 2e editie: Modern VLSI Design – Systems on Silicon, 2nd edition, Prentice Hall, 1998, ISBN 0-12-989690-2)
- N.H.E. Weste, K. Eshraghian, Principles of CMOS VLSI Design – A Systems Perspective, 2nd edition, Addison Wesley, 1992, ISBN 0-201-53376-6
- Neil H.E. Weste, David Harris, CMOS VLSI Design : A Circuits and Systems Perspective, 3rd edition, Addison Wesley, 2004, ISBN: 0321149017

- S. Kang, Y. Lebleblici, CMOS Digital Integrated Circuits – Analysis and Design, 2nd edition, McGraw-Hill, 1999, ISBN 0-07-292507-8
- Harry Veendrick, Deep Submicron CMOS ICs – From Basics to ASICS, Kluwer, 1998, ISBN 90-557-612-81
- J. P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2002, ISBN 0-471-12704-3

Wolf is het meest systeem-georienteerd, met weinig elektronica, Veendrick is precies andersom. Van deze laatste is er ook nog een (oudere) Nederlandstalige versie. Weste en Eshragian is achterhaald v.w.b. de technologie, maar veel systeem aspecten blijven geldig. De derde editie van dit boek (met Harris als co-author) is helemaal bij de tijd. De stof in Kang komt aardig overeen met die in Rabaey, maar Rabaey is meer behulpzaam bij het ontwikkelen van een intuïtie in het beoordelen van het relatieve belang van en het werken met bepaalde effecten. De rol van abstractie en modelleren komt in Rabaey duidelijker tot uiting. Uyemura heeft ongeveer dezelfde breedte als Rabaey, maar is veel oppervlakkiger, helemaal bij de latere hoofdstukken.

3.6. Katz en DeCarlo/Lin

De boeken van Katz en DeCarlo/Lin worden gebruikt voor respectievelijk ET1405, Digitale Systemen en ET1305, Lineaire Elektrische Circuits. Het zijn belangrijke bronnen van voorkennis (en voor het opzoeken van dingen die je weer vergeten bent ☺).

3.7. Storey

Dit boek wordt gebruikt voor ET1205-D1. De gebruikte FET modellen (en terminologie) zijn een beetje anders. Echter, je zou in staat moeten zijn om die verschillen te overbruggen bij het gebruik van de aangeboden stof. Het gaat bij ET1205-D2 voornamelijk over de eigenschappen van een FET als schakelaar, waarbij eigenlijk uitsluitend met MOSFETs gewerkt wordt. Verder is het klein-signaal gedrag minder van belang, en gaat het meer om de stroomformules, in het bijzonder bij (zeer) korte kanalen. Dan wordt bijvoorbeeld het velocity-saturation effect vaak bepalend voor de totale geleverde stroom. Dit is van minder belang voor analoge schakelingen.

4. Module 0 – Introductie en Motivatie

Dit onderdeel wordt behandeld aan de hand van hoofdstuk 1 van de tweede editie, met belangrijke aanvullende informatie in de college presentatie / hand-outs. Van hoofdstuk 1 wordt de sectie 'Quality Metrics of a Digital Design' echter pas behandeld bij module 4 – inverter.

4.1. Samenvatting

1. Begrip van de explosieve ontwikkeling van het gebied van de micro-elektronica.
2. Abstractie en modellering als een middel om de complexiteit van VLSI, zowel wat betreft grootschaligheid als wat betreft details, te hanteren.
3. Introductie van basis terminologie.

4.2. Leeswijzer

P	1.1	A historical Perspective	4 – 6
P	1.2	Issues in Digital Integrated Circuit Design	6 – 15
(1)	1.3	Quality Metrics of a Digital Design	15 – 31

(1) Wordt behandeld bij module 4

4.3. Oefeningen

College-oefeningen. Veel oefeningen zijn er verder niet voor deze module, maar je kunt je begrip voor de 'aard van het beestje' vergroten door te kijken in het materiaal onder §1.5 'To Probe Further' van het boek, of op het internet diverse nuttige sites te bezoeken. Hiervoor kun je de links van de site van het vak als startpunt gebruiken. Zie ook de oefeningen op de site van het boek, evenals de oefeningen op de slides (tijdens college).

5. Module 1 – Devices

Module 3 wordt bestudeerd aan de hand van hoofdstuk 3 van Rabaey.

5.1. Leeswijzer

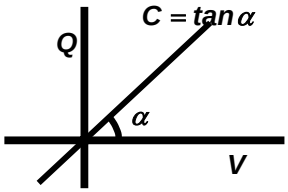
C	3.1	Introduction	74
P	3.2-3.2.1	A first glance at the diode	74 – 77
P	3.2.2	Static Behavior	77 – 80
O	3.2.3	Dynamic, or Transient, Behavior	80 – 83 (1)
O	3.2.4	Secondary Effects	84 – 85
O	3.2.5	Spice Diode Model	85 – 87
P	3.3 – 3.3.2	The MOS(FET) Transistor	87 – 99
O		Subthreshold Conduction	99 – 101
P		Models for Manual Analysis	101 – 106
O	3.3.2	Dynamic Behavior, etc.	106 – 113 (1)
P		Junction Capacitances	110 – 111
O	3.3.3	Some Secondary Effects	114 – 117
O	3.3.4	Spice Model for the MOS Transistor	117 – 120

O	3.4	A word on process variations	120 – 122
I	3.5	Perspective: Technology Scaling	122 – 128
P	3.6	Summary	128 – 129

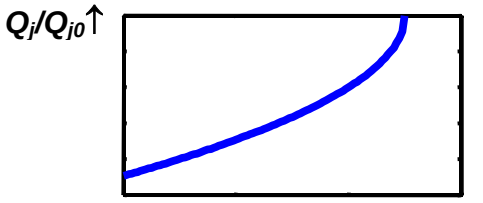
(1) Wij zullen (zie hieronder) een vereenvoudigd model voor de capaciteiten van diodes en MOS transistoren beschouwen. Zie hieronder, sectie 4.2 en 4.3. Primaire leerstof.

5.2. Equivalente Groot-Signaal waarden voor CMOS junctie capaciteiten

Zoals je in de secties over dynamische eigenschappen van de diode (Rabaey §3.2.3) en de MOS FET (3.3.2) zou kunnen lezen, zijn veel belangrijke capaciteiten (condensatoren) in CMOS structuren niet-lineair. Dit geldt m.n. voor de source- en drain junctiecapacteiten. Bij een lineaire capaciteit is het verband tussen lading en spanning een rechte lijn, en bij een niet-lineaire capaciteit is dat verband gekromd. Zie onderstaande figuren.



lineair



Niet-lineair

Het meenemen van zulke niet-lineariteiten bij de (handmatige) analyse van het dynamische gedrag (vertraging etc.) is niet eenvoudig. Daarom wordt in veel gevallen volstaan met een lineaire benadering van de niet-lineaire elementen. Deze kan bijvoorbeeld verkregen worden door het middelen van een soort effectieve capaciteit over het totale bereik van de spanning over het device. Dat betekent dat eerst de spanningszwaai bekend moet zijn, en daarna gemiddeld kan worden. De spanningszwaai kan afhankelijk zijn van de situatie, de schakeling, de omgeving, etc. Voor onze doelstelling zullen we hier niet precies zijn. We nemen een soort algemene, typische spanningszwaai en bepalen daar de gelineariseerde capaciteitswaarden mee.

Ook zullen we in dit college niet verder ingaan op de fysische analyse van de capaciteiten. Het model dat we zullen hanteren is niet bepaald nauwkeurig, maar wel bruikbaar als eerste benadering. Voor meer nauwkeurigheid kan een verfijndere analyse gedaan worden (zie het boek) of een simulator zoals SPICE gebruikt worden.

Het model dat we dan hanteren is als volgt:

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_d}$$

Hierbij duidt ΔQ_j het verschil in junctie lading aan tengevolge van een verschil in aangelegde spanning ΔV_d, anders gezegd

$$C_{eq} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}}$$

Hierbij zijn V_{high} en V_{low} de verschillende aangelegde spanningen.

Merk op dat we eigenlijk alleen over een diode- of junctiecapaciteit kunnen spreken wanneer de diode in sper staat ingesteld. Dat is voor de source/drain juncties van MOS transistoren doorgaans het geval.

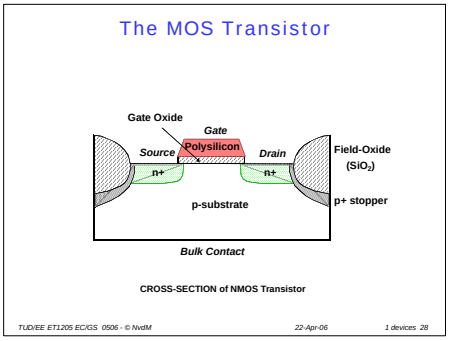
Merk ook op dat $\lim_{\Delta V_d \to 0} \frac{\Delta Q_j}{\Delta V_d}$ de zogenaamde differentiële of klein-signaal capaciteit voorstelt, de hellingshoek van de Q_j versus V_d grafiek. Deze waarde is vaak belangrijk bij analoge schakelingen. Bij digitale schakelingen kijken we normaal gesproken naar het groot-signaal gedrag, wat dus hier de reden is om te werken met een gelineariseerde waarde.

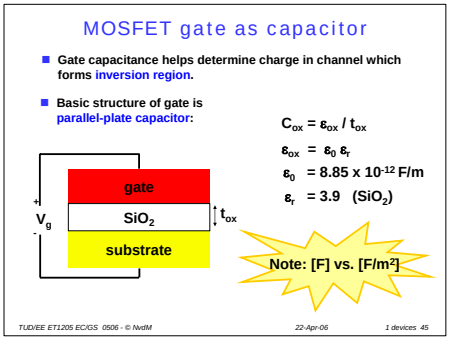
Voor de opgaven/ontwerpen/toetsvragen die we tegen zullen komen zullen we dus een (gelineariseerde), effectieve groot-signaal capaciteit als gegeven beschikbaar stellen.

Deze capaciteiten worden doorgaans gegeven als een C_j en C_{jsw} waarde, je moet deze waarden dan vermenigvuldigen met resp. de oppervlakte en de omtrek van het gebied om de totale diffusiecapaciteit te krijgen. Zie het kopje ‘Junction Capacitances’ op blz. 110, tot aan Problem 3.1. Formule 3.45 moet je zeker kunnen toepassen, maar die is niets anders als de formule die we ook zullen gebruiken voor interconnectcapaciteiten (Module 3).

5.3. Transistorcapaciteiten

De onderstaande slides illustreren dat een MOS transistor als een condensator werkt, waar de gate de ene elektrode (‘plaat’) vormt en het kanaal of het substraat (als de transistor in ‘cut-off’ mode is) de andere elektrode vormt, en het gate-oxide het dielectricum. Het model wat wij gaan hanteren voor de gate capaciteit is een lineaire capaciteit naar ground (aarde). De grootte van deze capaciteit wordt gegeven door het product van de gate-afmetingen (L en W van de transistor) en de C_{ox}. De C_{ox} is een technologie-parameter, en is voor een 0.25μm technologie in de orde van grootte van 6fF/μm^2. Dus, $C_{gate} = LWC_{ox}$.





De source en drain gebieden van een transistor zijn p/n juncties, waarvoor we zoals in de vorige paragraaf is uitgelegd, een gelineariseerde capaciteit gebruiken.

5.4. Oefeningen

College-oefeningen. Geschikte opgaven (zie de website van het boek, ook beschikbaar op de GS site), HS 3: opgaven 1 (c optioneel), 2 (met d), 3, 6-10, 11 (alleen a en c), 12. Zie verder de college-oefeningen op de slides.

6. Module 2 – Process

Module 3 wordt bestudeerd aan de hand van hoofdstuk 2 van Rabaey.

6.1. Leeswijzer

P	2.1	Introduction	36
P	2.2 – 2.2.2	Manufacturing CMOS Integrated Circuits	36 – 41
P	2.2.3	Some Recurring Process Steps	41 – 42
P	2.2.4	Simplified CMOS Process Flow	42 – 44
I	2.3	Design Rules	47 – 50
I	2.4	Packaging Integrated Circuits	51 – 61
I	2.5	Perspective - Trends in Process Technology	61 – 64
P	2.6	Summary	64
I	Insert A	IC Layout	67 – 71

6.2. Oefeningen

Zie hiervoor de tussentoetsen April 2001 en April 2002 op de GS website, alsmede de college-oefeningen op de slides en de extra oefenopgaven op de website.

7. Module 3 – Interconnect

Dit onderdeel wordt bestudeerd aan de hand van hoofdstuk 4 van het boek.

7.1. Leeswijzer

P	4.1	Introduction	136

P	4.2	A First Glance	136 – 138
P	4.3	Interconnect Parameters	138 – e.v.
O		So far we have …. (onder example 4.2)	147 – 148
O	4.3.3	Inductance	148 – 150
P	4.4	Electrical Wire Models	150 – 156
I	4.4.4	Distributed rc line	156 – 159 **(1)**
O	4.4.5	The transmission line	159 – e.v.
O	4.5	Spice wire models	170 – 171
I	4.5.3	Perspective: a look into the future	171 – 174

(1) Wij zullen (zie hieronder) een alternatieve beschouwing geven voor de vertragingstijd van signalen in verdeelde RC netwerken. Deze alternatieve beschouwing is primaire leerstof.

7.2. Verdeelde RC-netwerken: Symmetrische π Secties

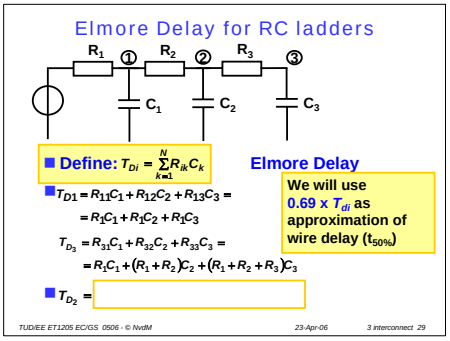
De Elmore-delay techniek wordt uitgelegd in §4.4.3 van het boek en op de ppt slides. Voor verdeelde RC lijnen van §4.4.4 gebruikt het boek een andere berekeningswijze. Echter, men kan afleiden dat de Elmore delay techniek ook gebruikt kan worden voor verdeelde RC lijnen en verdeelde RC trees, wanneer ieder segment van een RC-tree vervangen wordt door een symmetrische π-sectie. Dit is de aanpak die op de slides wordt uitgelegd en die wij voor deze cursus zullen hanteren.

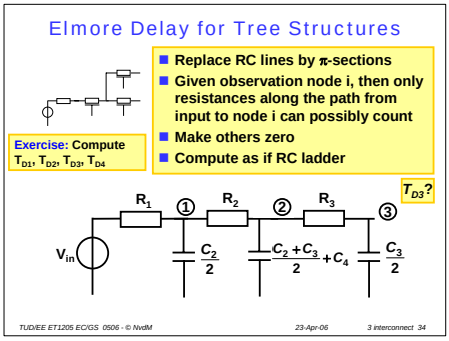
Wanneer ieder verdeeld RC segment wordt vervangen door een symmetrische π sectie is het resultaat dat we alleen hoeven te werken met lumped RC trees. Verder hebben we op de slides afgeleid dat voor het berekenen van de Elmore-delay tussen source en sink de weerstanden die niet in het pad zitten op nul gesteld kunnen worden waardoor een zogenaamde RC ladder ontstaat, en dat dan de som (over alle knopen) genomen wordt van de RC produkten waar C de capaciteit is van een knoop en R de weerstand van die knoop naar de bron.. De algemene formule is

$$T_{Di} = \sum_{k=1}^{N} R_{ik} C_k$$

waar T_{Di} de delay voorstelt van de ‘source’ (bron) naar de ‘sink’ (knoop i), zijnde het punt waarvan de Elmore delay gevraagd wordt, R_{ik} de weerstand is van het gemeenschappelijke deel van het pad naar de bron tussen knoop i en k, en C_k de capaciteit van knoop k.

De 2 ppt slides hieronder zijn het meest representatief voor deze techniek, ze vatten de formule samen, en geven voorbeelden voor berekening (en ook oefeningen).





7.3. Oefeningen

College-oefeningen. Zie de website, opgaven behorende bij HS 4: 1, 2 (alleen a en b), 3, 4a, 7, 12, 13. Verder de college-oefeningen op de slides.

8. Module 4 – Inverter

Dit wordt behandeld met hoofdstuk 5 van Rabaey, aangevuld met §1.3 van Rabaey.

8.1. Leeswijzer

P	5.1	Introduction	180
P	5.2	The Static CMOS inverter - intuitive	181 – 184
P	1.3.2	Functionality and Robustness	18 – 27
P	5.3	Evaluating the Robustness ...	184 – 191
I	5.3.3	Robustness Revisited	191 – 193
P	1.3.3	Performance	27 – 30
I	5.4	Performance of the CMOS inverter	193 – 213 **(1)**
P	1.3.4	Power and Energy Consumption	30 – 31
I	5.5	Power, Energy, and Energy-Delay	213 – 223
O	5.5.2	Static Consumption	223 – 225
O	5.5.3	Putting it All Together	225 – 227
O	5.5.4	Analyzing Power Consumption using SPICE	227 – 229
O	5.6	Perspective: Technology scaling…	229 – 231
P	5.7	Summary	232 – 233

(1) Het model dat wij zullen hanteren voor de capaciteiten in een CMOS inverter is veel eenvoudiger dan in het boek. Zie hieronder, en de discussie bij module 2, devices. Primaire leerstof.

7.2 Alternatieve beschouwing van CMOS inverter performance

Het gevolg van het rekenen met een eenvoudige, lineaire capaciteit van gate naar ground bij een MOS transistor is dat ook de ingangscapaciteit van een inverter eenvoudig wordt. De capaciteiten van de actieve gebieden (drain en source) worden ook gelinearisseerd (zie module 4) en uitgerekend alsof het interconnect capaciteiten zijn, met een term die evenredig is aan de oppervlakte en een term die evenredig is aan de omtrek.

8.2. 7.3 Oefeningen

College-oefeningen. Zie de website, opgaven voor HS 5: 1(a+c), 2b, 3 (behalve Spice simulatie), 4, 5, (a+c+d), 6, 7, 8. Zie ook de college-oefeningen op de slides.

9. Module 5 – Combinatorische Logica

Dit onderdeel wordt behandeld met hoofdstuk 6 uit Rabaey. De statische, complementaire CMOS poort is een veralgemening van de standaard inverter. Latere paragrafen beschrijven andere structuren voor het construeren van combinatorische poorten.

9.1. Samenvatting

1. Statische complementaire CMOS als veralgemening van standaard inverter, weten en begrijpen welke eigenschappen wel (zoals rail to rail swing, alleen dynamische dissipatie) overdragen, welke niet en welke nieuw zijn (zoals body effect).
2. Classificatie statisch – dynamisch.
3. Exclusiviteitsprincipe m.b.t. PUN en PDN.
4. Constructie van PUN en PDN met respectievelijk PMOS en NMOS transistoren, waarom.
5. Gegeven een transistortopologie de waarheidstabel (logische functie) kunnen bepalen.
6. Het kunnen construeren van een complexe poort voor een bepaalde logische functie, gegeven de waarheidstabel of booleaanse formule.
7. Dualiteit tussen PDN en PUN.
8. Onmogelijkheid van niet-inverterende poorten.
9. Aantal transistoren als functie van aantal ingangen.
10. Transistor sizing gebaseerd op equivalente R_{on} van een keten van transistoren, equivalente lange transistor met zelfde $R_{on.}$
11. Data-dependent delay door serie/parallel schakelen van transistoren, het bepalen van een equivalente Ron, het bepalen van de worst-case.
12. Kwalitatief begrip van 2^e orde effecten (interne capaciteiten, body effect, kortsluitstromen) als reden voor data-dependent timing, VTC en daarvan afgeleide eigenschappen, power.
13. Algemene afhankelijkheid van gate-delay van fan-in en fan-out, de wens tot vermijden van statische CMOS gates met hoge fan-in.
14. Kwalitatief begrip van schakelactiviteit (het gegeven dat de precieze schakelovergangen afhangen van inputsignalen) als mede bepalend voor de dissipatie.
15. Pseudo NMOS design stijl concept:
    Consequenties voor dissipatie, dimensionering, VTC, aantal transistoren voor een logische functie (oppervlakte).
16. Pass-Transistor logic – grond beginselen:
    Consequenties voor oppervlakte, VTC, cascadering.
17. Basis principes van dynamische logica:

Precharge fase, evaluatie fase, klok, geheugenwerking van de capaciteiten.

18. Consequenties:
    Alleen NMOS transistoren in PDN bepalen snelheid, aantal transistoren, non-ratioed, geen statisch vermogen, hogere snelheid, V_{OL}, V_{OH}, V_M, NM_H, NM_L, V_{IL}, V_{IH}, oppervlakte.
    Timing: precharge, bepalen van t_{PHL}.
19. Nut en noodzaak van evaluatie-transistor, kwalitatief begrip van logic activity voor de dissipatie.

9.2. Leeswijzer

P	6.1	Introduction	236
P	6.2	Static CMOS Design	236 – 237
P	6.2.1	Complementary CMOS	237 – 242
I		Propagation Delay of Complementary CMOS gates	242 – 249
I		Design Techniques for large fan-in	249 – 251
O		Optimizing performance in combinational networks	251 – 257
O		Power consumption in CMOS logic gates	257 – 263
P	6.2.2	Ratioed Logic	263 – 267
I		How to build even better loads	267 – 268
P	6.2.3	Pass-transistor basics	269 – 270
I		Example 6.10	271 – 272
O		Diversen	272 – 277
P		Solution 3: Transmission gate logic	277 – 280
I		Rest of § 6.2.3	280 – 284
I	6.3	Dynamic CMOS Design	
I	6.3.1	Dynamic Logic: Basic Principles	284 – 286
I	6.3.2	Speed and Power Dissipation of Dynamic Logic	287 – 290
I	6.3.3	Signal Integrity Issues in Dynamic Design	290 – 295
O	6.3.4	Cascading Dynamic Gates	295 – 303
O	6.4	Perspectives	303 – 306
P	6.5	Summary	306 – 307

9.3. Oefeningen

College-oefeningen. Oefeningen 6.1, 6.3a-b, 6.4, 6.5, 6.7, 6.8a, 6.10 van de website van Rabaey.

10. Module 6 - Sequential

Dit onderdeel wordt behandeld aan de hand van hoofdstuk 7 van Rabaey. De doelstelling van deze module is het bestuderen van CMOS/VLSI implementatie technieken van flip/flops en latches. Het item ‘pipelining’ wordt uitgesteld tot module 8 – timing design.

Voor extra uitleg kun je kijken op de site http://www.play-hookey.com/digital/. Deze bevat naast een uitleg ook een aantal interactieve animaties: een schema van een digitale schakeling met kleuren die de logische waarde aangeven en waarop je op de ingangen

kunt klikken om deze te veranderen. (Niet alleen flip-flops etc., maar ook gewone combinatorische poorten.)

10.1. Samenvatting

1. Verschil tussen voorgrond- en achtergrond geheugen.
2. Memory element timing parameters.
3. statische vs. dynamische geheugenwerking.
4. Regeneratie / positieve terugkoppeling als middel voor statische geheugenwerking.
5. Ladingsopslag als middel voor dynamische geheugenwerking.
6. Toepassingsmogelijkheden en beperkingen van statische en dynamische geheugenelementen, belangrijkste voordelen en nadelen van beide types t.o.v. elkaar.
7. Verschil tussen edge-triggered en level-sensitive devices, transparantie.
8. Set-up en hold requirements.
9. Master-slave principe.
10. Positivieve / negatieve latches / edge-triggered registers.
11. Het bi-stabiliteitsprincipe, stabiele v.s meta-stabiele werkingspunten, lusversterking in stabiele en meta-stabiele punten, omschakelingsmechanisme.
12. Werkingsprincipe van S-R latch als basis bi-stabiel element.
13. Geklokte S-R latch (ratioed sizing issues).
14. Multiplexer – gebaseerde latches, transistorimplementatie, werkingsprincipe, transmissiongate vs. NMOS implementatie.
15. Multiplexer based master-slave register, timing property analysis.

10.2. Leeswijzer

P	7.1	Introduction	326 – 327
P	7.1.1	Timing Metrics for Sequential Circuits	327 – 328
P	7.1.2	Classification of Memory Elements	328 – 330
	7.2	Static Latches and Registers	330
P	7.2.1	The Bistability Principle	330 – 332
P	7.2.2	Multiplexer-Based Latches	332 – 333
P	7.2.3	Master-Slave Edge-Triggered Register	333 – 335
I		Timing Properties of Multiplexer-Based Master ….	335 – 339
O	7.2.4	Low-Voltage Static Latches	339 – 341
P	7.2.5	Static SR Flip-Flops — Writing Data by Pure Force	341 – 344
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I	7.3.1	Dynamic Transmission-Gate Edge-Triggered Registers	344 – 346
O	7.3.2	C^2MOS — A Clock-Skew Insensitive Approach	346 – 350
O	7.3.3	True Single-Phase Clocked Register (TSPCR)	350 – 354
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(1)	7.5	Pipelining: An Approach to Optimize Sequential Circuits	358 – 360
(1)	7.5.1	Latch versus register based pipelines	360
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	7.6	Nonbistable Sequential Circuits	
P	7.6.1	The Schmitt Trigger	364 – 367
O	7.6.2	Monostable Sequential Circuits	367 – 368
I	7.6.3	Astable Circuits	368 – 370
O	7.7	Perspective: Choosing a Clocking Strategy	370 – 371
P	7.8	Summary	371 – 372

(1) §7.5 wordt als primaire stof behandeld bij module 7 – timing design

10.3. Oefeningen

College-oefeningen. Helaas kent dit hoofdstuk verder weinig bruikbare opgaven. Gelukkig helpen de oefeningen behorende bij modules 4 en 5 bij het begrip van module 6. Zie ook de oude examenopgaven met uitwerkingen, de opgaven op de collegesheets, de opgaven die in het college besproken zijn, en de 'problems' uit het boek.

11. Module 7 – Timing Design

Dit onderdeel wordt behandeld aan de hand van een klein gedeelte van hoofdstuk 10 van Rabaey, maar aangevuld met §7.5 t/m §7.5.1.

11.1. Samenvatting

1. Basis inzicht in timing design problemen bij VLSI systeem ontwerp
2. Inzicht in achtergronden van delay variaties.
3. Vertraging langs een RC lijn (van onbekende lengte) als bron van delay onzekerheid.
4. Weten wat synchroon ontwerpen inhoudt.
5. Gevolgen van klok skew voor synchroniciteit kunnen beoordelen.
6. Principe en belang van pipelining
7. Onderscheid kunnen maken tussen positieve en negatieve klok skew.
8. Timing regels voor klok skew in 1-fase edge-triggered en 2-fase master slave systemen begrijpen en kunnen toepassen.
9. Maatregelen tegen de gevolgen van klok skew (negatieve en begrensde skew en klok non-overlap periode vergroten) kunnen evalueren.
10. Behandelde principes van klokdistributie voor lage skew begrijpen en beoordelen.

11.2. Leeswijzer

P	10.1	Introduction	492
I	10.2	Timing Classification	492 – 495
P	10.3.1	Synchronous Timing Basics	495 – 500
I		Clock Jitter	500
I		The combined impact of Skew and Jitter	501 – 502
I	10.3.2	Sources of Skew and Jitter	
I	10.3.3	Clock Distribution Techniques	
O	10.3.4	Latch-Based Clocking	516 – 518
O	10.4-10.7	Self-Timed Circuit Design – Future Directions	519 – 551
P	***7.5 – 7.5.1 (!)***	Pipelining	358-361

11.3. Oefeningen

College-oefeningen. Verder, niet het eenvoudigste: 10.3, 10.5, 10.6. Verder 13.a 1^{e} deel (wat is het meta-stabiele punt). Zie verder de examenopgaven.

12. Module 8 – Modularity

Een echte systeemniveau module, met een duidelijke interactie naar logisch, elektrisch en layout niveau wat het kenmerk is van geïntegreerd systeemontwerp, en een belangrijk verschil is met 'gewoon' digitale schakelingen. Wordt behandeld met hoofdstuk 11 van Rabaey.

12.1. Leeswijzer

P	11.1	Introduction	560
P	11.2	Datapaths in Digital Processor Architectures	560 – 561
P	11.3	The Adder	561
P	11.3.1	The Binary Adder: Definitions	561 – 564
P	11.3.2	The Full Adder: Circuit Design Consideration	564 – 578
I	11.3.2	Manchester Carry Chain Adder	568 – 570
O	11.3.3	The Binary Adder: Logic Design Considerations	571 – 586
P	11.4	The Multiplier	586
P	11.4.1	The Multiplier: Definitions	586 – 587
P	11.4.2	Partial-Product Generation	587 – 589
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O		The Tree Multiplier	592 – 593
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P	11.5	The Shifter	595
P	11.5.1	Barrel Shifter	595 – 596
P	11.5.2	Logarithmic Shifter	596
O	11.6	Other Arithmetic Operators	596 – 600
O	11.7	Power and speed trade-offs	600 – 618
P	11.8	Perspective: Design as a Trade-off	618 – 619
P	11.9	Summary	619 – 620

12.2. Samenvatting

1. Begrijpen dat VLSI ontwerp zich op meerdere niveaus afspeelt.
2. Belang van modulariteit, hiërarchie, regelmaat voor het ontwerpen van VLSI systemen, kennen van deze begrippen.
3. Implicaties van deze begrippen voor de verschillende ontwerpniveaus (zoals bit-slicing)
4. basiskennis van VLSI optellers, vermenigvuldigers en schuivers.
5. Ripple-carry adder, werking en opbouw (logisch).
6. Idem op transistorniveau, VLSI geoptimaliseerde implementatie.

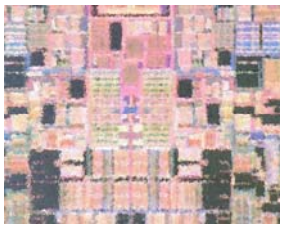
7. Delay evaluatie van ripple-carry adder.
8. Elimineren van inverterende trappen in carry-pad.
9. Mirror-adder (transistor implementatie)
10. Array multiplier, carry-save multiplier
11. Kritieke paden in deze multipliers.
12. Rechthoekig floorplan voor deze multiplier, als voorbeeld van implicaties en mogelijkheden van regelmaat en modulariteit voor layout.
13. Shifter design: binair, barrel en logaritmische
14. Implicaties voor lay-out, Lay-out strategieën voor bit-sliced datapaden.
15. Ontwerpen als trade-off van diverse tegenstrijdige belangen en eigenschappen.
16. Het belang van regelmaat en herhaling bij het ontwerpen van VLSI systemen.
17. Optimaliseren op verschillende niveaus
18. Het begrip “kritiek pad” kennen en begrijpen, kritieke paden kunnen bepalen.

12.3. Oefeningen

College-oefeningen. Opgaven 11.1, 11.2, 11.3, 11.4, 11.13 en 11.15. Zie ook de oude examens met uitwerkingen.

ET1205-D2
Elektronische Circuits
Geïntegreerde Systemen

N.P. (Nick) van der Meijs



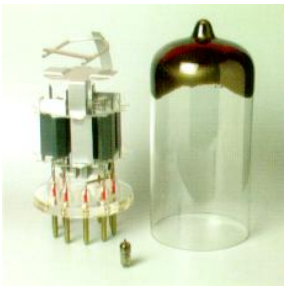
The First Computer

The Babbage Difference Engine (1832)

25,000 parts

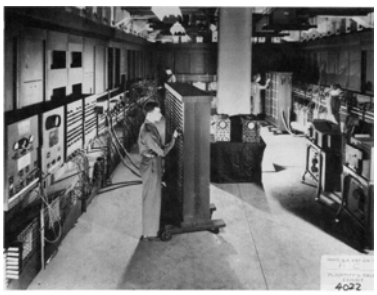
cost: £17,470

Vacuum Tube

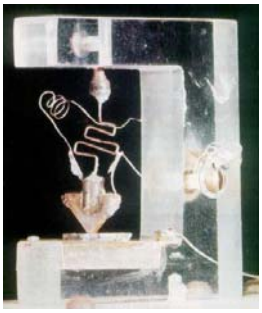


Fleming, 1904

ENIAC – The First Electronic Computer (1946)



First Transistor



Early Integrated Circuit

Bipolar Logic 1960's

ECL 3-input Gate Motorola 1966

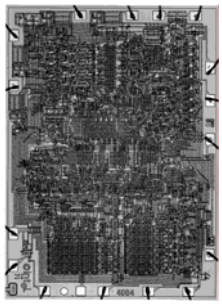
Intel Business PLan

The company will engage in research, development, adn manufacture and sales of integrated electronic structures to fulfill the needs of electronic systems manufacturers. This will include thin films, thick films, semiconductor devices, and other solid state componenets used in hybrid and monolithic integrated structures.

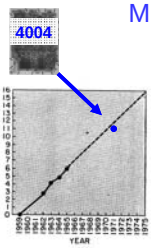
A variety of processes wil be established, both at a laboratory and production level. These include crystal growth, slicing, lapping, polishing, solid state diffusion, photolithographic masking and etching, vacuum evaporation, film deposition, assembly, packaging, and testing, as well as the development and manufacture of special processing and testing equipmentrequired to carry out these processes.

Products may include diodesd, transistors, field effect devices, photo sensitive devices, photo emitting devices, integrated circuits, and subsysteme commonly referred to by the phrase lagge scale integration" Principgl customers for these products are expected to be the manufacturers of advanced electronic systems for communications, radar, control and data processing. It is anticipated that many of these customers will be located outside California.

Intel 4004 Micro-Processor



Moore's Law



The number of transistors that can be integrated on a single chip will double every 18 months

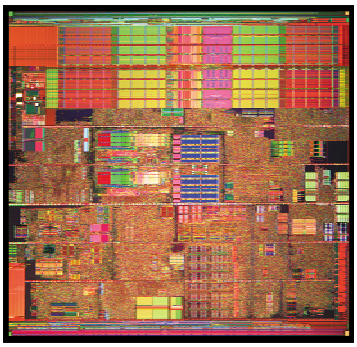
Gordon Moore, co-founder of Intel [Electronics, Vol 38, No. 8, 1965]

Intel Pentium IV

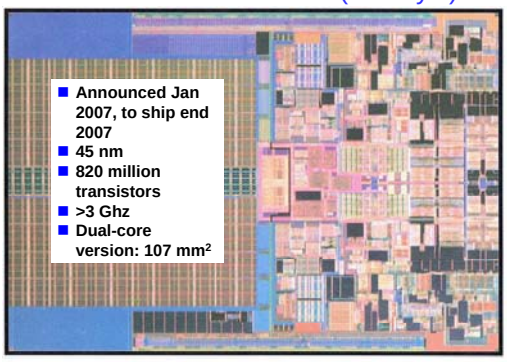
- 2001
- 0.18 µ details
- 42 million components
- 2 Ghz speed
- +/- 2 km interconnect

Intel Pentium IV (Prescott Core)

- Feb 2004
- 90 nm
- 125 million transistors
- 3.4 Ghz (later versions 3.8 Ghz)
- Architecture was abandoned because of heat problems



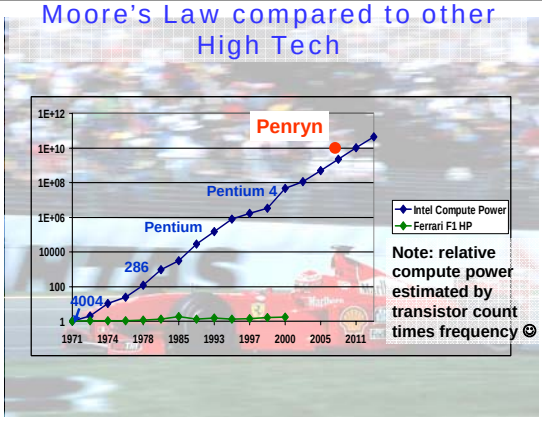
Intel 45 nm Core 2 (Penryn)



- Announced Jan 2007, to ship end 2007
- 45 nm
- 820 million transistors
- >3 Ghz
- Dual-core version: 107 mm²

[http://www.intel.com/technology/silicon/45nm_technology.htm]

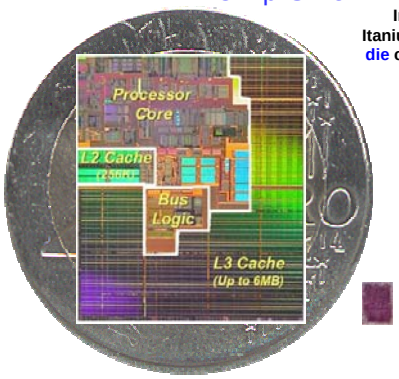
Moore's Law compared to other High Tech



Note: relative compute power estimated by transistor count times frequency ☺

Chip Size

Intel 4004 (1971) and Itanium (McKinley, 2002) die compared to 2€ coin



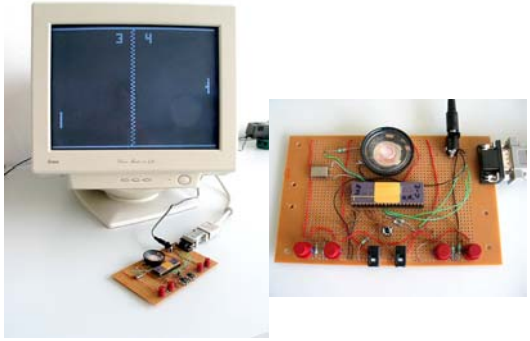
- So many transistors …
  and so little understanding
- What if we could understand
  how these transistors work
  and how we could use them

Geïntegreerde Systemen

Informatie over het college

- Inleiding in het ontwerpen en de realisatie van grote geïntegreerde schakelingen
- Volgend jaar zul je zelf een chip ontwerpen, en laten maken!!! (ontwerppracticum)
- Elektronica voor digitale schakelingen
- Het gedrag van transistoren en draden op een chip – detail nivo
- Beheersen van de complexiteit en grootschaligheid – systeem nivo

OP Lab: Pong Chip



Waarom Geïntegreerde Systemen

- Zeer belangrijke technologie, gezichtsbepalend voor onze maatschappij
- Bij uitstek een elektrotechnisch vakgebied
- Succesvolle methoden van dat vakgebied moeten als voorbeeld dienen voor toekomstige EE's
- Is van groot direct of indirect belang voor je verdere studie en latere carriere

Docent

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Basiseenheid	Netwerken & Systemen http://ens.ewi.tudelft.nl/
Afdeling	Microelectronics & Computer Engineering http://me.its.tudelft.nl

circuits & systems

Studiemateriaal

Boek:

Jan M. Rabaey - Digital Integrated Circuits, A Design Perspective, 2nd ed, Prentice Hall, 2003 (via ETV)

Syllabus:

Wordt bijgewerkt via web

Slides / Presentation Material:

Worden uitgedeeld en via het web (blackboard)

Nextprint (?):

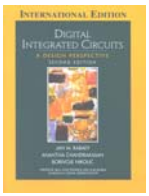
Reader beschikbaar na laatste college

Web site:

http://cas.et.tudelft.nl/~nick/courses/gs

Bi-directional link with blackboard

- Announcements, etc.
- Blackboard Discussion Forum (!)



Agenda

- Today first lecture
- Twice a week (Wed, Fri)
- Need to reschedule lectures of April 23, May 14, May 16.
- Exam: June 30.

Voorstel:

- donderdag 24 april : 08.30 - 10.30 uur. zaal E
- donderdag 22 mei : 08.30 - 10.30 uur. zaal E
- donderdag 29 mei : 08.30 - 10.30 uur. zaal E

Strategie voor GS

- Weet dat GS (EC) niet makkelijk is (Interessant (?) maar lastig)
  - Maak kennis met ontwerpen,
  - Synthese vraagt meer dan analyse
  - Analyse vraagt vaak goed gekozen benaderingen
- Weet dat het bijwonen van de colleges onvoldoende is voor een goed resultaat

Strategie voor GS (2)

- Gebruik de GS syllabus (en blackboard en GS web)
- Bedenk dat studielast te groot is voor de witte weken
- Wees actief tijdens de colleges en instructies: denk zelf en denk mee
- Voel je zelf verantwoordelijk voor je voortgang
- Houd je aan de volgende top drie:
  - 1. Zelfstudie
  - 2. Zelfstudie
  - 3. Zelfstudie

College

- Niet een op zichzelf staand verhaal
- Geen 100% dekking van de stof
- Gedeeltelijk aanvullend op boek/reader
- Vaak andere voorbeelden, invalshoeken
- (hopelijk) geen éénrichtingsverkeer
- Zelfstudie is het BELANGRIJKST

Zelfstudie

- Studeer – Oefen – Studeer – Oefen - …
- Hou de stof bij
- Lees een college vooruit
- Stel vragen
- Lees ook de andere delen uit boek
- Veel materiaal op het web

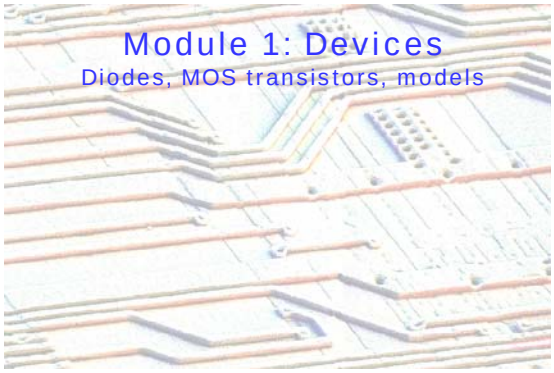
Studeren ≠ Lezen

Tentamen

- Gesloten boek, maar handgeschreven “cheat sheet” van 1 kantje A4 toegestaan (maakt niet uit hoe klein je schrijft …)
- Formules uit binnenflap voor/achter van boek worden ook uitgedeeld.
- Meer informatie volgt, op college en via BB

Module 1: Devices

Diodes, MOS transistors, models



Goal of this chapter

- Present intuitive understanding of device operation
- Introduction of basic device equations
- Introduction of models for manual analysis
- Introduction of models for SPICE simulation
- Analysis of secondary and deep-sub-micron effects
- Future trends

Outline

- Semiconductor Physics
- The diode
  - Depletion, I-V relations, capacitance,
- The MOS transistor
  - First glance, threshold, I-V relations, models
  - Dynamic behavior (capacitances), resistances,
- Process variations

Course Material for Devices

Chapter 3

P = primair, I = Illustratie, O = overslaan

C	3.1	Introduction	74
P	3.2-3.2.1	A first glance at the diode	74 – 77
P	3.2.2	Static Behavior	77 – 80
O	3.2.3	Dynamic, or Transient, Behavior	80 – 83 (1)
O	3.2.4	Secondary Effects	84 – 85
O	3.2.5	Spice Diode Model	85 – 87
P	3.3 – 3.3.2	The MOS(FET) Transistor	87 – 99
O		Subthreshold Conduction	99 – 101
P		Models for Manual Analysis	101 – 106
O	3.3.2	Dynamic Behavior, etc.	106 – 113 (1)
P		Junction Capacitances	110 – 111
O	3.3.3	Some Secondary Effects	114 – 117
O	3.3.4	Spice Model for the MOS Transistor	117 – 120
O	3.4	A word on process variations	120 – 122
I	3.5	Perspective: Technology Scaling	122 – 128
P	3.6	Summary	128 – 129

(1) Vervangend studiemateriaal voor dynamisch gedrag in syllabus

Modeling

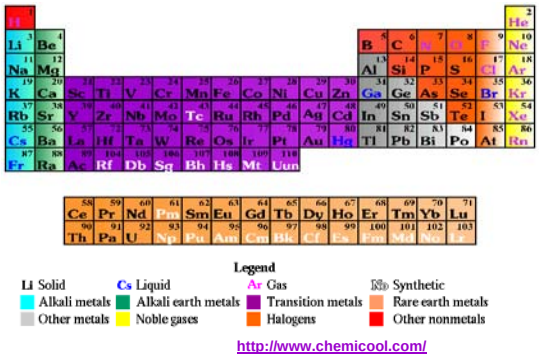
- An abstraction of (the properties) of something to help understanding and predicting its behavior
- Domain Specific: weather, climate, economy, stock market, ...
- Different models for something to answer different questions
- Black-Box modeling vs. Physically Based

- After Einstein: **a model should be as simple as possible, but not simpler**

Semiconductor Physics

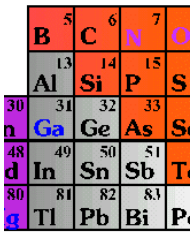
- All electrical behavior is determined by underlying physics
- This course is not about the physics
- But some small amount of background information helps built intuition
- Intuition is what an engineer/designer needs most
- Also see S&G Chapter 2.

Periodic System



http://www.chemicool.com/

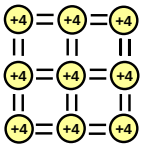
Periodic System



Name	Symbol	#	Valence
Silicon	Si	14	4
Boron	B	5	3
Phosphor	P	15	5
Arsenic	As	33	5
Germanium	Ge	32	4

Semiconductor Physics

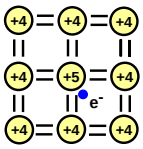
See also Tipler (BKV) 38.5



- Intrinsic Si
- Ideal crystal structure
- Valence 4
- almost no free carriers
- almost no conduction

$[n] = [p] = n_i = 1{,}5.10^{10}/cm^3$

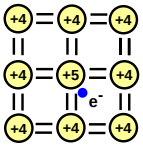
at 300 K for silicon



- doping with valence 5 atoms (Phosphor, Arsenic) introduces "loose electrons"
- electron donor
- conductivity depends on doping level

$n.p = n_i^2$ (in equilibrium)

Semiconductor Physics



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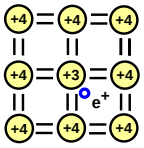


- doping with valence 3 atoms (Boron) introduces "loose holes"
- electron acceptors
- hole conductivity lower than electron conductivity

Semiconductor Physics

Si in equilibrium : $n.p = n_i^2 = 2.25 \times 10^{20}$ at 300K

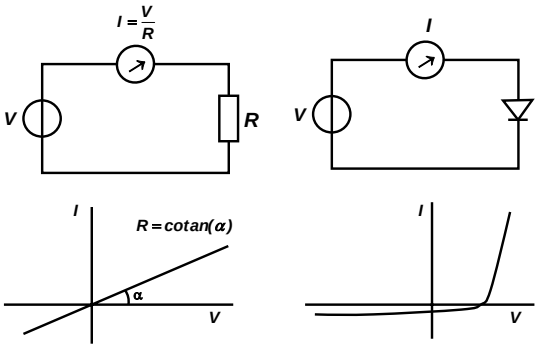
Intrinsic *Si* : $n = p = n_i$

$N_D >> N_A$	$N_A >> N_D$
Electron donors: As, P	Electron acceptors: B
n-type Si	p-type Si
$n \approx N_D$, $p = n_i^2/n$	$p \approx N_A$, $n = n_i^2/p$
Electrons: majority carriers	Holes: majority carriers
Holes: minority carriers	Electrons: minority carriers
Resistive material	Hole conductivity lower than electron conductivity
Conductivity depends on N_D	

The diode

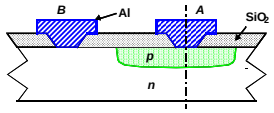
- **Depletion, I-V relations, capacitance,**

The diode: non-linear resistance

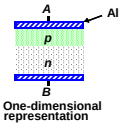


The Diode

See also Tipler (BKV) 38.6



Cross-section of *pn*-junction in an IC process



One-dimensional representation

Anode

Cathode

diode symbol

Diode is abundant as MOS source/drain

Ideal Diode, Abrupt pn junction Intuitive Description

p-Si n-Si

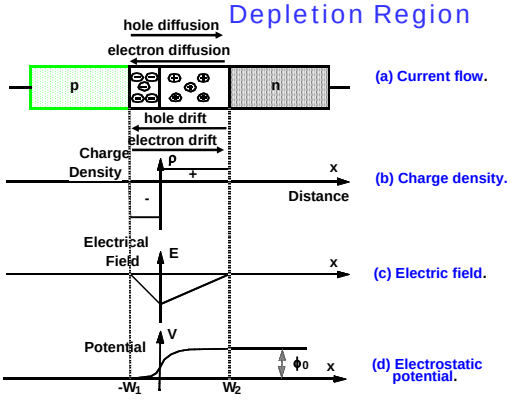
Electron diffusion → hole diffusion

p n

Hole drift → Electron drift

- Join n-Si with p-Si
- Concentration gradient of free carriers
- Diffusion current
- Space charge (depletion) region
- Electric field
- Drift current opposite to diffusion
- equilibrium

Depletion Region



Conduction

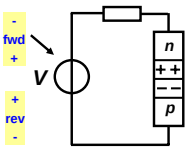
Typical N_A, N_D: 10^{15} … $10^{17}/cm^3$, ϕ_0 around 0.6 V

Built-in Potential

$$\phi_0 = \phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

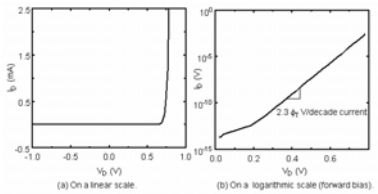
Thermal voltage

$$\phi_T = \frac{kT}{q} = 26mV \text{ at } 300K$$



- By applying an external voltage, width of depletion region can be changed
- Forward: becomes smaller and smaller, finaly conduction
- Reverse: becomes wider and wider => no conduction

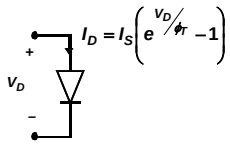
Diode Current



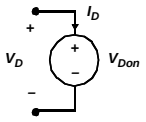
$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

- I_S: Saturation current
- Proportional to diode area
- Depends on doping levels, and widths of neutral regions
- Usually determined empirically

Models for Manual Analysis

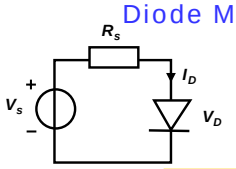


(a) Ideal diode model



(b) First-order diode model

Diode Model Example



Determine I_D

$I_D = I_S(e^{V_D/\phi_T} - 1)$ (diode model)

$V_s - R_s I_D = V_D$ (Kirchof)

$V_s - R_s I_S(e^{V_D/\phi_T} - 1) = V_D$ ☹

$I_s = 0.5e^{-16} A$

$kT/q = 25mV$

$V_s = 1.6V$

$R_s = 1k\Omega$

Picard Iteration

start: $V_D = 1.0V$

$\Rightarrow I_D = (V_s - V_D)/R_S = 0.600\ mA$

$\Rightarrow V_D = \phi_T(1 + ln(I_D/I_S)) = 0.663\ V$

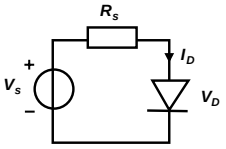
$\Rightarrow I_D = 0.937\ mA$

$\Rightarrow V_D = 0.674\ V$

$\Rightarrow I_D = 0.926\ mA$

$\Rightarrow V_D = 0.674\ V$ ☺

Diode Model Example



$I_s = 0.5e^{-16} A$

$kT/q = 25mV$

$V_s = 1.6V$

$R_s = 1k\Omega$

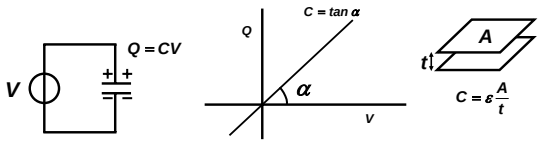
First order solution

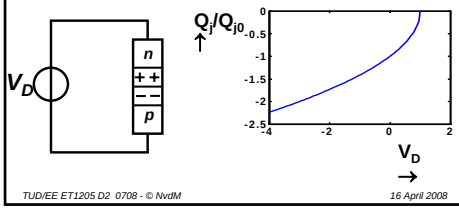
$V_D = 0.6V \Rightarrow I_D = 1mA$ error = 8 %

Now, take $V_s = 10.6V$ $R_s = 10K\Omega$

The error will be

Capacitance





Linearized Large-Signal Diode Capacitances

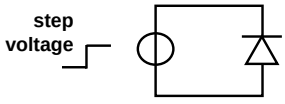
Summary:

- Diode capacitances highly n…
- Difficult with manual calculatio…
- We are ultimately interested in amount … charge being stored on (or removed from) capacitor
  - Since it takes time for this to happen, this determines the final switching speed of the circuit: more charge means more time!
- Linear capacitance: $\Delta Q = C\Delta V$: easy to work with
- Small-signal capacitance: $dQ = CdV$: for analog appl.
- Non-linear capacitance: $\Delta Q = f(V_{low}, V_{high})$

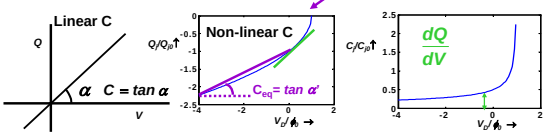
See the syllabus!

Work with C_{eq} for standardized voltage swings

Large Signal Equivalent Diode Capacitance



$C_{eq} = f(V_{high}, V_{low}) = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}}$



Linearized, large signal, depends on swing

Linearized, small signal, depends on bias

For analog applications

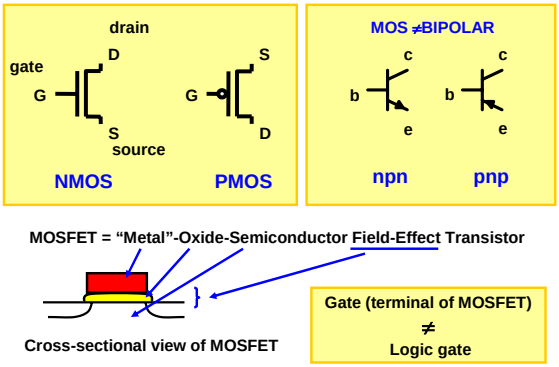
The MOS Transistor

- First glance, threshold, I-V relations, models
- Dynamic behavior (capacitances), resistances, more Second-Order effects, models

The MOS Transistor – compared to Storey

- no J-Fet
- Also other operating regions compared to saturation region (linear, velocity saturation)
- Include more effects (channel length modulation)
- Short-channel devices (bad for some analog circuits, good for (most) digital circuits)
- We will develop understanding of basic device equations

MOSFET Transistors

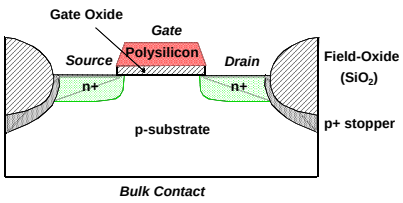


MOSFET = "Metal"-Oxide-Semiconductor Field-Effect Transistor

Cross-sectional view of MOSFET

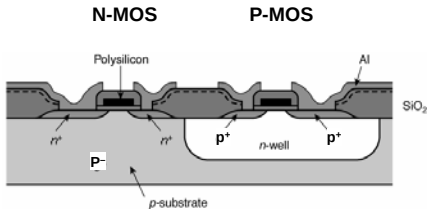
Gate (terminal of MOSFET) ≠ Logic gate

The MOS Transistor

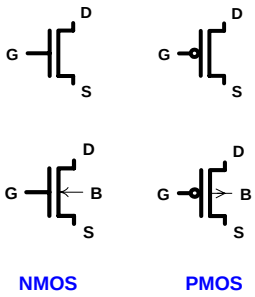


CROSS-SECTION of NMOS Transistor

Cross-Section of CMOS Technology



MOS Transistors



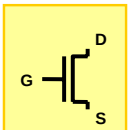
3-terminal model

bulk assumed to be connected to appropriate supply

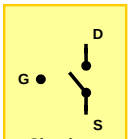
4-terminal model

B = bulk (substrate)

MOS Transistor Switch Level Models



NMOS



Simplest possible useful model

Position of switch depends on gate voltage

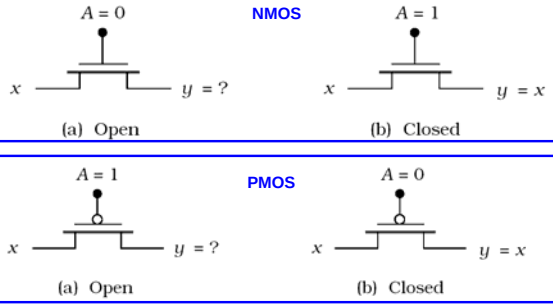
V_G	NMOS	PMOS
hi	closed	open
lo	open	closed

- Connection between source and drain depends on gate voltage, current can flow from source to drain and vice versa if closed
- No static current flows into gate terminal

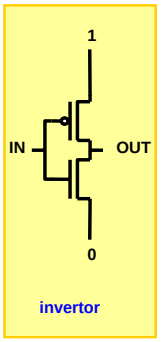
Mos Switch Model (2)

Position of switch depends on gate voltage

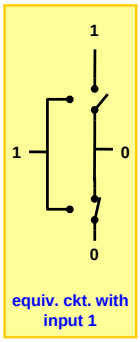
V_G	NMOS	PMOS
hi	closed	open
lo	open	closed



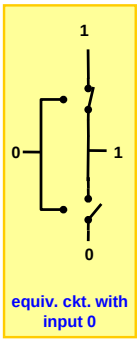
CMOS Inverter Operation Principle



invertor

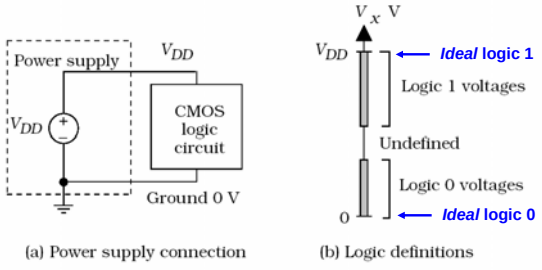


equiv. ckt. with input 1



equiv. ckt. with input 0

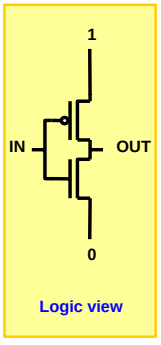
From Logic to Voltages



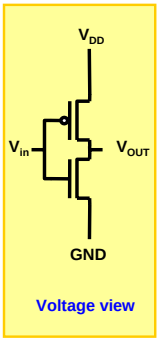
Ideal logic 0 corresponds to $V_x = 0V$
Ideal logic 1 corresponds to $V_x = V_{DD}$

Not all actual voltages in circuit necessarily correspond to ideal logic levels, see figure (b) above

From Logic to Voltages



Logic view

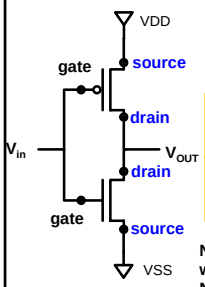


Voltage view

Note:

- GND = GROUND = 0V
- Sometimes also called V_{SS}
- V_{DD} is highest voltage level in circuit
- V_{DD} value depends on technology, has been reduced from 5V to 1V and lower over the years
- All voltages V_x in ckt: $0 \le V_x \le V_{DD}$

Source and Drain Terminals

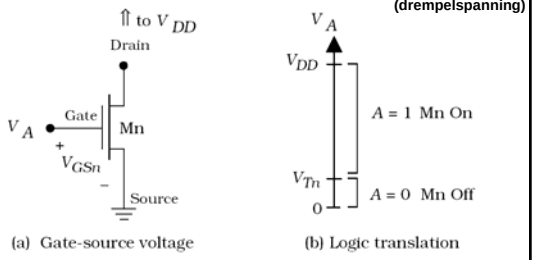


	NMOS	PMOS	PMOS
Source	Lowest potential	Highest potential	Lowest |potential|
Drain	Highest potential	Lowest potential	Highest |potential|

Note 1: Polarities of PMOS voltage reversed when compared to NMOS
Note 2: MOS transistor is completely symmetrical! Can interchange source and drain, without any effect. Source/drain is only a naming convention.

nFET Threshold Voltage

(drempelspanning)

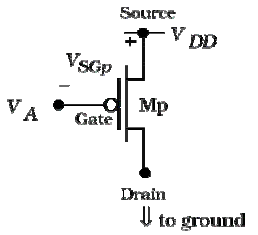


(a) Gate-source voltage (b) Logic translation

nFET is off when $V_{GSn} \le V_{Tn}$
nFET is on when $V_{GSn} > V_{Tn}$

V_{Tn} ~ 0.5 … 0.7V

pFET Threshold Voltage



nFET is off when $V_{GSn} \le V_{Tn}$
nFET is on when $V_{GSn} > V_{Tn}$

pFET and nFET behave complementary

Equivalent conditions

pFET is off when $V_{GSp} \ge V_{Tp}$
pFET is on when $V_{GSp} < V_{Tp}$

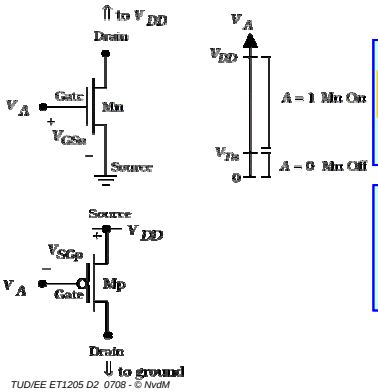
pFET is off when $-V_{GSp} \le -V_{Tp}$
pFET is on when $-V_{GSp} > -V_{Tp}$

pFET is off when $|V_{GSp}| \le |V_{Tp}|$
pFET is on when $|V_{GSp}| > |V_{Tp}|$

V_{Tp} ~ –0.5 … –0.7V (negative!)

Often most useful

Excercise

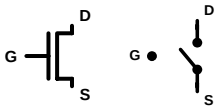


transistor on the left using
nFET is off when $V_{GSn} \le V_{Tn}$
nFET is on when $V_{GSn} > V_{Tn}$
corresponds to diagram on right

Draw same diagram for PMOS using
pFET is off when $-V_{GSp} \le -V_{Tp}$
pFET is on when $-V_{GSp} > -V_{Tp}$

MOS Transistor Treshold Voltage

Treshold voltage V_T: point at which transistor turns on



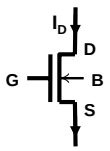
Position of switch depends on gate voltage (relative to source)

V_{GS}	NMOS	PMOS
$V_{GS} > V_T$	closed	open
$V_{GS} < V_T$	open	closed

Is this all there is?

- You don't believe that (CMOS) life can be so simple, do you?
- Discuss some of the things that you would expect to be non-idealities of CMOS as a switch
- Since we want to design CMOS circuits, we need a deeper understanding of CMOS circuits
- Next slide shows where we are going

MOS Models for Manual Analysis



determined by circuit
V_{DS}, V_{GS}, V_{SB}

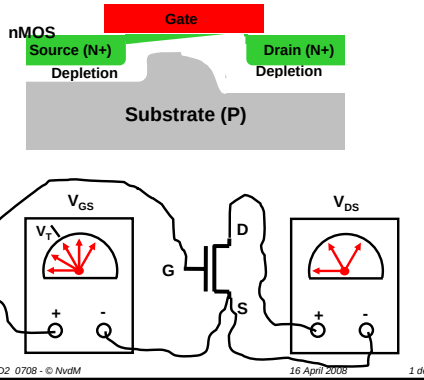
determined by technology
$k, \lambda, V_{DSAT}, V_{T0}, \gamma, \phi_F$

MOS model for manual analysis

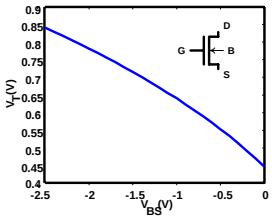
$$I_D = k\left(V_{GT}V_{MIN} - 0.5V_{MIN}^2\right)\left(1+\lambda V_{DS}\right) \quad \text{for } V_{GT} \ge 0$$
$$= 0 \quad \text{for } V_{GT} \le 0$$
$$V_{MIN} = MIN\left(V_{DS}, V_{GT}, V_{DSAT}\right)$$

$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

nMOS Transistor Operation



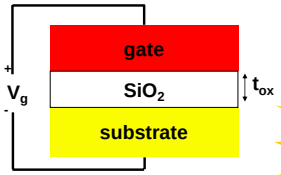
Body Effect



- V_T is not constant
- Depends on V_S vs V_B
- Our wish is to understand & predict behavior of CMOS devices
- We will start with V_T

MOSFET gate as capacitor

- Gate capacitance helps determine charge in channel which forms inversion region.
- Basic structure of gate is parallel-plate capacitor:



$C_{ox} = \varepsilon_{ox} / t_{ox}$

$\varepsilon_{ox} = \varepsilon_0 \varepsilon_r$

$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m

$\varepsilon_r = 3.9$ (SiO_2)

Note: [F] vs. [F/m^2]

The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_i}{C_{ox}}$$

Contact Potential
Fermi Potential
Depletion Layer Charge
Surface Charge
Implants

$$Q_B = \gamma\left(\sqrt{|-2\phi_F + V_{SB}|}\right) \quad \text{with} \quad \gamma = \frac{\sqrt{2\varepsilon_{Si} N_A}}{C_{ox}}$$

Body Effect Coefficient

Forget all this

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

But be able to use this

with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_i}{C_{ox}}$$

and this

$I_D(V_{GS}, V_{DS}, V_{BS})$

MOS model for manual analysis

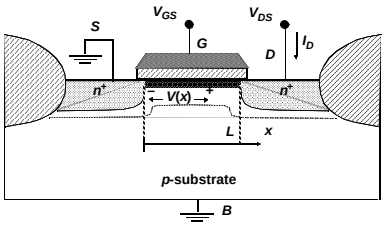
$$I_D = k\left(V_{GT} V_{MIN} - 0.5 V_{MIN}^2\right)\left(1 + \lambda V_{DS}\right) \quad \text{for } V_{GT} \geq 0$$

$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = MIN(V_{DS}, V_{GT}, V_{DSAT})$$

- Different operation regions
- Different behavior for each region:
  - off
  - resistive ← NEXT
  - saturation
  - velocity saturation

Current-Voltage Relations



MOS transistor and its bias conditions

I-V In Resistive Region

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

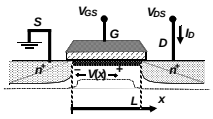
$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T]$$ Inversion Charge

$$I_D = -\mu_n \frac{dV}{dx} Q_i(x) W$$

I_D Drain Current
μ_n mobility (n-Si)

$$v_n = -\mu_n \varepsilon(x) = \mu_n \frac{dV}{dx}$$

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS} - V - V_T] dV$$



$$I_D L = \mu_n C_{ox} W \left[(V_{GS} - V_T) V - \frac{1}{2} V^2 \right]_0^{V_{DS}}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Process Gain and Device Gain

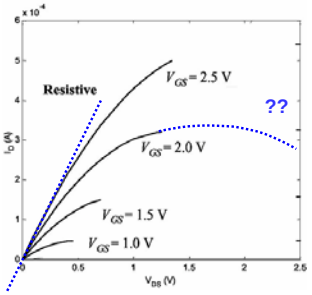
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$k_n' = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}$$ Process transconductance parameter

$$k = k_n' \frac{W}{L}$$ Gain factor of device

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$ (resistive/linear/ohmic regime)

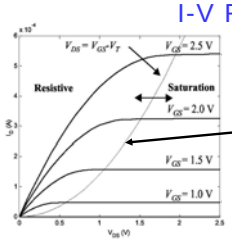
I-V Relation



■ No!

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$ (resistive regime)

I-V Relation



This curve is where I_D curves begin to run flat: I_D does not anymore depend on V_{DS}

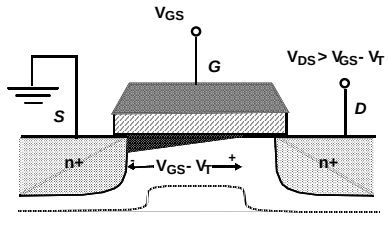
$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

The curve is given by

$$\frac{dI_D}{dV_{DS}} = k[(V_{GS} - V_T) - V_{DS}] = 0 \Rightarrow V_{DS} = V_{GS} - V_T$$

The value $V_{DS} = V_{GS} - V_T$ is special: it is the boundary between resistive regime and saturation regime (pinch-off)

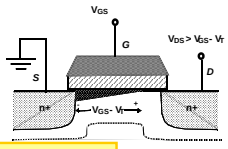
Transistor in Saturation



I-V in saturation

$V_{DS} < V_{GS} - V_T$:

$$I_D = k \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$



Saturation: $V_{DS} > V_{GS} - V_T$

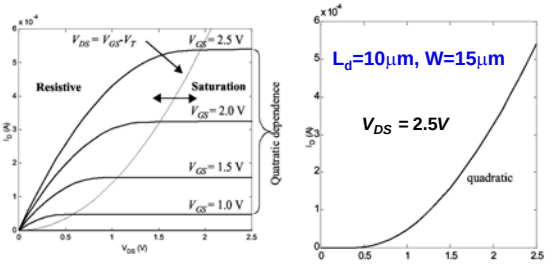
Current does not increase when $V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = I_D \Big|_{V_{DS} = V_{GS} - V_T}$$ Saturation current

$$I_{DSAT} = k \left[(V_{GS} - V_T)(V_{GS} - V_T) - \frac{1}{2} (V_{GS} - V_T)^2 \right]$$

$$= \frac{1}{2} k (V_{GS} - V_T)^2$$

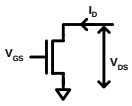
I-V Relation



$$I_D = k\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad \text{(resistive regime)}$$

$$= \frac{1}{2}k(V_{GS}-V_T)^2 \quad \text{(saturation)}$$

Output Impedance



Definition: $Z_{out} = \frac{dV_{ds}}{dI_d}$

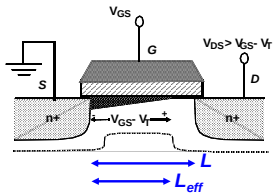
$$I_D = \frac{1}{2}k(V_{GS}-V_T)^2$$

What is the output impedance?

Is this plausible?

What is happening?

Channel Length Modulation



Empirical Model for Effective Channel Length

$$L_{eff} = \frac{L}{1+\lambda V_{DS}}$$

$$I_{DSAT} = \frac{1}{2}k_n'\frac{W}{L_{eff}}(V_{GS}-V_T)^2$$

$$= \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$= \frac{1}{2}k(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

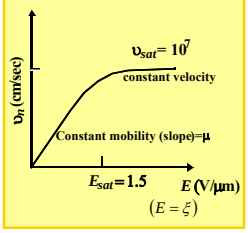
Velocity Saturation (1)

1. Still model not complete: need to include effects of limited carrier velocity

2. Carrier velocity (ideal model):
Linear with field

$$v_n = -\mu_n\xi(x) = \mu_n\frac{dV}{dx}$$

3. Reality



4. Simple v_{sat} Model:

$v_n = \mu_n\xi$ for $\xi \le \xi_c$

$= \mu_n\xi_c = v_{sat}$ for $\xi \ge \xi_c$

ξ_c Critical Field

v_{sat} Saturation *Velocity*

Velocity Saturation (2)

Onset of velocity saturation can be translated into a critical voltage V_{DS}: V_{DSAT}. This value depends on *L*.

Velocity saturation parameters

$$V_{DSAT} = L\xi_c = \frac{Lv_{sat}}{\mu_n}$$

voltage velocity

L	V_{DSAT}
2	3
1	1.5
0.25	0.375
0.18	0.27
…	…

First order, empirical model

$$I_{DSAT} = I_D(V_{DS} = V_{DSAT})$$

$$= k\left[(V_{GS}-V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right]$$ Velocity Saturation

Overview

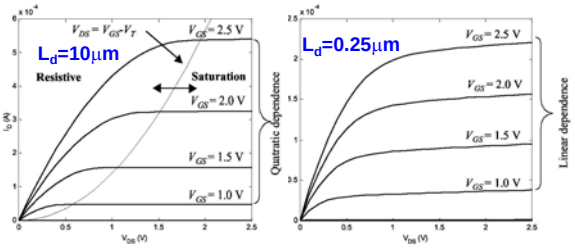
$$I_D = k\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$ resistive regime base equation

$$= \frac{1}{2}k(V_{GS}-V_T)^2$$ saturation: $V_{DS} \rightarrow V_{GS}-V_T$

$$= k\left[(V_{GS}-V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right]$$ velocity sat: $V_{DS} \rightarrow V_{DSAT}$

$$I_D = I_D'(1+\lambda V_{DS})$$ Channel Length Modulation

I_D as a function of V_{DS}

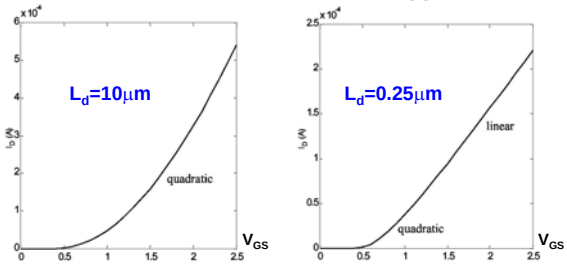


Long channel device w/o velocity saturation

Short channel device with velocity saturation

$$W = 1.5L$$

I_D as a function of V_{GS}



Long channel device w/o velocity saturation

$$I_D = \frac{1}{2}k(V_{GS} - V_T)^2$$

Short channel device with velocity saturation

$$I_D = k\left[(V_{GS} - V_T)V_{DSAT} - 0.5V_{DSAT}^2\right]$$

MOS Models for Manual Analysis

Region Specific Models

Channel length modulation added to resitive region, in order to enforce continuity

$$I_D' = k\left(V_{GT}V_{DS} - 0.5V_{DS}^2\right)$$ Resistive region

$$I_D' = k\left(V_{GT}V_{GT} - 0.5V_{GT}^2\right)$$ Saturation

$$I_D' = k\left(V_{GT}V_{DSAT} - 0.5V_{DSAT}^2\right)$$ Velocity Saturation

$$I_D = I_D'(1 + \lambda V_{DS})$$ Channel Length Modulation

Comprehensive model

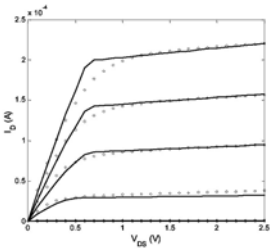
$$I_D = k\left(V_{GT}V_{MIN} - 0.5V_{MIN}^2\right)(1 + \lambda V_{DS}) \quad \text{for } V_{GT} \geq 0$$

$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = MIN(V_{DS}, V_{GT}, V_{DSAT})$$

$$V_{GT} = V_{GS} - V_T, \quad V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

MOS Model Comparison

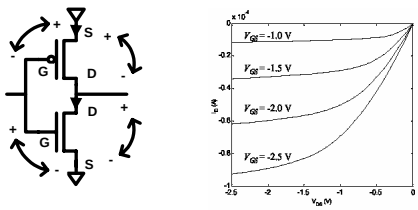


- Many more far more advanced models do exist (BSIM4 ~ 20k lines of C)
- Are only suited for computer simulation
- The SPICE simulator is the 'good old' workhorse of the industry
- Reliable, but low speed

Solid line: simple model

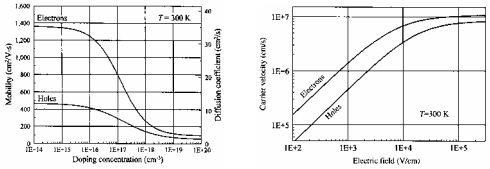
Dotted line: SPICE simulation

NMOS vs. PMOS



- PMOS (V_{DS}, V_{GS}, I_D, V_T) < 0
- Can calculate as if NMOS using absolute values
- PMOS device not as strong as NMOS

NMOS vs. PMOS (2)



Zero-field mobility (bulk!) Velocity vs. Field

$$\mu_p < \mu_n \Rightarrow k_p' < k_n'$$

$$v_{sat_p} \approx v_{sat_n} \Rightarrow |V_{DSAT_p}| > |V_{DSAT_n}|$$

	V_{Tn} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

Alternative Saturation Expression

- Saturation if $V_{DS} > V_{GS} - V_T$
- Show that $V_{DS} > V_{GS} - V_T \Leftrightarrow V_{GD} < V_T$
- Proof:

$$V_{DS} > V_{GS} - V_T$$
$$\Leftrightarrow V_D - V_S > V_G - V_S - V_T$$
$$\Leftrightarrow V_D > V_G - V_T$$
$$\Leftrightarrow V_G - V_T < V_D$$
$$\Leftrightarrow V_G - V_D < V_T$$
$$\Leftrightarrow V_{GD} < V_T$$

Physically this relates to 'amount of inversion' at drain side
If inversion at drain side disappears: pinch-off

- This is an alternative expression for the saturation region
- Can be handy

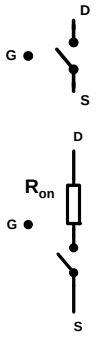
MOS Device Symmetry

- MOS transistors are symmetrical
- Strong inversion at source if $V_{GS} > V_T$
- Strong inversion at drain if $V_{GD} > V_T$ } Independent!
- You should check the I-V relations when interchanging drain and source
- Identification of source drain only by convention
- Determined by circuit-environment

	NMOS	PMOS	General
Source	V_{SS}-side	V_{DD}-side	Strongest inversion
Drain	V_{DD}-side	V_{SS}-side	Weakest inversion

V_{SS}: low supply voltage, V_{DD} = high supply voltage

Improved MOS Transistor Switch Level Model



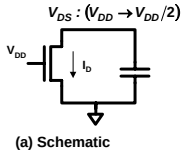
Position of switch depends on gate to source voltage

V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

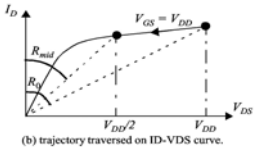
More detailed model may include R_{on}

- R_{on} is highly non-linear
- Make linear approximation R_{eq}
- Model with (linear) R_{eq} less detailed then previous equation based model, but often useful for first estimates of behavior

Switch Model R_{on}



(a) Schematic



(b) trajectory traversed on ID-VDS curve.

$$R_{eq} = \frac{1}{2}\left[\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right]$$

$$\frac{1}{1+\lambda V_{DD}} \approx 1 - \lambda V_{DD} + O\left(\lambda^2 V_{dd}^2\right)$$

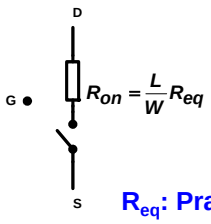
2.3% error with $\lambda = 0.06\ V^{-1}, V_{DD} = 2.5V$

$$R_{eq} \approx \frac{1}{2}\frac{V_{DD}}{I_{DSAT}}\left[\left(1-\lambda V_{DD} + \frac{1}{2}(1-\lambda V_{DD}/2)\right)\right]$$

$$= \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left[1 - \frac{5}{6}\lambda V_{DD}\right]$$

Theory!

MOS Transistor Switch Level Model (Empirical).



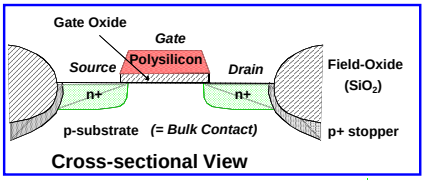
Position of switch depends on gate to source voltage

V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

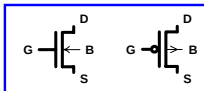
R_{eq}: Practice!

R_{eq} \ V_{dd} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

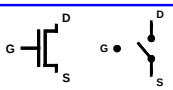
The MOS Transistor Summary



Cross-sectional View



Schematic symbols, very often w/o bulk contact

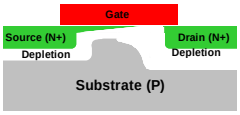


Switch closed if $V_{GS} > V_T$

Simplest possible equiv. ckt.

The MOS Transistor Summary ctd.

- Need to analyze speed, power, noise etc of MOS circuits
- Simple switch-level model not sufficient
- Study exact operation to derive more precise IV relations



$$I_D = k\left(V_{GT}V_{MIN} - 0.5V_{MIN}^2\right)\left(1+\lambda V_{DS}\right) \quad \text{for } V_{GT} \geq 0$$
$$= 0 \quad \text{for } V_{GT} \leq 0$$

$$V_{MIN} = MIN\left(V_{DS}, V_{GT}, V_{DSAT}\right)$$
$$V_{GT} = V_{GS} - V_T, \qquad V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

Summary

- Semiconductor Physics
- The diode
  - Depletion, I-V relations, capacitance, secondary effects, models
- The MOS transistor
  - First glance, threshold, I-V relations, models
  - Dynamic behavior (capacitances), resistances, more Second-Order effects, models

Part 2: Process

Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

Outline

- CMOS Processing
  - Wafer Production
  - CMOS Process Outline
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Only very briefly

Course Material for 02-Process

Chapter 2, 2nd ed.

P = primair, I = Illustratie, O = overslaan

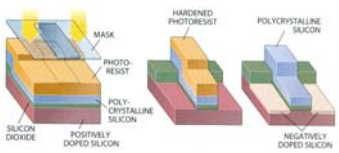
P	2.1	Introduction	36
P	2.2-2.2.2	Manufacturing CMOS Integrated Circuits	36-41
P	2.2.3	Some Recurring Process Steps	41-42
P	2.2.4	Simplified CMOS Process Flow	42-44
I	2.3	Design Rules	47-50
I	2.4	Packaging Integrated Circuits	51-61
I	2.5	Perspective - Trends in Process Technology	61-64
P	2.6	Summary	64
I	Insert A	IC Layout	67-71

CMOS Processing

- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

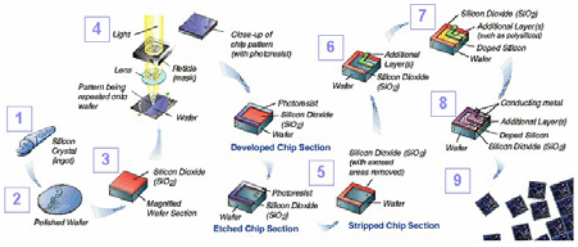
IC Technology

- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist

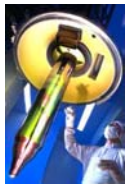


Multiple cycles, 100's STEPS in total

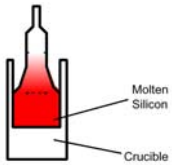
Another Overview of Semiconductor Processing



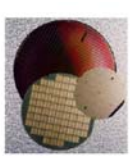
Wafer Processing – Czochralski Method

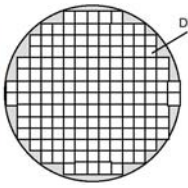


- Start with crucible of molten silicon (≈1425ºC)
- Insert crystal seed in melt
- Slowly rotate/raise seed to form single crystal boule
- After cooling, slice boule into wafers & polish



Wafer Structure

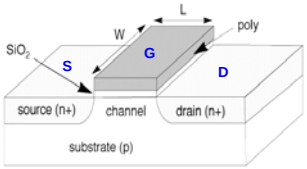


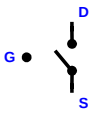


300 mm wafer (sematech)

CMOS Process Outline

MOS Transistor



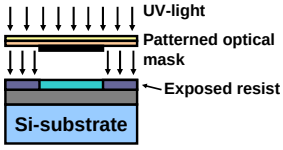


Position of switch depends on gate to source voltage

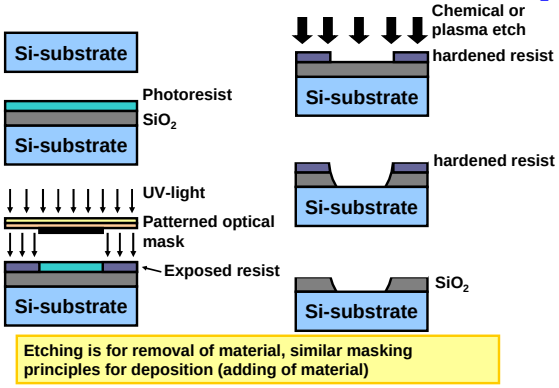
V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

How Patterns on a Chip are Created

- Basic Principle: Photolithography
  - Like projecting an image through a photographic negative (or positive)
- Coat wafer with Photoresist
- Shine UV light through glass mask
- Develop: dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")



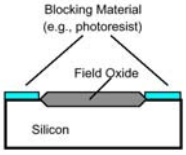
Example: Etching Step, opening of SiO_2



Etching is for removal of material, similar masking principles for deposition (adding of material)

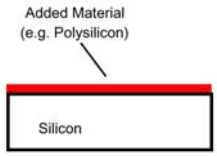
Oxidation

- SiO_2 formed by oxidation
  - Wet oxidation: heat with water (900ºC - 1200 ºC)
  - Dry oxidation:heat with pure oxygen (1200 ºC)
- Oxide occupies more volume
- Alternative: deposition



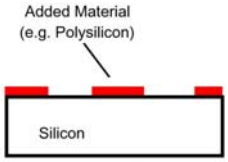
Adding Materials

- Add materials on top of silicon
  - Polysilicon
  - Metal
  - SiO_2
- Methods
  - Vapor deposition
  - Sputtering (Metal ions)



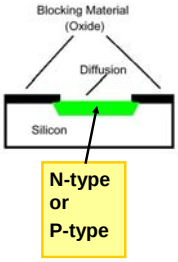
Patterning Added Materials

- Add material to wafer
- Coat with photoresist
- Selectively remove photo resist (PR), after exposure through mask
- Remove unprotected (by PR) material
- Remove remaining PR



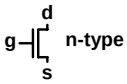
Diffusion

- Modify electrical properties of Si:
  - N-type (extra electrons)
  - or p-type
    (fewer electrons ⇔ extra holes)
- Introduce dopant via epitaxy or ion implant e.g. Arsenic (N), Boron (P)
- Allow dopants to diffuse
- Block diffusion in selective areas using oxide or PR (photo-resist)
- Diffusion spreads both vertically, horizontally

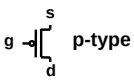


CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



n-type



p-type

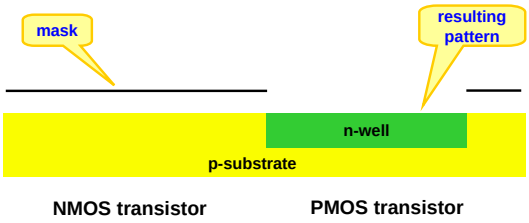
- "on" when V_g is high
- With n-type s/d
- Electrons (n) as carrier
- Built in p-type Si

- "on" when V_g is low
- With p-type s/d
- Holes (p) as carrier
- Built in n-type Si

n-well (for PMOS) in p-type substrate (for NMOS)

Outline of Process Flow

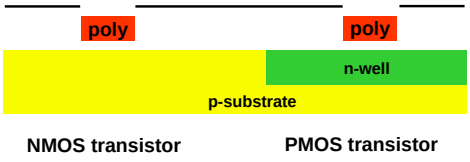
First place n-well to provide properly-doped substrate for n-type, p-type transistors :



NMOS transistor PMOS transistor

Outline of Process Flow, cont'd

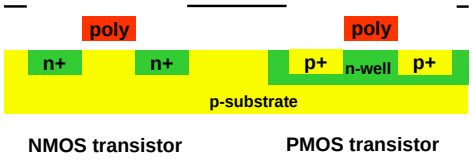
Pattern gate next, to later act as a mask for source and drain diffusions:



NMOS transistor PMOS transistor

Outline of Process Flow, cont'd

Add s/d diffusions, with self-masking by poly gate:



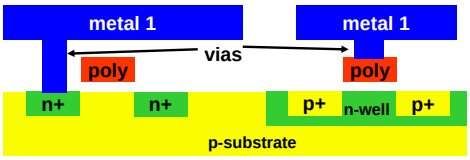
NMOS transistor PMOS transistor

Self-masking: Poly also works as a mask, ensuring good alignment of s/d to gate

Outline of Process Flow, cont'd

Start adding metal layers:

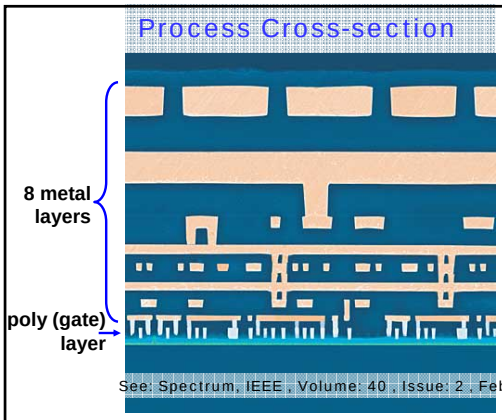
Via: contact hole between metal layers



NMOS transistor PMOS transistor

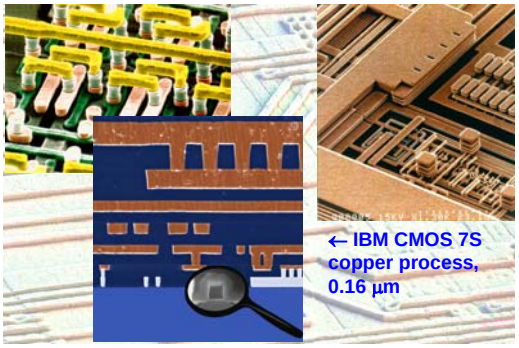
Similar for subsequent metal layers

Process Cross-section



See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

Interconnect Examples (motorola, ibm)



← IBM CMOS 7S copper process, 0.16 μm

IC Recipe Precisely Fixed

- Process conditions (temperature, time, concentration, ...) very critical
- Many strong compatibility issues of materials and processes
- Very expensive and difficult to tune
- Very expensive equipment and facilities
- Need Billions of turnover for break-even

Complex Lithographic Process

- Example: ASML TWINSCAN™ XT:1250
- Sub wave length Lithography
  193 nm KrF Laser (Deep UV)
- 65 nm resolution
- < 8 nm overlay
- > 85 WpH (300 mm)
- DOF ~ 0.50 µm (1: 600.000)
- price around 5M€
- www.asml.com
- Modern wafer fab: > 5-10B$

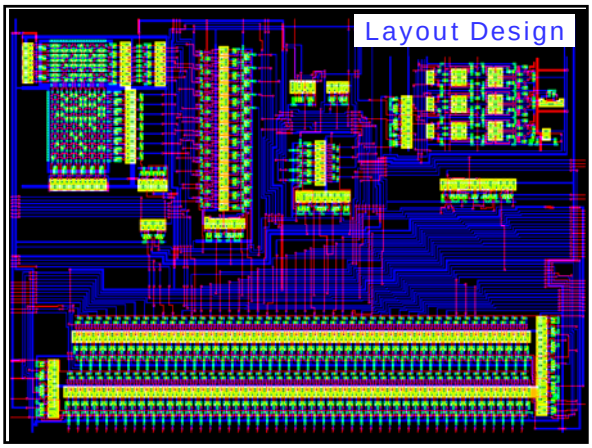
Compare Stepper Wafer Size and Resolution to NL scale

- Wafer size: ∅ 300mm
- Resolution: 45nm
- Netherlands: 40.000 km² ~ 200km x 200km

300mm	1	45nm
200km	667x10³	3cm

A 'magnified' waferstepper could 'print' the Netherlands with a resolution of 3 cm in 42 sec.

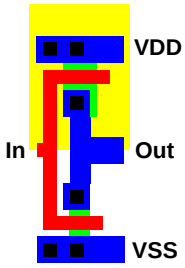
Equivalent to a 44 terabit camera (6.7x6.7 Mega pixel)



Layout Design

Layout Design Concepts

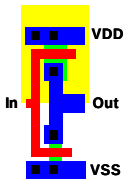
- Layer map
- Layout examples
- Stick diagrams



You should be able to understand such a drawing as well as simpler drawings called 'stick diagram'

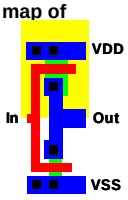
Layout Design

- Layout is design of fabrication masks
- Each mask is drawn in different color
- Layout is not a free-form drawing
  Most often: Manhattan Layout (rectangular)
  Sometimes 45-degree angles
  Curved geometry only for special applications
- Layout should obey Design Rules



Layer Map

- Layers are assigned colors and/or patterns, not always 1 to 1
- Is a matter of convention
- Site-dependent, process dependent, tool dependent
- Be prepared to reverse-engineer layer map of unknown layouts

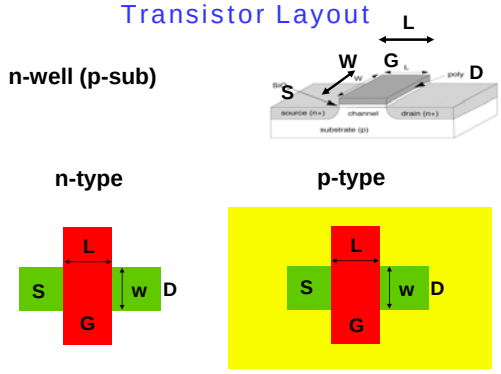


Our Reduced CMOS Layer Map

yellow	nwell	– place for P-transistors
green	active	– source and drain regions
red	polysilicon	– gate material
blue	metal 1	– first interconnect metal
black	contact, via	– hole in interlayer oxide

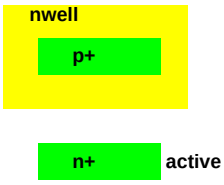
- Our layouts will be composed of these colors
- Or equivalent B/W patterns
- Compare to / instead of color plate 1
- Note: active = active area = diff = diffusion, well ≈ tub

Transistor Layout

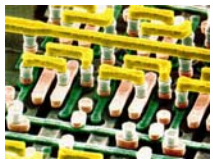


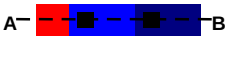
Polarity of Active Area

- Active layer or active area is the source/drain implant layer (area). Usually abbreviated as 'active' only.
- Normally, a so-called select mask determines polarity of active
- See color plate 5
- We will implicitly define polarity of active by n-well
- Or we will even omit the nwell and use the context

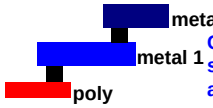


Contact Holes and Vias



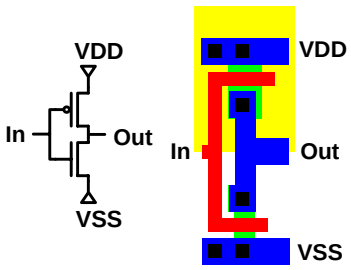


Layout (top view)



Cross-section along A-B

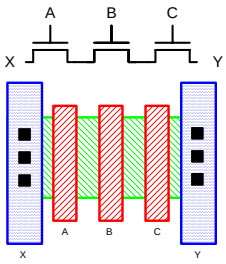
Invertor Layout



Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

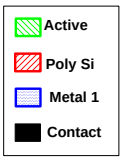
Given such a layout, you should be able to draw the circuit on the left, as well as the different cross-sections

From Schematic to Layout



Transistor schematic

Layout



Exercise

Zie onderstaande lay-out van een transistor.

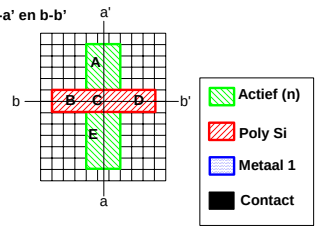
Geef voor ieder van de aansluitingen gate, source, drain aan uit welke letters A-E (zie de layout) het gebied bestaat.

G: .....

S: .....

D: .....

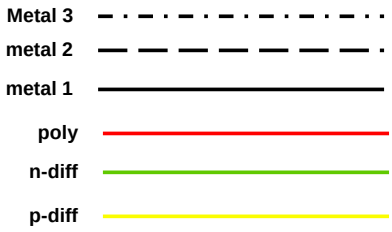
Teken een doorsnede langs a-a' en b-b'



Stick diagrams

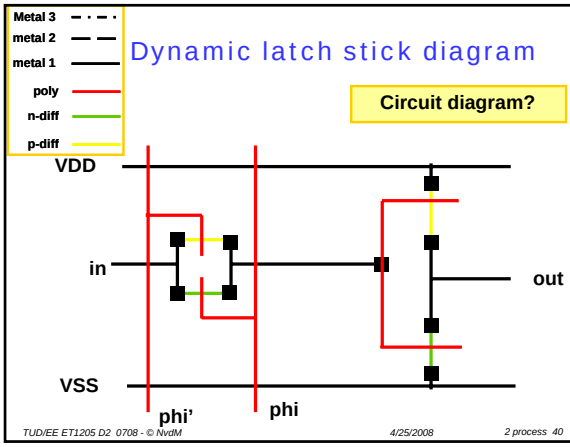
- **A stick diagram is a cartoon of a layout.**
- **Does show components/vias but only relative placement.**
- **Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.**

Stick layers



- **Caution: stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff**

Dynamic latch stick diagram

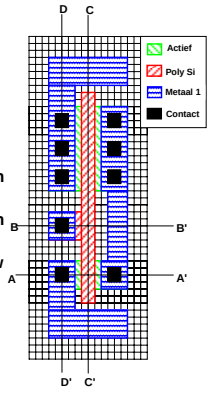


Design Rules

- **The fabrication process will suffer from tolerances**
- **Chip features will have a practical minimum size to allow them to be fabricated reliably enough (with high enough yield)**
- **This is captured into a set of precise Design Rules**
- **Modern processes have terribly complex set of design rules as a compromise between flexibility and manufacturability**
- **We will ignore this subject**
- **But you will have to understand it during OP next year.**

Zie bijgaande layout van een CMOS inverter

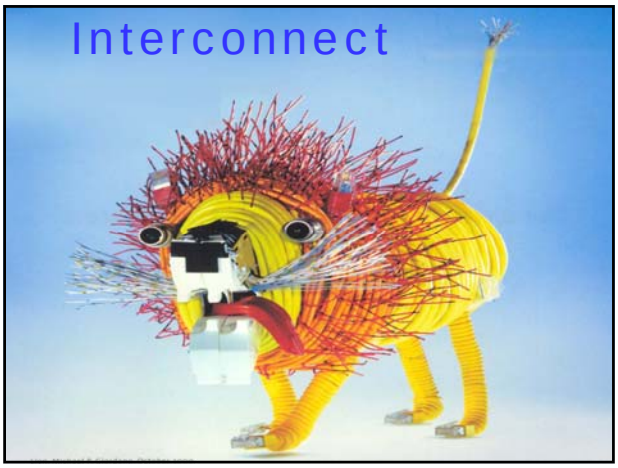
- **Teken doorsnedes langs A-A', B-B' en C-C'**
- **Welke van de twee transistoren is (vermoedelijk) de P-MOS transistor (waarom?)**
- **Teken voor deze keuze de layout van de N-well.**
- **Geef in de layout aan waar de Vss en Vdd aansluitingen zitten.**
- **Teken het transistor schema, met l/w ratio's**



Summary

- CMOS Processing
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- CMOS Process Outline
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Why we need design rules

Interconnect



Course Material for Interconnect

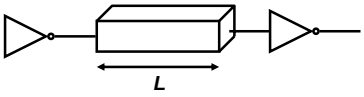
Chapter 4, 2nd ed.

P = primair, I = Illustratie, O = overslaan

P	4.1	Introduction	136
P	4.2	A First Glance	136 –138
P	4.3	Interconnect Parameters	138 – e.v.
O		So far we have …. (onder example 4.2)	147 – 148
O	4.3.3	Inductance	148 – 150
P	4.4	Electrical Wire Models	150 – 156
I	4.4.4	Distributed rc line – *hiervoor is vervangende stof*	156 – 159 (1)
O	4.4.5	The transmission line	159 – e.v.
O	4.5	Spice wire models	170 – 171
I	4.5.3	Perspective: a look into the future	171 – 174

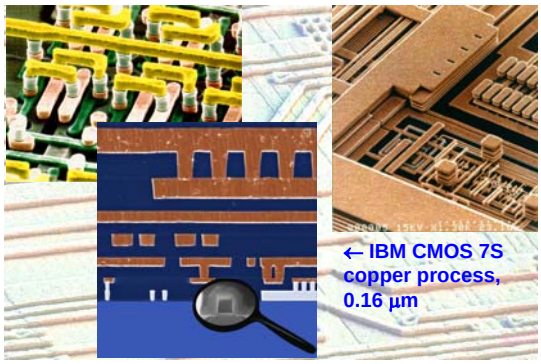
Replacement voor Distributed RC line: Elmore Delay

Interconnect



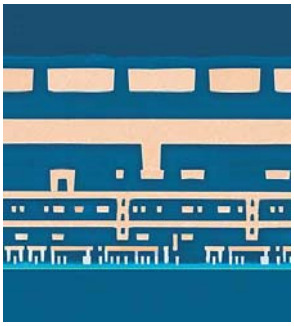
- Wires are not ideal interconnections
- They may have non-negligible capacitance, resistance, inductance
- These are called wire parasitics
- Can dominate performance of chip
- Must be accounted for during design
- Using approximate models
- Detailed post-layout verification also necessary

Wires

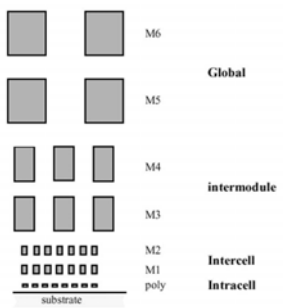


← IBM CMOS 7S copper process, 0.16 µm

Interconnect Hierarchy



Cross-section of IBM 0.13 µ process



Example Interconnect Hierarchy for typical 0.25µ process (Layer Stack)

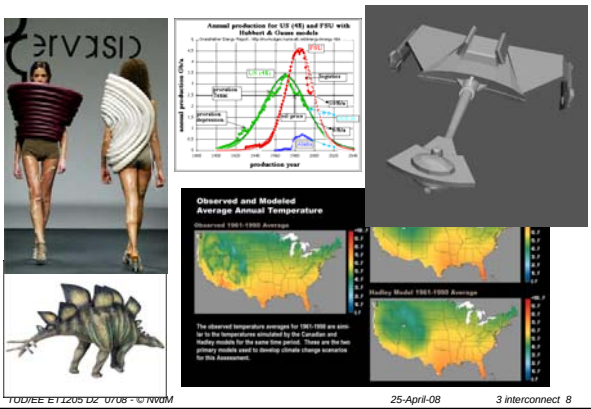
Outline

- Capacitance
  Area/perimeter model, coupling
- Resistance
  Sheet resistance
- Interconnect delay
  Delay metrics, rc delay, Elmore delay

Capacitance

- Area/perimeter model, coupling

Wake Up! Models ahead!



Merriam-Webster Online Dictionary

Thesaurus

6 entries found for **model**.
To select an entry, click on it.

model [noun]
model[2,verb]
model[3,adjective]
animal model
role model
Webster's Desk model

Go

Main Entry: [1]**mod·el**
Pronunciation:
Function: *noun*
Etymology: Middle French *modelle*, from Old Italian *modello*, from (assumed) Vulgar Latin *modellus*, from Latin *modulus* small measure, from *modus*
1 *obsolete* : a set of plans for a building
2 *dialect British* : COPY, IMAGE
3 : structural design <a home on the *model* of an old farmhouse>
4 : a usually miniature representation of something; *also* : a pattern of something to be made
5 : an example for imitation or emulation
6 : a person or thing that serves as a pattern for an artist; *especially* : one who poses for an artist
7 : ARCHETYPE
8 : an organism whose appearance a mimic imitates
9 : one who is employed to display clothes or other merchandise : MANNEQUIN

(as an atom) that cannot be directly observed

12 : a system of postulates, data, and inferences presented as a mathematical description of an entity or state of affairs

13 : VERSION

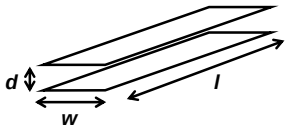
Modeling

- An abstraction of (the properties) of something to help understanding and predicting its behavior
- Domain Specific: weather, climate, economy, stock market, ...
- Different models for something to answer different questions
- Black-Box modeling vs. Physically Based

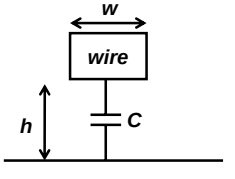
After Einstein:

a model should be as simple as possible, but not simpler

Wire Capacitance – Parallel Plate



$$C = \frac{\varepsilon_0 \varepsilon_r w l}{d}$$

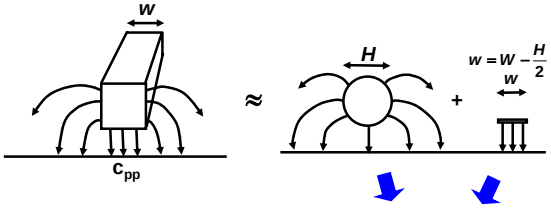


$$\frac{C}{l} = \varepsilon_0 \varepsilon_r \frac{w}{h}$$

$\varepsilon_0 = 8.85$ pF/m

$\varepsilon_r = 3.9$ (SiO_2)

Wire Capacitance – Fringing Fields



$$c_{wire} = c_{fringe} + c_{pp} = \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)} + \frac{w\varepsilon_{di}}{t_{di}}$$

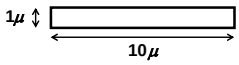
- Works reasonably well in practice
- Not directly applicable for interconnects with varying widths

Wire Capacitance – Area/Perimeter Model

- C_a was calculated with modified wire width
- Formula inapplicable for irregular interconnects (non-constant width)

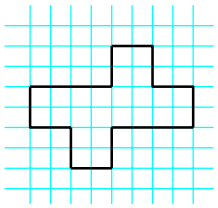
- More practical approximation

$C = A \times C_a + P \times C_p$	units	alternative
A = Area	m^2	μm^2
C_a = Area capacitance	F/m^2	$aF/\mu m^2$
P = Perimeter	m	μm
C_p = Perimeter capacitance	F/m	$aF/\mu m$



$C = \square \times C_a + \square \times C_p$

Area / Perimeter Capacitance Model

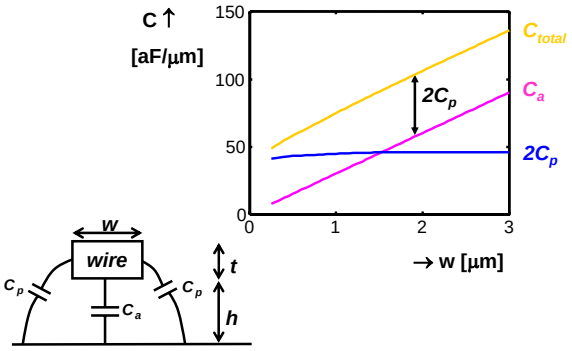


$C = \square \times C_a + \square \times C_p$

- **Question**: How to derive C_a, C_p ?

  How accurate is this model?

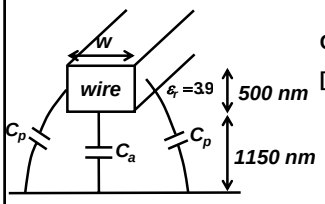
Derivation of C_a, C_p

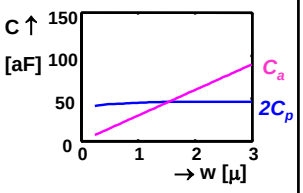


Derivation of C_a, C_p

- 2D (cross-section) numerical computation (or measurement)
- C_l : total wire capacitance per unit length
- $C_a = \varepsilon_0 \varepsilon_r / h$
- $C_p = 1/2 (C_l - C_a \times w)$
- C_p depends on t, h ➔ determined by technology, layer
- C_p would depend slightly on w (see previous graph), this dependence is often ignored in practice

Area / Perimeter Capacitance

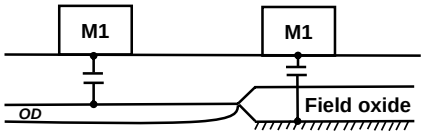




- C_p dominates for many wires
- C_p may not be neglected
- A constant value for C_p is usually a good approximation
- C_p is sometimes called C_f (fringe capacitance)

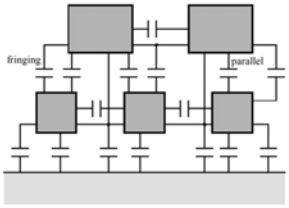
Interconnect Capacitance Design data

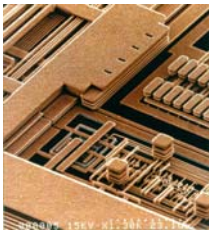
- See Table 4.2 (or inside backside cover)
- Example: M1 over Field vs. M1 over Active (hypothetical)



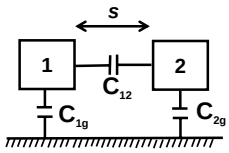
M1 over Active	M1 over Field	Unit
$C_a = 41$	$C_a = 30$	$aF/\mu m^2$
$C_p = 47$	$C_p = 40$	$aF/\mu m$

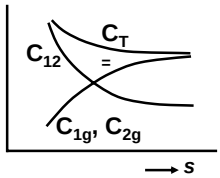
Coupling Capacitances





Coupling Capacitances (2)



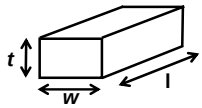


- $C_T = C_{1g} + C_{12} = C_{2g} + C_{12}$ fairly constant
- Use that as first order model
- Interconnect capacitance design data (e.g. Table 4.3)

Resistance

- **Sheet resistance**

Wire Resistance



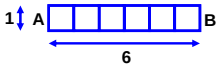
- Proportional to l
- Inversely proportional to w and t (cross-sectional area)
- Proportional to ρ: specific resistance, material property [Ωm]
- R = ρl/wt
- Aluminum: $\rho = 2.7 \times 10^{-8}$ Ωm
  Copper: $\rho = 1.7 \times 10^{-8}$ Ωm

Sheet Resistance

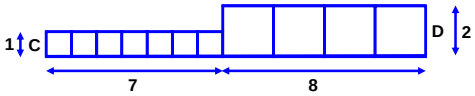
- R = ρl/wt
- t, ρ constant for layer, technology
- R = R l/w
- R : sheet resistance [Ω/]
  resistance of a square piece of interconnect
  other symbol: R_s
- Interconnect resistance design data e.g. Table 4.5 (or inside back-cover)

Interconnect Resistance

- Assume $R_\square = 40\ \Omega$
- Estimate the resistance between A and B in the wire below.



$R_{AB} \approx 6 \times 40 = 240\ \Omega$



$R_{CD} \approx 11 \times 40 = 440\ \Omega$

Engineering is about making controlled approximations to something that is too complicated to compute exactly, while ensuring that the approximate answer still leads to a working (functional, safe, …) system

Exercise

An interconnect line is made from a material that has a resistivity of $\rho = 4\ \mu\Omega$-cm. The interconnect is 1200 Å thick, where 1 Angstrom (Å) is 10^{-10} m. The line has a width of 0.6 μm.

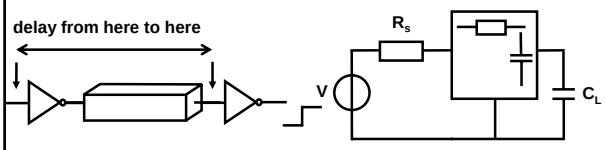
a) Calculate the sheet resistance $R_{\square}$ of the line.

b) Find the line resistance for a line that is 125 μm long.

Interconnect delay

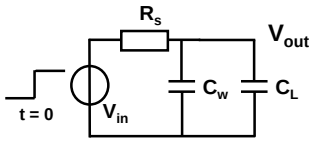
- **Delay metrics, rc delay, Elmore delay**

Delay



- Model driver as linearized Thevenin source V, R_s, assume step input
- Model load as C_L
- Wire is an RC network (two-port)

Wire Capacitance



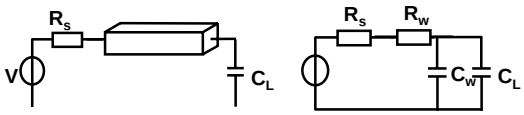
Assume wire behaves purely capacitive

$$(C_w + C_L)\frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_s} = 0$$

$$V_{out} = V_{in} - \tau\frac{dV_{out}}{dt} \qquad \tau = R_s(C_w + C_L)$$

$$V_{out} = \left(1 - e^{-t/\tau}\right)V_{in}$$

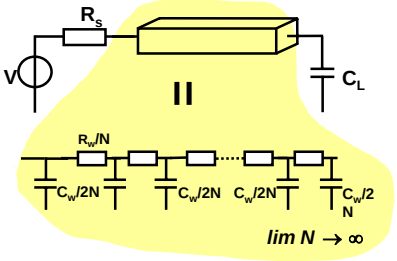
Wire Resistance



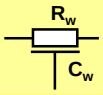
Now, assume wire capacitance *and resistance*

- $\tau = (R_s + R_w)(C_w + C_L)$
- Is this a good model?
- R and C are distributed along the wire

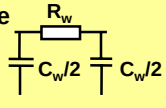
Uniform RC Line



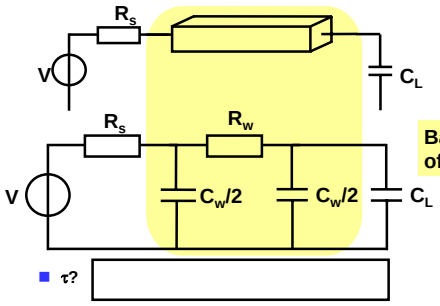
Symbol



[Always] use first order model



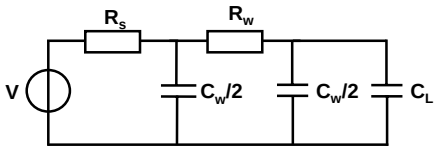
RC Delay (Uniform RC Line)



Basic π-model of wire

- τ? [ ]

Equivalent Time Constant



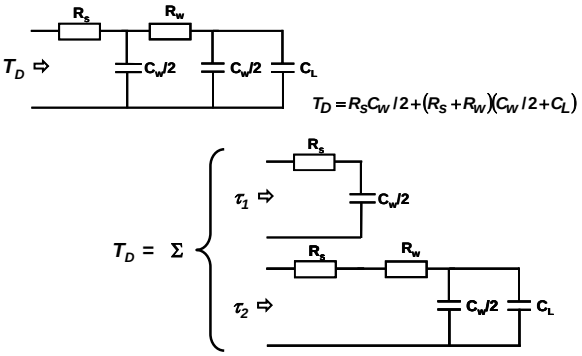
- Multiple time-constants
- Need for one "equivalent" number
- Offered by *Elmore Delay* T_D

$$T_D = R_S C_W/2 + (R_S + R_W)(C_W/2 + C_L)$$

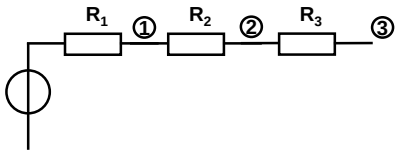
- Effective "one number" model for delay

How to compute Elmore Delay?

Equivalent Time Constant

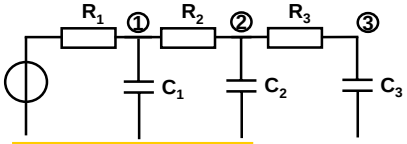


Shared Path Resistance



- Define: R_{ii} = Resistance from node i to input
- Example: $R_{11} = R_1 \quad R_{22} = R_1 + R_2 \quad R_{33} = R_1 + R_2 + R_3$
- Define: R_{ik} = Shared path resistance to input for node i and k
- $R_{12} = R_1 \quad R_{13} = R_1 \quad R_{23} =$ [ ]

Elmore Delay for RC ladders



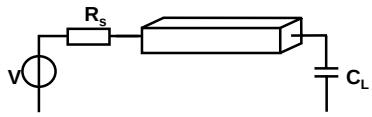
- Define: $T_{Di} = \sum_{k=1}^{N} R_{ik} C_k$

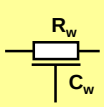
Elmore Delay

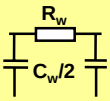
We will use $0.69 \times T_{di}$ as approximation of wire delay ($t_{50\%}$)

- $T_{D1} = R_{11}C_1 + R_{12}C_2 + R_{13}C_3 =$
  $= R_1C_1 + R_1C_2 + R_1C_3$
  $T_{D_3} = R_{31}C_1 + R_{32}C_2 + R_{33}C_3 =$
  $= R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$
- $T_{D_2} =$ [ ]

Elmore Delay for Distributed RC Lines

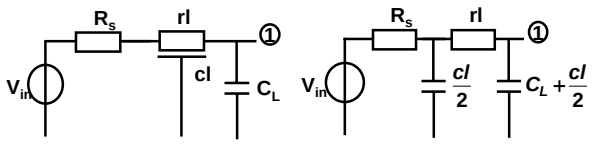


Symbol 

Symmetric π-model 

- **Theorem:** For Elmore Delay calculations, each uniform distributed RC section is equivalent to a symmetric π-model

Canonical Driver-Line-Load



- $T_{D_1} = R_s \frac{cl}{2} + (R_s + rl)\left(C_L + \frac{cl}{2}\right)$

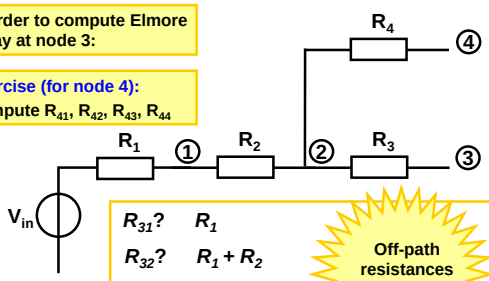
$= R_s(cl + C_L) + rlC_L + \frac{1}{2}rcl^2$

- **Delay quadratic in line length**

Shared Path Resistance for Tree Structures

In order to compute Elmore Delay at node 3:

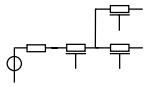
Exercise (for node 4):
Compute R_{41}, R_{42}, R_{43}, R_{44}



R_{31}?	R_1
R_{32}?	$R_1 + R_2$
R_{33}?	$R_1 + R_2 + R_3$
R_{34}?	$R_1 + R_2$

Off-path resistances don't count

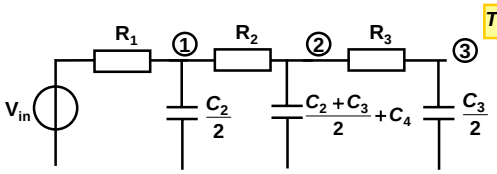
Elmore Delay for Tree Structures



Exercise: Compute T_{D1}, T_{D2}, T_{D3}, T_{D4}

- **Replace RC lines by π-sections**
- **Given observation node i, then only resistances along the path from input to node i can possibly count**
- **Make others zero**
- **Compute as if RC ladder**

T_{D3}?



Summary

- **Capacitance**
  Area/perimeter model, coupling
- **Resistance**
  Sheet resistance
- **Interconnect delay**
  Delay metrics, rc delay, Elmore delay

CMOS INVERTER

Course Material for Inverter

Chapter 5, 2nd ed.

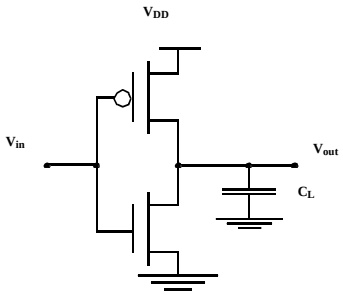
P = primair, I = Illustratie, O = overslaan

P	5.1	Introduction	180
P	5.2	The Static CMOS inverter - intuitive	181 – 184
P	1.3.2	Functionality and Robustness	18 – 27
P	5.3	Evaluating the Robustness ...	184 – 191
I	5.3.3	Robustness Revisited	191 – 193
P	1.3.3	Performance	27 – 30
I	5.4	Performance of the CMOS inverter	193 – 213
P	1.3.4	Power and Energy Consumption	30 – 31
I	5.5	Power, Energy, and Energy-Delay	213 – 223
O	5.5.2	Static Consumption	223 – 225
O	5.5.3	Putting it All Together	225 – 227
O	5.5.4	Analyzing Power Consumption using SPICE	227 – 229.
O	5.6	Perspective: Technology scaling…	229 – 231
P	5.7	Summary	232 – 233

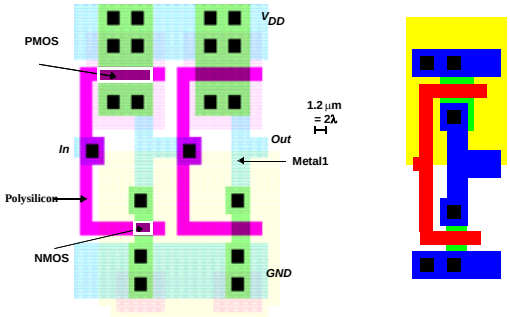
The CMOS Inverter - Outline

- First Glance
- Digital Gate Characterization
- Static Behavior (Robustness)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance)
  - Capacitances
  - Delay
- Power
  - Dynamic Power, Static Power, Metrics

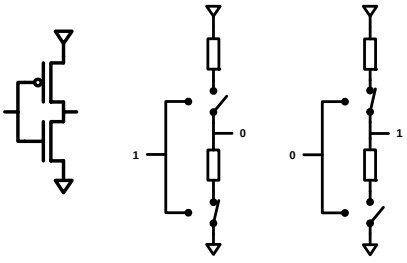
The CMOS Inverter: A First Glance



CMOS Inverters (1)



CMOS Inverter Operation Principle

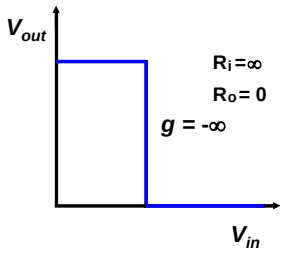


$V_{OH} = V_{DD}$ $V_{OL} = 0$

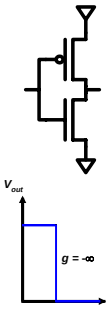
Digital Gate Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  - Speed (delay)
  - Power Consumption
  - Energy

The Ideal Inverter



Static CMOS Properties



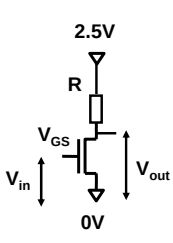
Basic inverter belongs to class of static circuits: output always connected to either V_{DD} or V_{SS}. Not ideal but:

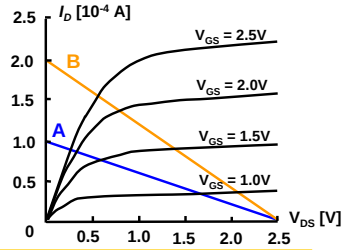
- Rail to rail voltage swing
- Ratio less design
- Low output impedance
- Extremely high input impedance
- No static power dissipation
- Good noise properties/margins

Exercise: prioritize the list above

Voltage Transfer Characteristic (VTC)

Load Line (Ckt Theory)



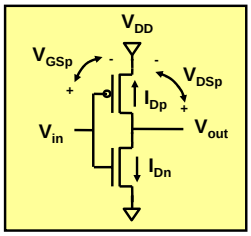


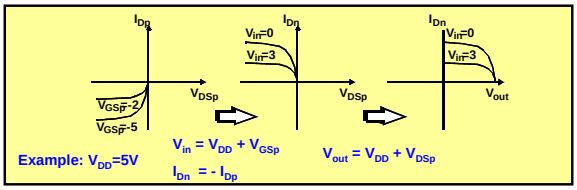
Exercise:
The blue load line A corresponds to R =
The orange load line B corresponds to R =
With load line A and V_{GS} = 1V, V_{out} =
Draw a graph $V_{out}(V_{in})$ for load line A and B

PMOS Load Lines

Goal: Combine I_{Dn} and I_{Dp} in one graph

Kirchoff:
$V_{in} = V_{DD} + V_{GSp}$
$I_{Dn} = -I_{Dp}$
$V_{out} = V_{DD} + V_{DSp}$



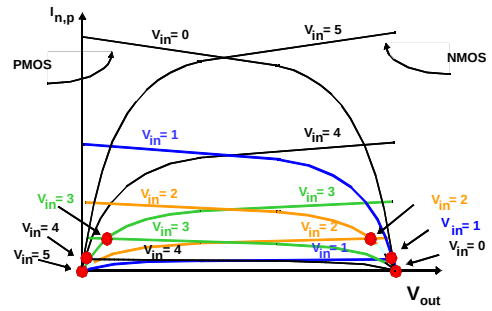


Example: V_{DD}=5V

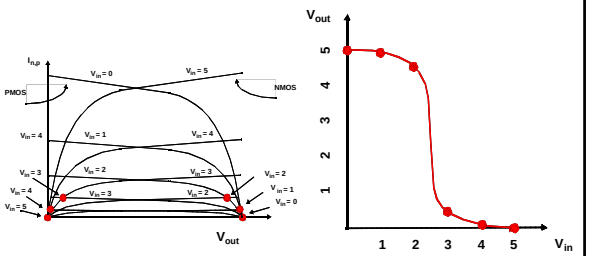
$V_{in} = V_{DD} + V_{GSp}$
$I_{Dn} = -I_{Dp}$

$V_{out} = V_{DD} + V_{DSp}$

CMOS Inverter Load Characteristics

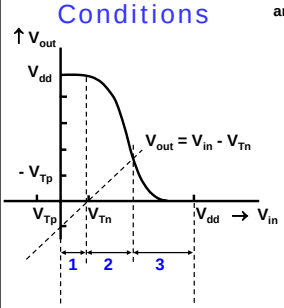


CMOS Inverter VTC



NMOS Operating Conditions

Need to know for proper dimensioning, analysis of noise margin, etc.



NMOS

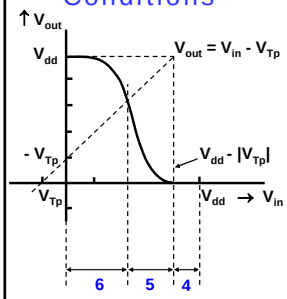
1 $V_{in} = V_{GS} < V_{Tn} \Rightarrow$ off

2 $V_{out} > V_{in} - V_{Tn}$
$V_{DS} > V_{GS} - V_{Tn}$
$V_{GD} < V_{Tn}$ $\Rightarrow$ saturation

3 $V_{out} < V_{in} - V_{Tn} \Rightarrow$ resistive

PMOS Operating Conditions

Need to know for proper dimensioning, analysis of noise margin, etc.



PMOS

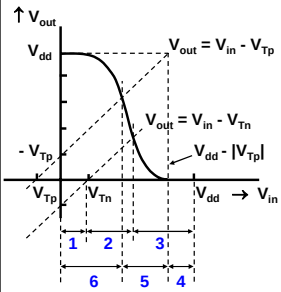
4 $V_{in} > V_{DD} + V_{Tp} \Rightarrow$ off

5 $V_{out} < V_{in} - V_{Tp} \Rightarrow$ saturation

6 $V_{out} > V_{in} - V_{Tp} \Rightarrow$ resistive

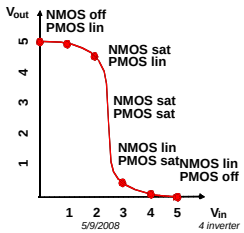
Exercise: check results for PMOS

Operating Conditions



NMOS 1 off
2 saturation
3 resistive

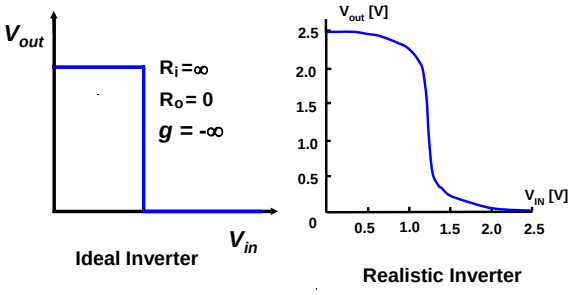
PMOS 4 off
5 saturation
6 resistive



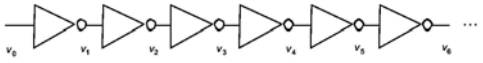
Inverter Static Behavior

- Regeneration
- Noise margins
- Delay metrics

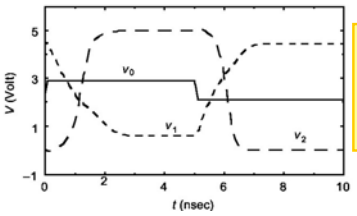
The Realistic Inverter



The Regenerative Property



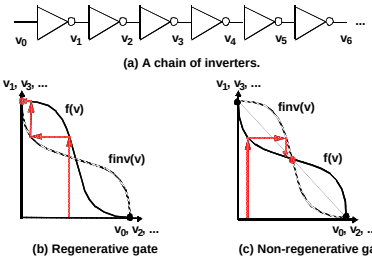
A chain of inverters



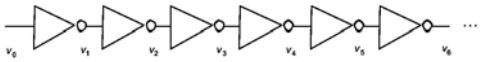
The regenerative property

- **Regenerative Property:** ability to regenerate (repair) a weak signal in a chain of gates

The Regenerative Property (2)



The regenerative Property (3)

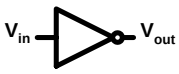


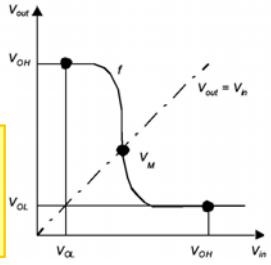
Exercise: what is the output voltage of a chain of 4 inverters with a piece-wise linear VTC passing through (0, 10), (4,8), (6,2) and (10,0) [Volt], as the result of an input voltage of 5.5 [Volt].

Exercise: discuss the behavior for an input of 5 [Volt]

Inverter Switching Treshold

- Not the device threshold $V_m = f(R_{onn}, R_{onp})$
- Point of $V_{in} = V_{out}$

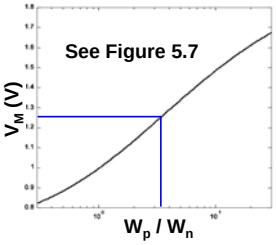




- Try to set W_n, L_n, W_p, L_p so that VTC is symmetric as this will improve noise margins

optimize NMOS-PMOS ratio

Simulated Gate Switching Threshold



Electrical Design Rule
$W_p \approx 2.5\ W_n$

- Assumes $L_p = L_n$
- Should be applied consistently

- Symmetrical VTC $\Rightarrow V_m \approx \frac{1}{2} V_{DD} \Rightarrow W_p/W_n \approx$ ☐
- In practice: choose somewhat smaller value of W_p/W_n
- Why? ☐

Inverter Switching Threshold
Analytical Derivation

- V_M is V_{in} such that $V_{in} = V_{out}$
- $V_{DS} = V_{GS} \Leftrightarrow V_{GD} = 0 \Rightarrow$ saturation
  - Assume $V_{DSAT} < V_M - V_T$ (velocity saturation)
  - Ignore channel length modulation
- V_M follows from
  - $I_{DSATn}(V_M) = - I_{DSATp}(V_M)$

§ 5.3.1

Inverter Switching Threshold
Analytical Derivation (ctd)

$$I_{DSATn}(V_M) = - I_{DSATp}(V_M) \qquad I_D = kV_{DSAT}(V_{GS} - V_T - V_{DSAT}/2)$$

$$\Leftrightarrow k_n V_{DSAT_n}(V_M - V_{Tn} - V_{DSATn}/2) = -k_p V_{DSAT_P}(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)$$

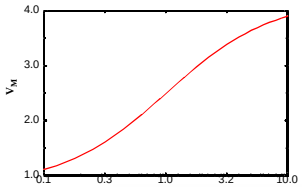
$$\Leftrightarrow \frac{k_p}{k_n} = \frac{-V_{DSAT_n}(V_M - V_{Tn} - V_{DSATn}/2)}{V_{DSAT_P}(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)} \qquad k = \frac{W}{L}k'$$

$$\Rightarrow \frac{(W/L)_p}{(W/L)_n} = \left| \frac{k'_n V_{DSAT_n}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSAT_P}(V_M - V_{DD} - V_{Tp} - V_{DSATp}/2)} \right|$$

- See Example 5.1:
- $(W/L)_p = 3.5\,(W/L)_n$ for typical conditions and $V_M = ½\ V_{DD}$
- Usually: $L_n = L_p$

Gate Switching Threshold w/o Velocity Saturation

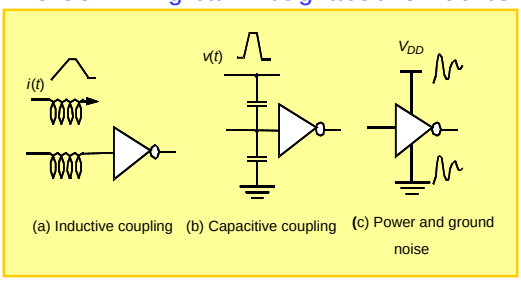
- Long channel approximation
- Applicable with low V_{DD}



Exercise (Problem 5.1): derive V_M for long-channel approximation as shown below

$$V_M = \frac{r(V_{DD} - V_{Tp} + V_{Tn})}{1+r} \quad with \quad r = \sqrt{\frac{-k_p}{k_n}}$$

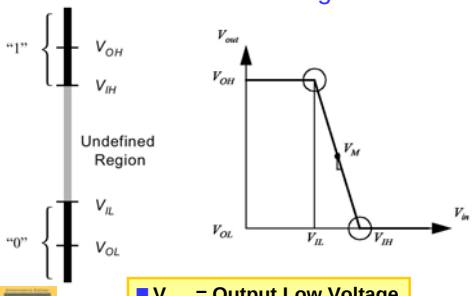
Noise in Digital Integrated Circuits



(a) Inductive coupling (b) Capacitive coupling (c) Power and ground noise

- Study behavior of static CMOS Gates with noisy signals

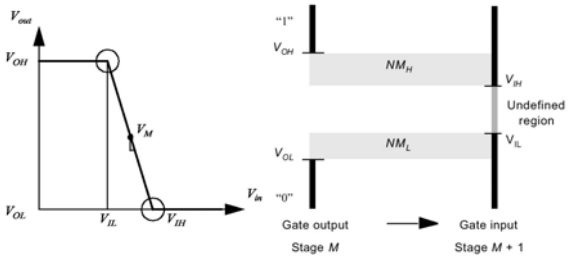
Noise Margins



§ 1.3.2

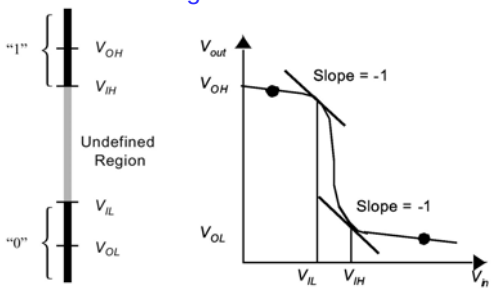
- V_{OL} = Output Low Voltage
- V_{IL} = Input Low Voltage
- V_{OH}, V_{IH} = …

Noise Margins



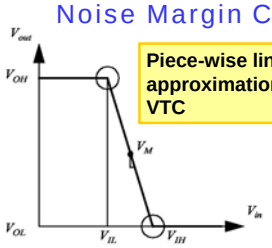
- $NM_H = V_{OH} - V_{IH}$ = High Noise Margin
- $NM_L = V_{IL} - V_{OL}$ = Low Noise Margin

Noise Margin for Realistic Gates



Exercise: explain significance of slope = -1 for noise margin

Noise Margin Calculation



Piece-wise linear approximation of VTC

g = gain factor (slope of VTC)

We know how to compute V_M
Next: how to compute g

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

§ 5.3.2

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

Noise Margin Calculation (2)

- Approximate *g* as the slope in V_{out} vs. V_{in} at $V_{in} = V_M$

$$k_n V_{DSAT_n}(V_{in} - V_{Tn} - V_{DSATn}/2)(1 + \lambda_n V_{out}) +$$

$$k_p V_{DSAT_p}(V_{in} - V_{DD} - V_{Tp} - V_{DSATp}/2)(1 + \lambda_p V_{out} - \lambda_p V_{DD}) = 0$$

$$g = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M} \approx \frac{1+r}{(V_M - V_T - V_{DSATp}/2)(\lambda_n - \lambda_p)} \qquad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

- Mostly determined by technology
- See example 5.2

- **Exercise:** verify calculation
- **Exercise:** explain why we add channel length modulation to the I_D expressions (we did not do this to determine V_M)

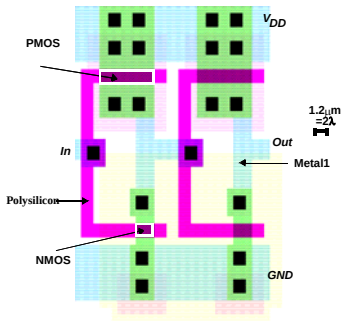
Dynamic Behavior (Performance)

- Capacitances
- Delay

§ 5.4

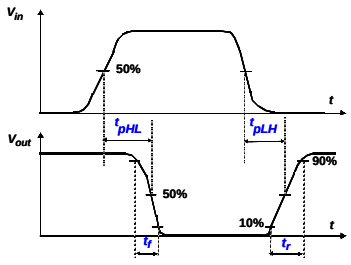
- But: we take much simpler model for capacitances compared to book.
- See the syllabus.
- § 5.4.1 of book is only illustration.

CMOS Inverters



- What causes the delay?
- What is R_{on} ?
- Where are the capacitances?
- Which capacitances determine T_p?

Delay Definitions

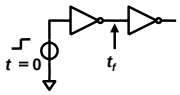


$$t_p = \frac{1}{2}(t_{pHL} + t_{pLH})$$

§ 1.3.3

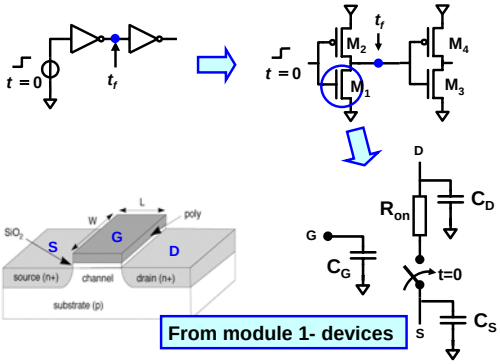
t_p : property of gate
t_r, t_f : property of signal

CMOS Inverter Rise/Fall Delay



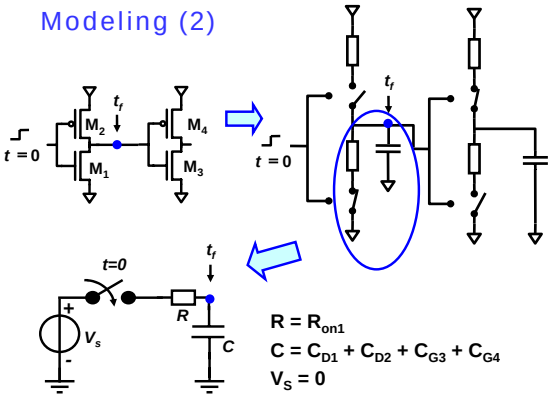
- Goal: determine t_f, t_r and t_p
- First: compute relevant capacitances
- Second: determine equivalent R_{on}
- Third: compute RC delay (τ) and scale result
- Assume: ideal source, step input

Modeling



From module 1- devices

Modeling (2)

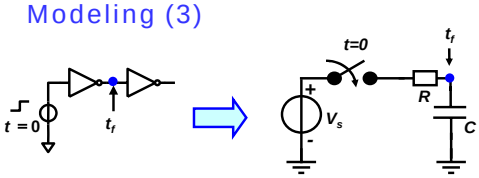


$R = R_{on1}$

$C = C_{D1} + C_{D2} + C_{G3} + C_{G4}$

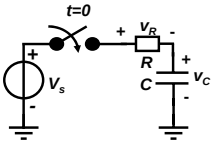
$V_S = 0$

Modeling (3)

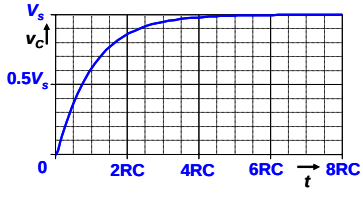


- Delay can be modeled using RC circuit
  - First order simplified model
- R is (linearized) on-resistance of active transistor
- C is sum of (linearized) C's that are switched
  - Typically, C_G of driven gate, C_D of driving gate
  - Plus relevant interconnect C
  - Might need to include interconnect R in model
- V_s is final voltage of delay node (initial voltage determined by previous state)

RC Delay Review (1)



$$v_C(t) = v_C(\infty) + (v_C(t_0) - v_C(\infty))e^{-(t-t_0)/\tau}$$



$$RC\frac{dv_C}{dt} = V_S - v_C$$

$$v_C = V_S(1 - e^{-\frac{t}{RC}})$$

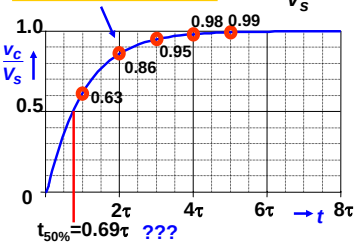
RC Delay Review (2)

- Response can be normalized with respect to $\tau = RC$ and $V_S = v_C(t = \infty)$

$$v_C = V_S(1 - e^{-\frac{t}{RC}})$$

$$\frac{v_C}{V_S} = (1 - e^{-t/\tau})$$

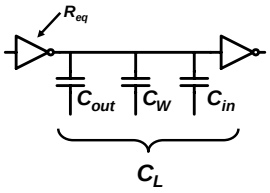
Example: $(1 - e^{-2}) = 0.86$



Each τ-step gives 63% of remaining swing

swing	time
0–50%	0.69τ
0–63%	1.0τ
10%–90%	2.2τ
0–90%	2.3τ

Inverter Propagation Delay Summary

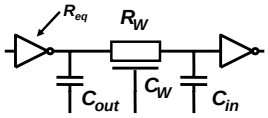


$$t_{pHL} = 0.69 R_{eqn} C_L$$

$$t_{pLH} = 0.69 R_{eqp} C_L$$

$$t_p = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right)$$ **Propagation time**

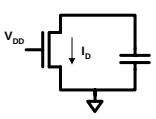
Propagation Delay w. Wire Resistance



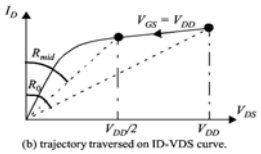
$$t_{PHL} = 0.69 R_{eqn}(C_{out} + 0.5 C_W) + 0.69(R_{eqn} + R_W)(0.5 C_W + C_{in})$$

- **See module 3, interconnect**

Equivalent R_{on} (R_{eq})



(a) Schematic



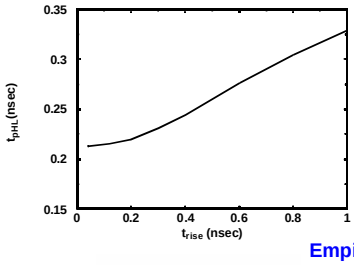
(b) trajectory traversed on ID-VDS curve.

$$R_{eq} = \frac{1}{2}\left[\frac{V_{DD}}{I_{DSAT}\left(1+\lambda V_{DD}\right)} + \frac{V_{DD}/2}{I_{DSAT}\left(1+\lambda V_{DD}/2\right)}\right]$$

$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

See 3-devices, example 3.8

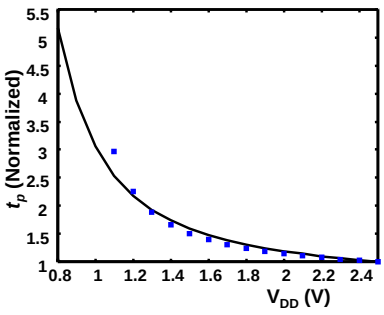
Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

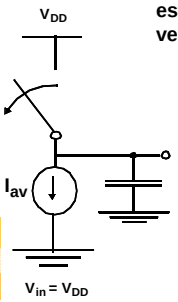
Empirical from the first edition of book

Delay as a function of V_{DD}



Fg.5.17

CMOS Inverter Propagation Delay



Alternative current-based estimate for T_p, assuming velocity saturation

$$T_{pHL} = \frac{C_L \frac{V_{swing}}{2}}{I_{av}} \approx \frac{C_L V_{DD}}{2 I_{DSAT}\left(1 + \frac{3}{4}\lambda V_{DD}\right)}$$

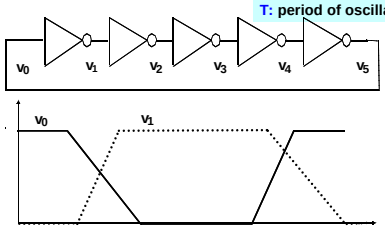
Pr. 5.4

Exercise (Problem 5.4): Derive the expression above

Ring Oscillator

Frequently used to obtain T_p by measurement (or simulation)

N: number of inverters
T_p: propagation delay
T: period of oscillation

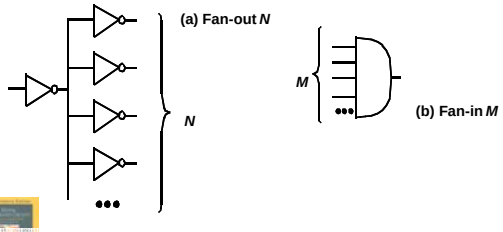


§ 1.3.3

$T = 2 \times T_p \times N \Leftrightarrow T_p = T/2N$

Exercise: explain the factor 2 in the expression above

Fan-in and Fan-out



§ 1.3.2

Power (§ 5.5)

- Dynamic Power
- Static Power
- Metrics

CMOS Power Dissipation

- Power dissipation is a very important circuit characteristic
- CMOS has relatively low static dissipation
- Power dissipation was the reason that CMOS technology won over bipolar and NMOS technology for digital IC's
- (Extremely) high clock frequencies increase dynamic dissipation
- Low V_T increase leakage
- Advanced IC design is a continuous struggle to contain the power requirements!

§ 1.3.4 § 5.5

Power Density

Estimate

- Furnace: 2000 Watt, r=10cm ➔ P ≈ 6Watt/cm^2
- Processor chip: 100 Watt, 3cm^2 ➔ P ≈ 33Watt/cm^2

Power-aware design, design for low power, is blossoming subfield of VLSI Design

Where Does Power Go in CMOS

- Dynamic Power Consumption
  - Charging and discharging capacitors
- Short Circuit Currents
  - Short circuit path between supply rails during switching
- Leakage
  - Leaking diodes and transistors
  - May be important for battery-operated equipment

Dynamic Power

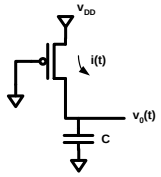
Dynamic Power

- E_i = energy of switching event i
  - (to first order) independent of switching speed
  - depends on process, layout
- Power = Energy/Time

$$P = \frac{1}{T}\sum_i E_i$$

- E_i = Power-Delay-Product P-D
  - important quality measure
- Energy-Delay-Product E-D
  - combines power*speed performance

Low-to-High Transition Energy



Equivalent circuit for low-to-high transition

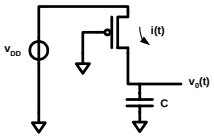
E_C - Energy stored on C

$$E_C = \int_0^\infty i v_0 dt \qquad v_0 = v_0(t) \qquad i = i(t) = C\frac{dv_0}{dt}$$

$$= \int_0^\infty C v_0 \frac{dv_0}{dt} dt$$

$$= \int_0^{V_{DD}} C v_0 dv_0 = \frac{1}{2} C v_0^2 \Big|_0^{V_{DD}} = \frac{1}{2} C V_{DD}^2$$

Low-to-High Transition Energy



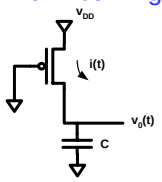
$E_{V_{DD}}$ Energy delivered by supply

$$E_{V_{DD}} = \int_0^\infty i(t) V_{DD} dt = \int_0^{V_{DD}} C V_{DD} \frac{dv_0}{dt} dt = C V_{DD}^2$$

$$E_{V_{DD}} = C V_{DD}^2 \qquad E_C = \frac{1}{2} C V_{DD}^2$$

Where is the rest?

Low-to-High Transition Energy



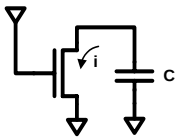
E_{diss} Energy dissipated in transistor

$$E_{diss} = \int_0^\infty i(V_{DD} - v_0) dt$$

$$= \int_0^\infty i V_{DD} dt - \int_0^\infty i v_0 dt$$

$$= E_{V_{DD}} - E_C$$

High-to-Low Transition Energy



Equivalent circuit

Exercise: Show that the energy that is dissipated in the transistor upon discharging C from V_{DD} to 0 equals $E_{diss} = ½CV_{DD}^2$

CMOS Dynamic Power Dissipation

$$Energy = E_{charge} + E_{discharge}$$

$$Power = \frac{Energy}{Time} = \frac{Energy}{transition} \times \frac{\#\,transitions}{time}$$

$$= C V_{DD}^2 \times f$$

- Independent of transistor on-resistances
- Can only reduce C, V_{DD} or f to reduce power
- In this formula, f accounts for switching activity (not necessarily a simple regular waveform)

Summary

- First Glance
- Digital Gate Characterization (§ 1.3)
- Static Behavior (Robustness) (§ 5.3)
  - VTC
  - Switching Threshold
  - Noise Margins
- Dynamic Behavior (Performance) (§ 5.4)
  - Capacitances
  - Delay
- Power (§ 5.5)
  - Dynamic Power, Static Power, Metrics

MODULE 5

COMBINATIONAL LOGIC

Course Material for Combinational

Extra: Slides about how to implement a static combinational gate with NMOS/PMOS transistors, given the Boolean function

P	6.1	Introduction	236
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P	6.2.1	Complementary CMOS	237 – 242
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I	6.3.1	Dynamic Logic: Basic Principles	284 – 286
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I	6.3.3	Signal Integrity Issues in Dynamic Design	290 – 295
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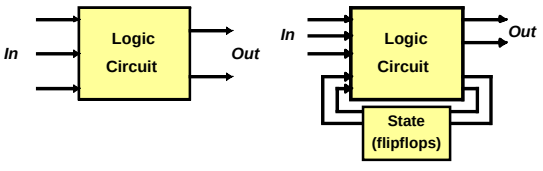
O	6.4	Perspectives	303 – 306
P	6.5	Summary	306 – 307

Combinational Logic - Outline

- Conventional Static CMOS basic principles
- Complementary static CMOS
  - Complex Logic Gates
  - VTC, Delay and Sizing
- Ratioed logic
- Pass transistor logic
- Dynamic CMOS gates ➔only illustration

Complementary Static CMOS Basic Principles

Combinational vs. Sequential Logic



(a) Combinational

Output = *f* (In)

(b) Sequential

Output = *f* (In, History)

Reminder

DeMorgan Transformations

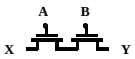
$$\overline{A+B} = \overline{A}.\overline{B}$$

$$\overline{A.B} = \overline{A}+\overline{B}$$

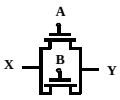
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B



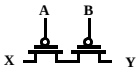
Y = X if A or B

§ 6.2.1

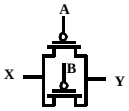
PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low

Y = X if ...

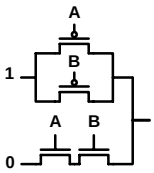


Y = X if $\overline{A}$ and $\overline{B}$



Y = X if $\overline{A}$ or $\overline{B}$

2-Input Nand



$Y = 1$ if $\overline{A}$ OR $\overline{B}$

$Y = 1$ if $\overline{A}$ AND $\overline{B}$ } DeMorgan

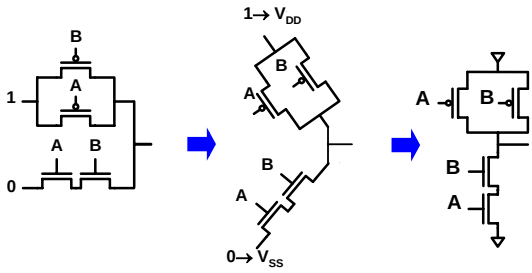
$Y = \overline{A \text{ AND } B}$

$Y = 0$ if A AND B

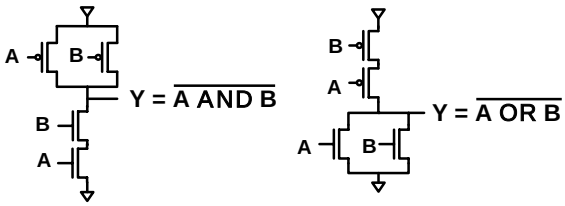
B	A	Y
0	0	1
0	1	1
1	0	1
1	1	0

2-Input Nand

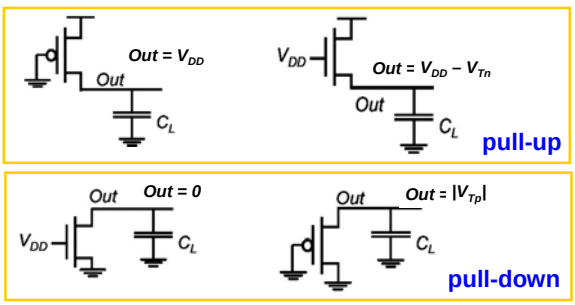
$Y = \overline{A \text{ AND } B}$



2-input Nand/Nor

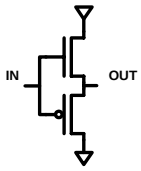


NMOS vs. PMOS, pull-down vs. pull-up



- PMOS is better pull-up
- NMOS is better pull-down

Bad Idea



Exercise: Determine logic function

Determine V_{out} for $V_{in} = V_{DD}$ and $V_{in} = V_{SS}$

Why is this a bad circuit?

CMOS Gate is Inverting

Assume full-swing inputs (high = V_{DD}, low = V_{SS})

- Highest output voltage of NMOS is
  $V_{GS} - V_{Tn} = V_{DD} - V_{Tn}$
- An 1 on NMOS gate can produce a strong 0 at the drain, but not a strong 1
- Lowest output voltage of PMOS is
  $V_{DD} + V_{GS} - V_{Tp} = |V_{Tp}|$
  (with V_{GS}, $V_{Tp} < 0$ for PMOS)
- An 0 on PMOS gate can produce a strong 1 at the drain, but not a strong 0
- Need NMOS for pull-down, PMOS for pull-up

  A 1 at input can pull-down, 0 at input can pull-up
  A 1 can produce a 0, a 0 can produce a 1

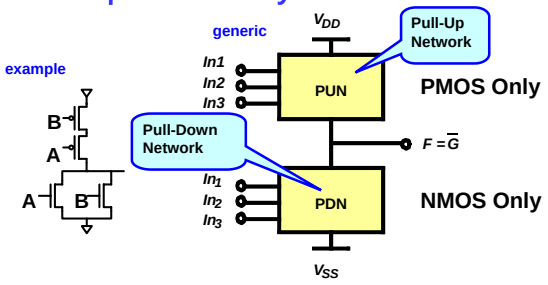
Inverting behavior

For a non-inverting Complementary CMOS Gate, you can only use 2 inverting gates

Complementary static CMOS

- Complex Logic Gates
- VTC, Delay and Sizing

Complementary Static CMOS

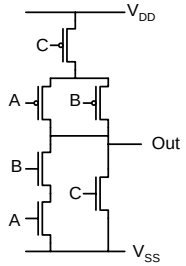


§ 6.2.1

- Conduction of PDN and PUN must be mutually exclusive (Why?)
- Pull-up network (PUN) and pull-down network (PDN) are dual

Mutual Exclusive PDN and PUN

Out = (AB + C)'



C	B	A	PDN	PUN	Out	
0	0	0	?	1	1	PDN Off, PUN On
0	0	1	?	1	1	
0	1	0	?	1	1	
0	1	1	0	?	0	PUN Off, PDN On
1	0	0	0	?	0	
1	0	1	0	?	0	
1	1	0	0	?	0	
1	1	1	0	?	0	

For all Complementary Static CMOS Gates, either the PUN or the PDN is conducting, but never both.

Complementary Static CMOS (2)

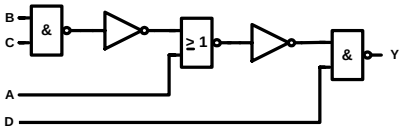
- Conduction of PUN and PDN must be mutually exclusive
- PUN is dual (complement) network of PDN
  series ⇔ parallel
  nmos ⇔ pmos
- Complementary gate is inverting
- No static power dissipation
- Need 2N transistors for N-input gate

Implementation of Combinational Logic

- How van we construct an arbitrary combinational logic network in general, using NMOS and PMOS transistors (using Complementary static CMOS)?
- Example: $Y = \overline{(A + BC)D}$
- Remember: only inverting gates available

Implementation of Combinational Logic

- Example: $Y = \overline{(A + BC)D}$
- Remember: only inverting gates available
- Logic depth: number of gates in longest path ⇨ DELAY

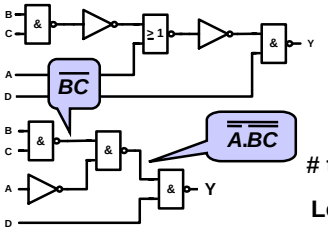


transistors ☐ logic depth ☐

- Q: Can this be improved?

Improved Gate Level Implementation

- Using DeMorgan $A + BC = \overline{\overline{A}.\overline{BC}}$



$Y = \overline{(A + BC)D}$

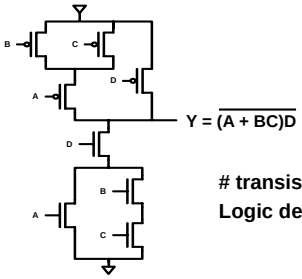
transistors ☐

Logic depth ☐

- Q: Can this be further improved?

Complex CMOS Logic Gates

- Restriction to basic NAND, NOR etc. not necessary
- Easy to synthesize complex gates



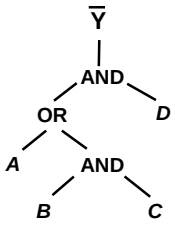
$Y = \overline{(A + BC)D}$

transistors: 8

Logic depth: 1

How to Synthesize Complex Gates

$Y = \overline{(A + BC)D}$

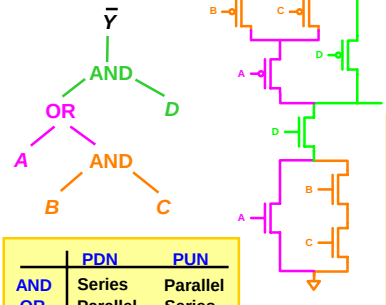


- Using tree representation of Boolean function
- *Operator* with branches for *operands*
- As a series-parallel network

	PDN	PUN
AND	Series	Parallel
OR	Parallel	Series

Complex Gate Synthesis Example

$\overline{Y} = (A + (BC))D$

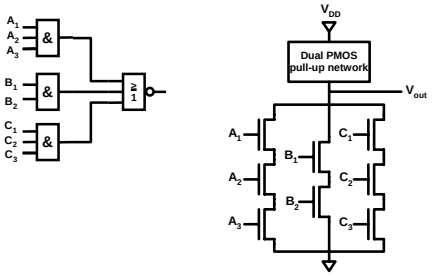


	PDN	PUN
AND	Series	Parallel
OR	Parallel	Series

Recipe

- Write $\overline{Y}$ = f(inputs)
- Decompose f in tree form
- Realize tree branches according to table at bottom-left
- Use inverted inputs if necessary

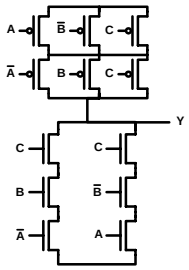
And-Or-Invert Gate



And-Or-Invert Example

- From a Truth-Table: take 0-outputs

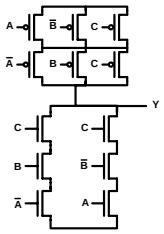
A	B	C	Y	
0	0	0	1	
0	0	1	1	
0	1	0	1	
0	1	1	0	→ $\bar{A}BC$
1	0	0	1	
1	0	1	0	→ $A\bar{B}C$
1	1	0	1	
1	1	1	1	



$\bar{Y} = \bar{A}BC + A\bar{B}C$

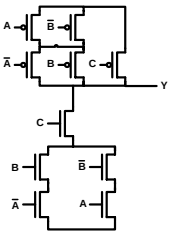
$\bar{A}$, $\bar{B}$ to be created with extra inverters (or by restructuring previous circuits)

And-Or-Invert Improvement



$\overline{Y = \bar{A}BC + A\bar{B}C}$

12 transistors

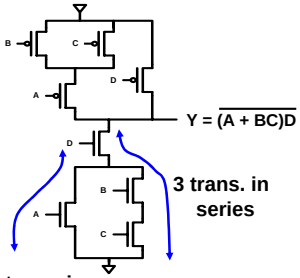


$\overline{Y = (\bar{A}B + A\bar{B})C}$

10 transistors

2-level logic minimization: see Katz (CS1), § 2.3

CMOS Complex Gate Sizing



3 trans. in series

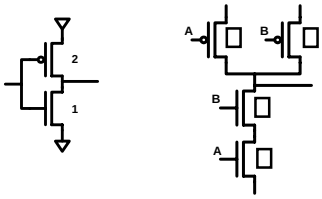
2 trans. in series

- Function of gate independent of transistor sizes: ratio-less
- But current-drive capability depends on transistor sizes
- Worst-case current-drive depends on number of transistors in series

CMOS Complex Gate Sizing

- Assume all transistors will have mininum length L
- Determine W_n for PDN transistor of inverter that would give the desired 'drive strength'
- For each transistor in PDN of complex gate do the following:
  - Determine the length l of the longest PDN chain in which it participates
  - Set $W = l\ W_n$
- Repeat this procedure for PUN, using W_p for PUN transistor of inverter.

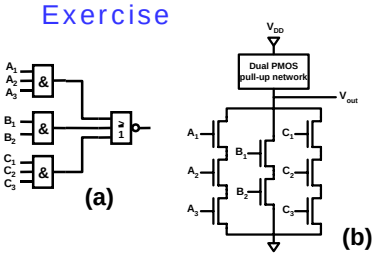
Gate Sizing



- W/L ratios
- what are the W/L of 2-input NAND for same drive strength?

0-th order calculation

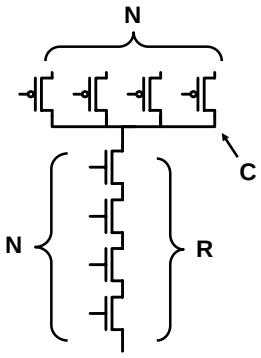
Exercise



Exercise:

- Perform gate sizing of (a) for nominal drive strength equal to that of min size inverter, assume PU/PD = 3
- Determine PUN of (b)
- Perform gate sizing of (b) for same drive strength (same PU/PD)
- Compare sum of gate areas in (a) and (b). Note: area ~ width

Avoid Large Fan-In



C linear in N

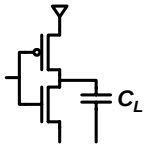
R linear in N

Delay ∝ RC quadratic in N

Empirical

Delay = $a_1FI + a_2FI^2 + a_3FO$

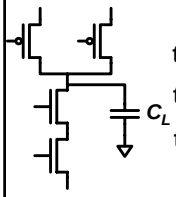
Data-Dependent Timing



$t_{PHL} = 0.69R_NC_L$

$t_{PLH} = 0.69R_PC_L$

You should be able to identify the transistor paths that charge or discharge C_L, and calculate resulting RC delay model, including effects of wires and fan-out

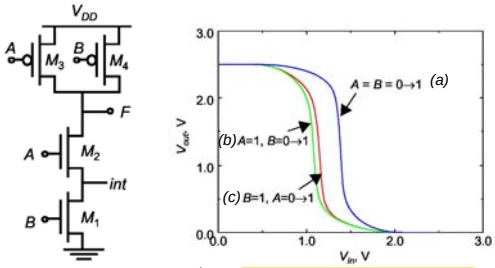


$t_{PHL} = 0.69(R_N \times 2)C_L$ Series connection

$t_{PLH} = 0.69R_pC_L$ One input goes low

$t_{PLH} = 0.69(R_p/2)C_L$ Two inputs go low, parallel connection

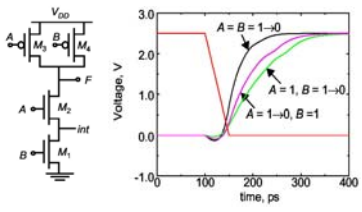
Data-dependent VTC: 2nd order effects



- Charge at 'int'
- Body effect in M_2
- Short-circuit currents

- Don't need to be able to work with these effects
- But remember: there is more going on than shown by our simple, 1st order model

Data-dependent Timing (2)

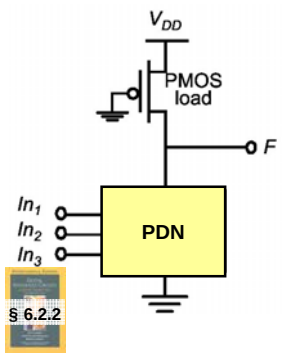


Input Data Pattern	Delay (pS)
A = B= 0→1	69
A = 1, B= 0→1	62
A= 0→1, B = 1	50
A=B=1→0	35
A=1, B = 1→0	76
A= 1→0, B = 1	57

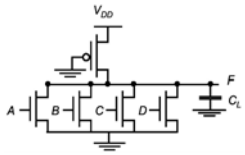
Ratioed logic

Pass transistor logic

Pseudo NMOS Ratioed Logic



- ☺ Reduced area
- ☺ Reduced capacitances
- ☹ Increased V_{OL}
- ☹ Reduced noise margins
- ☹ Static dissipation



Ratioed Logic V_{OL} Computation

I_{Dn} (linear) = I_{Dp} (saturation)

Exercise: verify these assumptions/steps

$$k_n\left((V_{DD}-V_{Tn})V_{OL}-\frac{V_{OL}^2}{2}\right)=k_p\left((-V_{DD}-V_{Tp})V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Ignore quadratic terms (they are relatively small)

$$k_n(V_{DD}-V_{Tn})V_{OL}\approx k_p(-V_{DD}-V_{Tp})V_{DSAT}$$

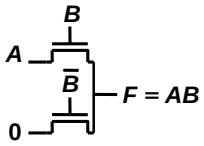
Ignore, because approximately equal

$$V_{OL}\approx\frac{k_p}{k_n}|V_{DSAT}|\approx\frac{\mu_p W_p}{\mu_n W_n}|V_{DSAT}|$$

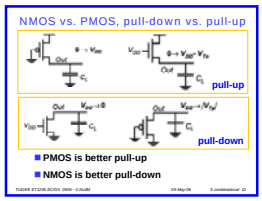
Pass-transistor and Pass-gate circuits

Pass Transistor Logic

- Save area, capacitances
- Need complementary inputs (extra inverters)

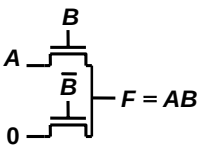


But remember:



Pass Transistor Logic

- Save area, capacitances
- Need complementary inputs (might mean extra inverters)
- Reduced V_{OH}, noise margins

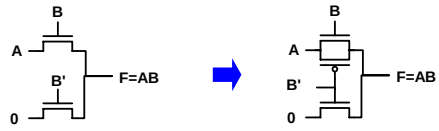


- $V_{OH}=V_{DD}-\left(V_{Tno}+\gamma\left(\sqrt{|2\phi_f|+V_{OH}}-\sqrt{|2\phi_f|}\right)\right)$
- Static dissipation in subsequent static inverter/buffer
- Disadvantages (and advantages) may be reduced by complementary pass gates (NMOS + PMOS parallel)

Exercise: Why is there static dissipation in next conventional gate?

Pass Gates

- Remedy: use an N-MOS and a P-MOS in parallel

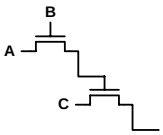


- Pass gates eliminate some of the disadvantages of simple pass-transistors
- But also some of the advantages
- Design remains a trade-off!

Pass-gate a.k.a. Transmission-gate

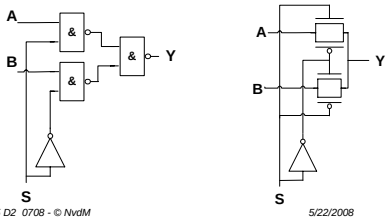
Exercise

- Discuss what happens when you connect the output of a single pass-transistor (not a pass-gate) to the input of another pass-transistor stage (i.e. the gate of another pass-transistor). Why should you never use such a circuit?



Pass Transistor Logic

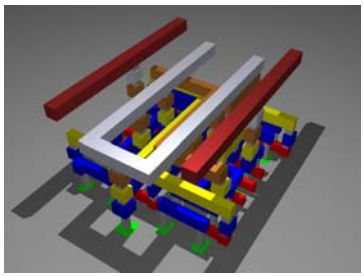
- Most typical use: for multiplexing, or path selecting
- Assume in circuit below it is required to either connect A or B to Y, under control by S
- Y = AS + BS' (S' is easier notation for S-bar = S-inverse = $\overline{S}$)
- Y = ((AS)' (BS)')' allows realization with 3 NAND-2 and 1 INV: 14 transistors
- Pass gate needs only 6 (or 8) transistors (see also Katz, section 4.2)



Summary

- Conventional Static CMOS basic principles
- Complementary static CMOS
  - Complex Logic Gates
  - VTC, Delay and Sizing
- Ratioed logic
- Pass transistor logic

MODULE 6



SEQUENTIAL ELEMENTS

§ 7.5 Will be discussed with module 08 timing design

Sequential Elements - Outline

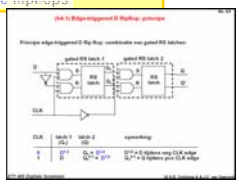
- Background
  - Timing, terminology, classification
- Static Flipflops
  - Latches
  - Registers
- Dynamic Flipflops
  - Latches
  - Registers
- Non-bistable elements
  - Schmitt Trigger

- Much of this material has already been covered in CS1 (v Genderen), Lecture 4(?), Katz Section 6.1
- Here we will add transistor-level implementation, dynamic flipflops

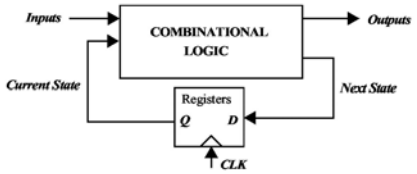

Ch. 7


Ch. 6

[Sorin Cotofana]



FSM with Positive Edge Triggered Registers




§ 7.1

- Flip-flops provide memory/state
- VLSI uses predominantly D-type flip-flops

Memory elements

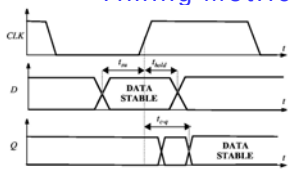
- Store a temporary value, remember a state
- Typically controlled by clock.
- May have load signal, etc.
- In CMOS, memory is created by:
  - capacitance (dynamic);
  - feedback (static).

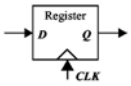
- Also see http://en.wikipedia.org/wiki/Flip-flop_(electronics)

Variations in memory elements

- Form of required clock signal.
- How behavior of data input around clock affects the stored value.
- When the stored value is presented to the output.
- Whether there is ever a combinational path from input to output.

Timing Metrics Reminder





$t_{c\text{-}q}$: delay from clock (edge) to Q
t_{su} : setup time
t_{hold} : hold time
t_{plogic} : worst case propagation delay of logic
t_{cd} : best case propagation delay (contamination delay)
T : clock period

$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$
$t_{cdregister} + t_{cdlogic} \geq t_{hold}$

Nomenclature

Beware for confusion

	Katz (CS1)	Rabaey
Latch	Level sensitive storage element	Level sensitive storage element
Register	Group of storage elements	Edge triggered storage element
Flip Flop	Edge triggered storage element	Bistable element using feedback

CLK = CK=ϕ

Latches vs. Registers

Latch

- Level-sensitive
- Transparent when clock is active
- Clock active high: positive latch
- Clock active low: negative latch
- Faster, smaller

Register

- Edge-triggered
- Input and output isolated
- Sampling on 0 → 1 clock: positive edge triggered
- Sampling on 1 → 0 clock: negative edge triggered
- Safer

Static vs. Dynamic Memory Elements

Static

- Operate through positive feedback
- Preserve state as long as power is on
- Can work when clock is off
- More robust

Dynamic

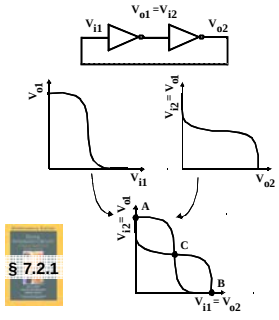
- Store charge on (parasitic) capacitor
- Charge leaks away (in milliseconds)
- Clock must be kept running (for periodic refresh)
- Faster, smaller

Rabaey: bistable elements are called Flip Flops

Static Latches and Registers

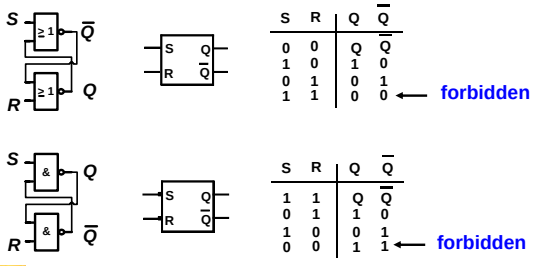
- Latches ➔ can be gated or not
- Registers

Positive Feedback: Bi-Stability



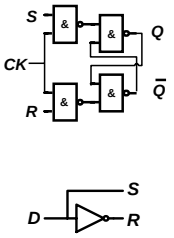
- Loop-gain in A,B <<1
- A,B: stable points
- Loop-gain in C >> 1
- C: meta-stable point

SR-Latch



§ 7.2.5

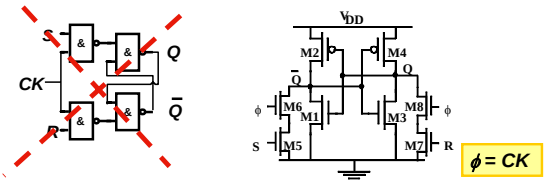
Clocked SR-Latch



- Katz: gated latch
- Positive latch (active on CK high)
- Naïve implementation
- 16 transistors
- D latch requires 9xN, 9xP
- Larger area, cost, power

- Construction of D-latch
- D-latch, D-register most common in VLSI

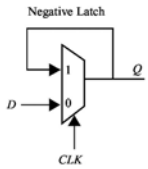
CMOS Clocked SR-Latch



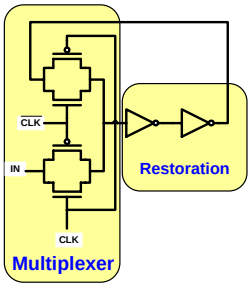
- Save 6 (incl. 4 large) PMOS transistors and 2 NMOS
- D-latch requires 7 x N, 3 x P (instead of 9xN, 9xP)

Q: Is this a ratioed design or not?
Does it consume static power?

Multiplexer-Based Latches



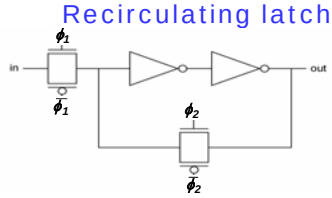
Recirculating latch



§ 7.2.2

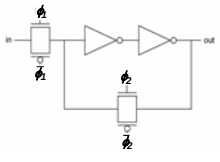
Mux-based latches much more common in modern dig. IC's

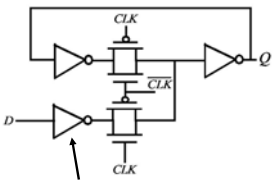
Recirculating latch



- Quasi-static, static on one phase
- Feedback restores value
- Requires 4 x N, 4 x P, minimum size
  (compare 7 x N, 3 x P, non-minimum size)
- ϕ_1 and ϕ_2 inverse but should be non-overlapping
- Can suffer from charge sharing (when ϕ not non-overlapping)
  C_{in} and C_{load} form communicating vessels when Output connected directly to input

Insensitive for Charge Sharing

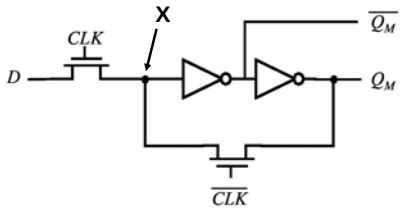




Uni-directionality of this inverter prevents coupling between Q and D

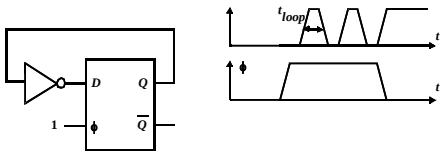
- Non ratioed
- High load to CLK

Recirculating NMOS Latch.



- Degraded 1 at X
- Lower noise margin, higher delay, power

Latch Designs can Suffer from Race Problems



§ 7.2.3

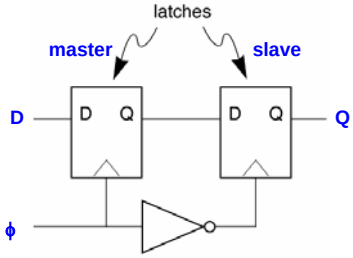
Signal can race around during $\phi = 1$

Registers

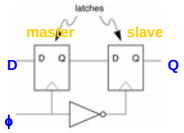
- Not transparent—use multiple storage elements to isolate output from input.
- Master-slave, edge triggered principle

§ 7.2.3

§ 6.1.4-5

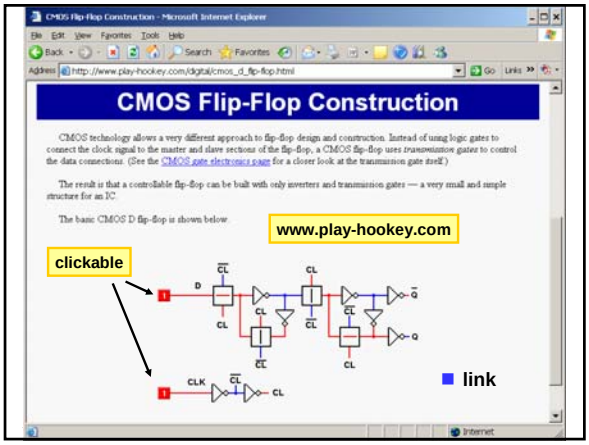


Master-slave operation

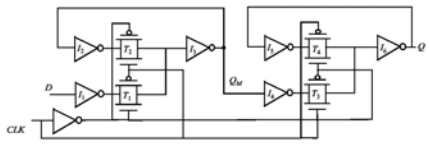


$\phi = 0$:
- master latch is disabled;
- slave latch is enabled,
- but master latch output is stable,
- so output does not change.

$\phi = 1$:
- master latch is enabled,
- loading value from input;
- slave latch is disabled,
- maintaining old output value.

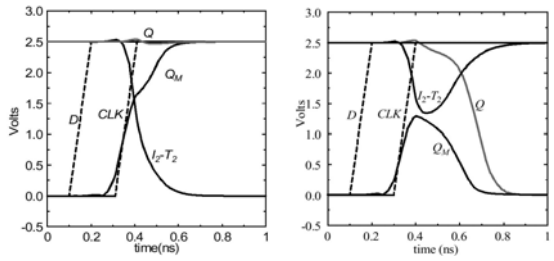


Transistor Level Master Slave Positive Edge Triggered Register



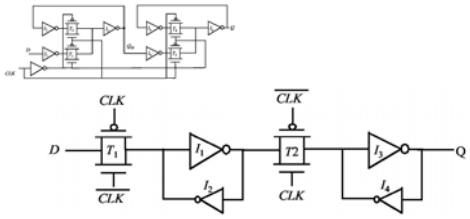
- Robust Design
- Can eliminate I_1 and I_4, however, they make design more robust (avoid charge sharing, robust input)
- High Clock Load (8 x)

Set-up Time Simulation



Slightly smaller delay between D and CLK

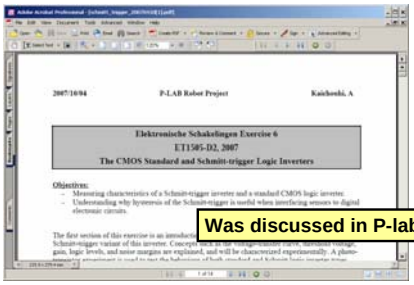
Ratioed Reduced Clock Load Register



- I_2 and I_4 are small, even long
- Lower clock load
- Increased design complexity
- Reduced robustness (reverse conduction)

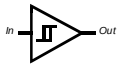
Non-bistable Elements

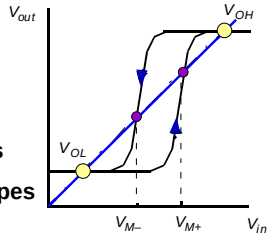
- Schmitt Trigger



Was discussed in P-lab

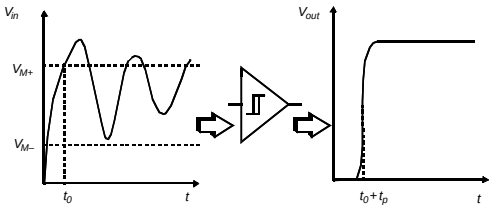
Schmitt Trigger



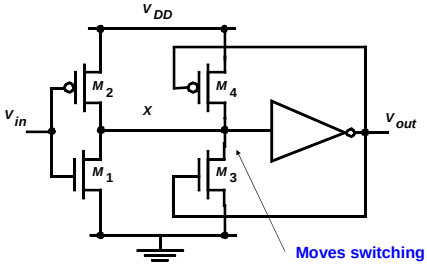


- VTC with hysteresis
- Restores signal slopes

Noise Suppression using Schmitt Trigger

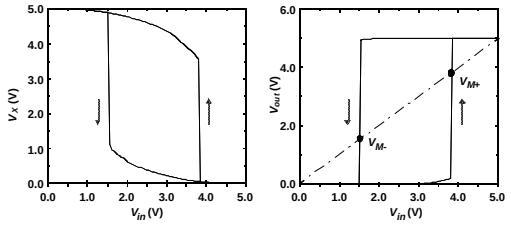


CMOS Schmitt Trigger

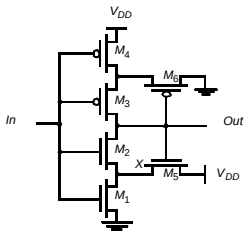


Moves switching threshold of first inverter

Schmitt Trigger Simulated VTC



CMOS Schmitt Trigger (2)

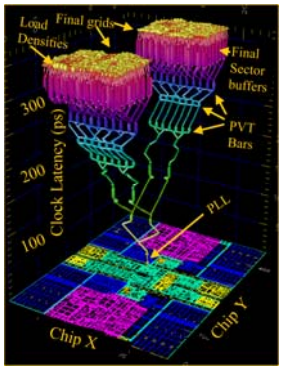


Summary

- **Background**
  - **Timing, terminology, classification**
- **Static Flipflops**
  - **Latches**
  - **Registers**
- Dynamic Flipflops
  - Latches
  - Registers
- **Non-bistable elements**
  - **Schmitt Trigger**

MODULE 7

TIMING DESIGN



Course Material for Timing Design

P	10.1	Introduction	492
I	10.2	Timing Classification	492 – 495
P	10.3.1	Synchronous Timing Basics	495 – 500
I		Clock Jitter	500
I		The combined impact of Skew and Jitter	501 – 502
I	10.3.2	Sources of Skew and Jitter	
I	10.3.3	Clock Distribution Techniques	
O	10.3.4	Latch-Based Clocking	516 – 518
O	10.4-10.7	Self-Timed Circuit Design – Future Directions	519 – 551
P	*7.5 – 7.5.1 (!)*	Pipelining	358-361

Material from Chapter 10, one section from Chapter 7

Outline

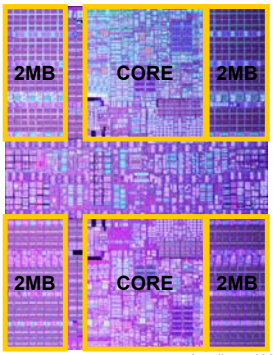
- Timing Design Background and Motivation
  - Delay variations, impact
  - Sequential circuits, synchronous design
  - Pipelining, metrics reminder
- The Clock Skew Problem
- Controlling Clock Skew
- Case Study

Get basic appreciation of some system level design issues

Design of LARGE Integrated Circuits

- Correct signal
  - Logic value
  - Right level (restoring logic, …)
- At right place
  - Interconnect (R, C, L)
  - Busses
  - Off-chip drivers, and receivers
- At right time
  - How to cope with (uncertain) delay

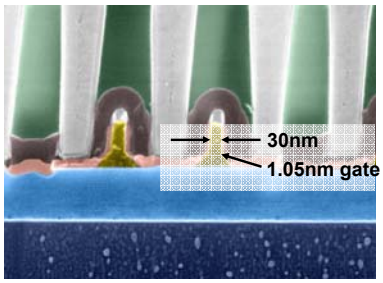
Case Study: IBM Power6 CPU



- introduced 21 may 2007
- 64 bit, dual core
- 790 million transistors
- 4.7 (5*) GHz
- 65nm SOI, 10 Cu levels interconnect
- 2 Cores
- 8 MB on-chip level2 cache
- processor bandwidth: 300GB/sec
- 1953 signal I/O, 5449 power I/O

http://www-03.ibm.com/press/us/en/pressrelease/21580.wss

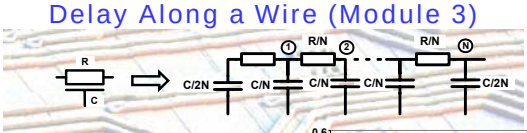
IBM 65nm SOI Technology



Uncertain Delay

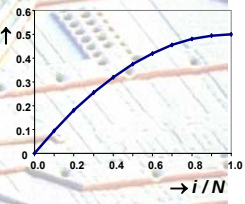
- Data-dependent Delay
- Short and long combinational paths
- Device parameters variations (§3.4)
  - Batch to batch — V_t threshold voltage
  - Wafer to wafer — k' transconductance
  - Die to die — W, L dimensions
- Supply Variations
  - IR drop, dI/dt drop, ringing,
- Interconnect Delay
  - Don't know length of line during logic design
  - Delay at begin of line smaller than at end
  - Interconnect parameter variability

Delay Along a Wire (Module 3)



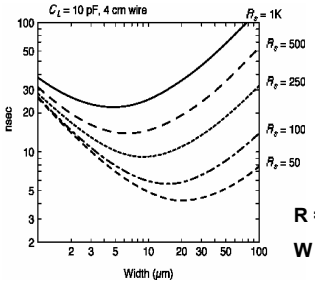
- Signal on RC line exhibits finite propagation speed
- Delay at beginning of line smaller than at end
- Follows from solving diffusion equation
- Elmore delay model also predicts propagation behavior (only approximately)

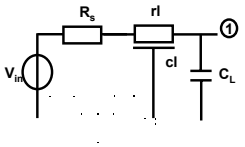
$$T_{Di} = \sum_{k=1}^{N} R_{ik} C_k$$



- Exercise: draw this graph for N = 3, N = 6, or use integration to solve limit for N → ∞

Delay of Clock Wire





R = 0.07 Ω/□, C = 0.04 fF/μm²

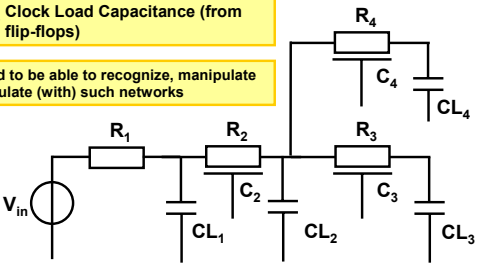
W = Width, r = R/W, c = C*W

5ns compares with 200 MHz

Canonical Clock Tree Network

R_1	Clock Driver Output Resistance
R_2-R_4	Clock Line Segment Resistance
C_2-C_4	Clock Line Segment Capacitance
CL_1-CL_4	Clock Load Capacitance (from flip-flops)

You need to be able to recognize, manipulate and calculate (with) such networks



§ 4.4.3

Impact of Uncertain Delay

- Combinational circuits will eventually settle at correct output values when inputs are stable
- Sequential circuits
  - Have state
  - Must guarantee storing of correct signals at correct time
  - Require ordered computations

Sequential Circuits

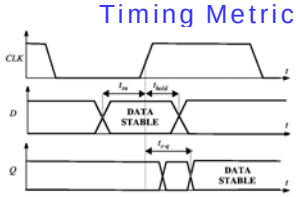
- Sequential circuits require ordered computation
- Several ways for imposing ordering
  - ✓ Synchronous (clock)
  - ✗ Asynchronous (unstructured)
  - ✗ Self-timed (negotiation)

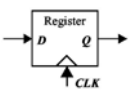
- Clock works like an orchestra conductor

Synchronous Design

- Global Clock Signal
- Synchronicity may be defeated by
  - Delay uncertainty in clock signal
  - Relative timing errors: clock skew
  - Slow logic paths
  - Fast logic paths

Timing Metrics Reminder





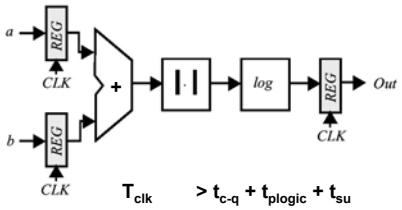
§ 7.1.1

§10.3.1

$t_{c\text{-}q}$: delay from clock (edge) to Q
t_{su} : setup time
t_{hold} : hold time
t_{plogic} : worst case propagation delay of logic
t_{cd} : best case propagation delay (contamination delay)
T : clock period

$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$
$t_{cdregister} + t_{cdlogic} \geq t_{hold}$

Sequential Circuit Timing.

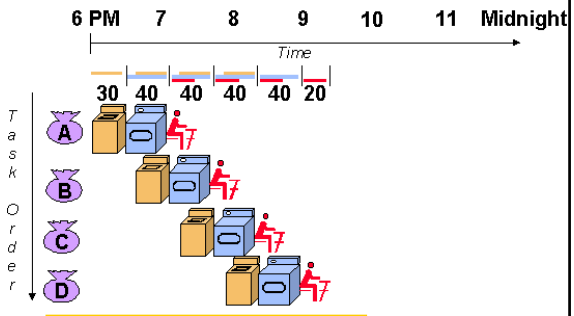


$T_{clk} > t_{c\text{-}q} + t_{plogic} + t_{su}$

$t_{plogic} = t_{p,add} + t_{p,abs} + t_{p,log}$

How to reduce T_{clk}?

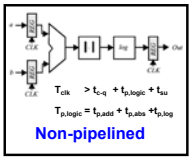
Pipelined Laundry System

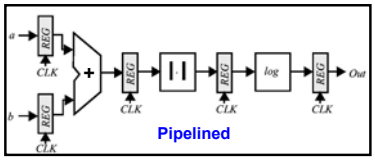


Also: http://en.wikipedia.org/wiki/Pipelining

From http://cse.stanford.edu/class/sophomore-college/projects-00/risc/pipelining/index.html
which credited http://www.ece.arizona.edu/~ece462/Lec03-pipe/

Pipelining





Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

$T_{clk} > t_{c\text{-}q} + \max(t_{p,add}, t_{p,abs}, t_{p,log}) + t_{su}$

- Improve resource utilization
- Increase functional throughput

Pipelining Observations

- Very popular/effective measure to increase functional throughput and resource utilization
- At the cost of increased *latency*
- All high performance microprocessors excessively use pipelining in instruction fetch-decode-execute sequence
- Pipelining efficiency may fall dramatically because of branches in program flow
  - Requires emptying of pipeline and restarting
  - Partially remedied by advanced branch prediction techniques
- But all is dictated by GHz marketing drive
  - All a customer asks is: "How many GHz?"
  - Or says: "Mine is … GHz!"

Bottom line: more flip-flops, greater timing design problems

The Clock Skew Problem

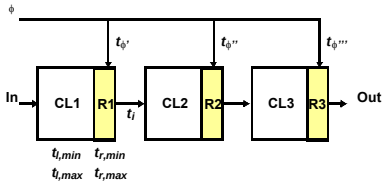
- In Single Phase Edge Triggered Clocking
- In Two Phase Master-Slave Clocking

§10.3.1

(Also: Katz § 6.2.2)

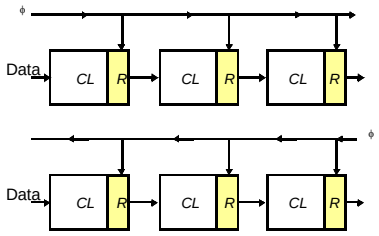
The Clock Skew Problem

Clock Rates >> 1 Ghz in CMOS

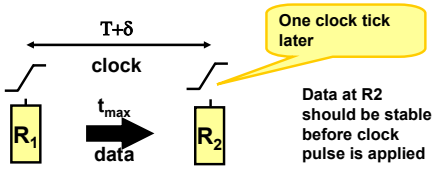


- Clock Edge Timing Depends upon Position
  - Because clock network forms distributed RC line with lumped load capacitances at multiple sites (see earlier slide)
- (Relative) Clock Skew $\delta = t_{\phi''} - t_{\phi'}$
- Clock skew can take significant portion of T_{clk}

Positive and Negative Skew



Edge-Triggered Slow Path Skew Constraint



Timing constraint (t_i = interconnect delay)

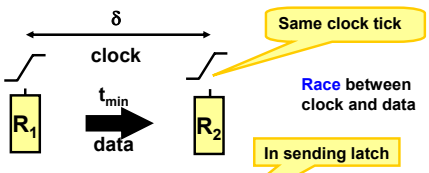
$T + \delta \geq t_{max} = t_{p,logic} + t_i + t_{c\text{-}q,max} + t_{su}$

Internal delay of flip-flop

$T \geq t_{max} - \delta$

- **Minimum Clock Period** Determined by Maximum Delay between Latches minus skew

Edge-Triggered Fast Path Skew Constraint



Timing constraint

$\delta \leq t_{min} = t_{cd,logic} + t_i + t_{c\text{-}q,min} - t_{hold}$

- **Maximum Clock Skew** Determined by Minimum Delay between Latches

Clock Constraints in Edge-Triggered Logic

$T \geq t_{max} - \delta$ | $\delta \leq t_{min}$

- **Observe:**
  - Minimum Clock Period Determined by Maximum Delay between Registers minus clock skew
  - Maximum Clock Skew Determined by Minimum Delay between Registers
- **Conclude:**
  - Positive skew must be bounded
  - Negative skew reduces maximum performance

Controlling Clock Skew

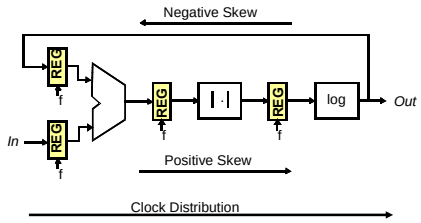
Case Study

§10.3.3

Countering Clock Skew Problems

- Routing the clock in opposite direction of data (negative skew)
  - Hampers performance
  - Dataflow not always uni-directional
  - Maybe at sub circuit (e.g. datapath) level
  - Other approaches needed at global chip-level
  - Useful skew (or beneficial skew) is serious concept
- Enlarging non-overlap periods of clock [only with two-phase clocking]
  - Hampers performance
  - Can theoretically always be made to work
  - Delay in clock network may require impractical/excessively large scheduled $T_{\phi 12}$ to guarantee minimum $T_{\phi 12}$ everywhere across chip
  - Is becoming less popular for large high performance chips

Dataflow not unidirectional



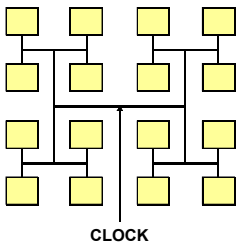
- Data and Clock Routing
- Cannot unambiguously route clock in opposite direction of data
- Need bounded skew

Need bounded Skew

- Bounded skew most practical measure to guarantee functional correctness without reducing performance

- Clock Network Design
  - Interconnect material
  - Shape of clock-distribution network
  - Clock driver, buffers
  - Clock-line load
  - Clock signal rise and fall times
  - …

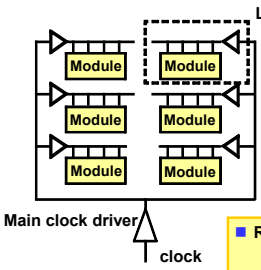
H-tree Clock Network



- All blocks equidistant from clock source ⇒ zero (relative) skew
- Sub blocks should be small enough to ignore intra-block skew
- In practice perfect H-tree shape not realizable

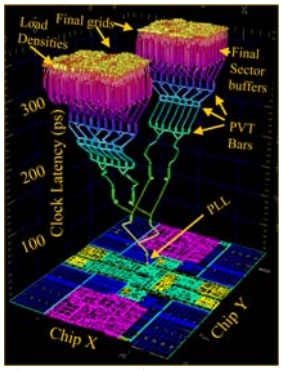
Observe: Only Relative Skew Is Important

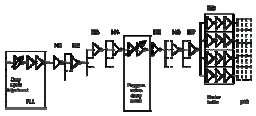
Clock Network with Distributed Buffering



- Reduces absolute delay
  - Makes Power-Down easier
  - Easier of-chip communication
- Sensitive to variations in Buffer Delay

Power6 Clock Distribution

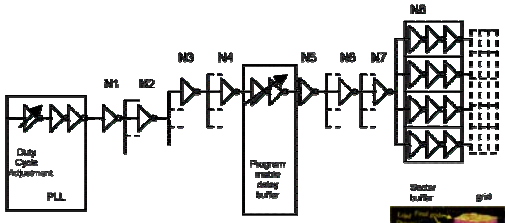


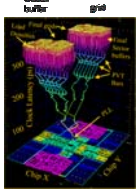


- Latency ~ cycle time

friedrich, isscc 2007

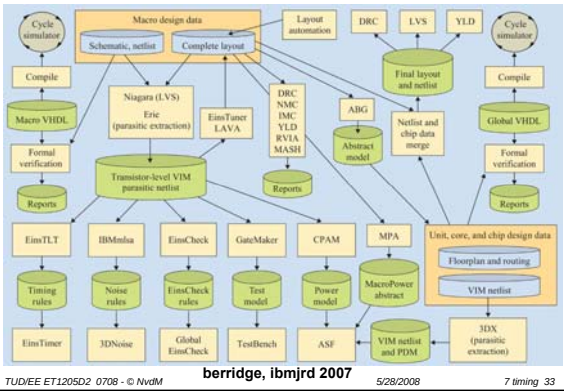
Power6 Clock Distribution





stolt, jssc 2008

IBM Power6 Physical Design Flow



berridge, ibmjrd 2007

Timing Design

- Clocking Scheme is important design decision
- Influences
  - Power
  - Robustness
  - Ease of design, design time
  - Performance
  - Area, shape of floor plan
- Needs to be planned early in design phase
- But is becoming design bottle neck nevertheless
  - Clock frequencies increase
  - Die sizes increase
  - Clock skew significant fraction of T_{clk}
- Alternatives
  - Asynchronous *or* self-timed

Not in this course 

Summary

- Timing Design Background and Motivation
  - Delay variations, impact
  - Sequential circuits, synchronous design
  - Pipelining, metrics reminder
- The Clock Skew Problem
- Controlling Clock Skew
- Case Study

Got basic appreciation of some system level design issues?

MODULE 8

MODULARITY

Course Material for Modularity

Chapter 11 P = primair, I = Illustratie, O = overslaan

P	11.1	Introduction	560
P	11.2	Datapaths in Digital Processor Architectures	560-561
P	11.3	The Adder	561
P	11.3.1	The Binary Adder: Definitions	561-564
P	11.3.2	The Full Adder: Circuit Design Consideration	564-578
I	11.3.2	Manchester Carry Chain Adder	568-570
O	11.3.3	The Binary Adder: Logic Design Considerations	571-586
P	11.4	The Multiplier	586
P	11.4.1	The Multiplier: Definitions	586-587
P	11.4.2	Partial-Product Generation	587-589
P	11.4.3	Partial-Product Accumulation	589-592
O		The Tree Multiplier	592-593
I	11.4.4	Final Addition	593-594
P	11.5	The Shifter	595
P	11.5.1	Barrel Shifter	595-596
P	11.5.2	Logarithmic Shifter	596
O	11.6	Other Arithmetic Operators	596-600
O	11.7	Power and speed trade-offs	600-618
P	11.8	Perspective: Design as a Trade-off	618-619
P	11.9	Summary	619-620

Outline

- Background on Modular Design
  - Hierarchy, reuse, regularity
  - Architecture, bit-slicing
- Adder Design
- Multiplier Design
- Shifter Design
- Layout Strategies (regularity)
- Design as a Trade-Off

contains a lot of reminders

Get further appreciation of some system level design issues

Adder Design

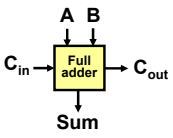
- Adders are fundamental building blocks
  - Digital filtering (DSP): MP3 en/decoder, GSM, GPS, …
  - Data processing
  - Multiplication
  - Address arithmetic
  - …
- Good performance is key
- Many architectures
  - √ Static adder
  - × Dynamic adder (Manchester Carry Chain)
  - × Pipelined Adder
  - × Carry-Bypass, Carry Lookahead, Carry Select
  - × …
- Design trade-offs, optimization
  - √ Architecture level
  - √ Logic level
  - √ Circuit level
  - √ Layout level

Most effective

Least effective

Also see Digital Systems – Katz § 5.5

Full-Adder



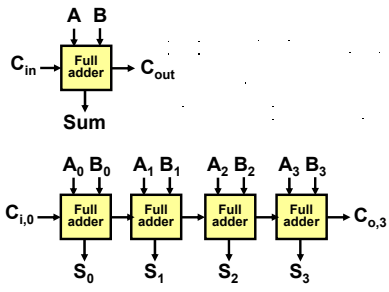
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Add three one-bit numbers

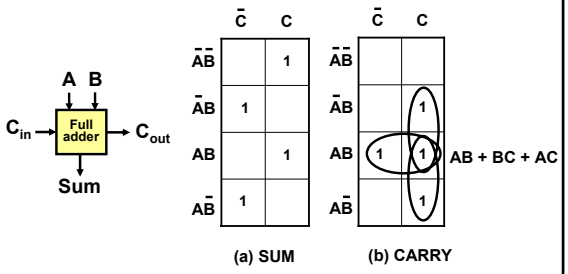
Equivalently: count # 1's in A, B, C_i

Output as 2-bit number <C_oS>

The Ripple-Carry Adder



The Binary Adder



$S = A \oplus B \oplus C_i$
$= \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i + A\bar{B}\bar{C}_i + ABC_i$

$C_0 = AB + BC_i + AC_i$

AND-OR expressions for sum and carry

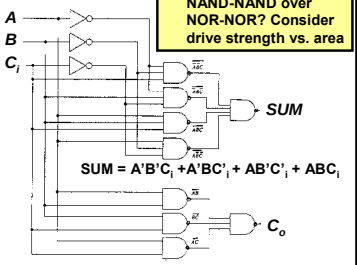
Naïve Complementary CMOS Implementation

- Use DeMorgan to convert AND-OR expressions for *SUM* and *CARRY* to NAND-NAND
- $PQ + RS = \overline{\overline{PQ}\,\overline{RS}}$ (example)

Q: What is advantage of NAND-NAND over NOR-NOR? Consider drive strength vs. area

Transistor Count

3 × INVERT
3 × NAND-2
5 × NAND-3
1 × NAND-4



SUM = $A'B'C_i + A'BC'_i + AB'C'_i + ABC_i$

Can do better using more clever boolean factoring, but…

Full-Adder Boolean Factoring

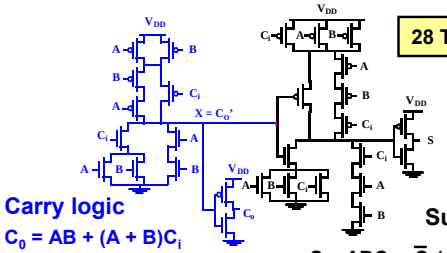
$S = A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$
$= ABC_i + \bar{C}_0(A + B + C_i)$

$C_0 = AB + BC_i + AC_i$
$= AB + (A + B)C_i$

A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Improved Complementary Static Full Adder

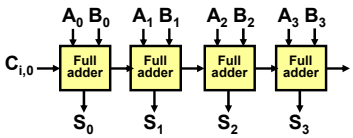
28 Transistors



Carry logic
$C_0 = AB + (A + B)C_i$

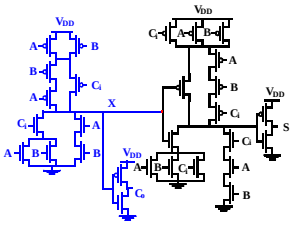
Sum logic
$S = ABC_i + \bar{C}_0(A + B + C_i)$

Ripple-Carry Adder Delay



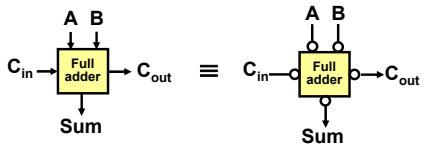
- Worst case delay through full carry path (ripple carry)
- Linear with the number of bits (N)
- $T_{adder} = (N-1)\,T_{carry} + \text{Max}\,(T_{carry}, T_{sum})$
- $T_{adder} = O(N)$ "T_{adder} is of Order N" *means linear with N*
- **Goal: Make the fastest possible carry path circuit**

Adder Evaluation



Carry Chain:
- Long PMOS chains
- High C at X
- 2 (inverting) stages

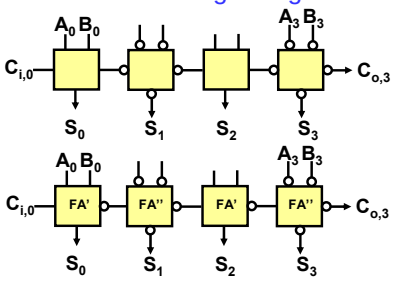
Inversion Property



$$\overline{S}(A,B,C_i) = S(\overline{A},\overline{B},\overline{C_i})$$

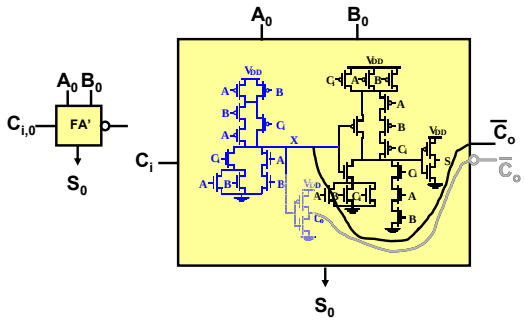
$$\overline{C_0}(A,B,C_i) = C_0(\overline{A},\overline{B},\overline{C_i})$$

Minimize Critical Path by Reducing Inverting Stages



- Can eliminate inverter in carry from each FA
- Need 2 different types of cells, but both with inverting carry – will require only one stage per bit

Eliminate Inverter In Carry



Multiplier Design

- Multipliers are fundamental building blocks too
  - Digital filtering (DSP): MP3 en/decoder, GSM, GPS, …
  - Data processing
  - Address arithmetic
  - …
- Good performance is key, often they are the performance bottleneck
- Multipliers are complex arrays of adders
- Many architectures
  - ✓ Basic Array Multiplier
  - ✗ Bit-serial
  - ✗ Booth-encoding multiplier
  - ✗ Baugh-Wooley multiplier
  - ✗ Wallace tree multiplier
  - ✗ …
- Design trade-offs, optimization
  - ✓ Architecture level, Logic level, Circuit level, Layout level

The Binary Multiplication

$$X = \sum_{i=0}^{M-1} X_i 2^i \quad Y = \sum_{j=0}^{N-1} Y_j 2^j$$

$$Z = X \times Y = \sum_{k=0}^{M+N-1} Z_k 2^k$$

$$= \left(\sum_{i=0}^{M-1} X_i 2^i\right)\left(\sum_{j=0}^{N-1} Y_j 2^j\right)$$

$$= \sum_{i=0}^{M-1}\left(\sum_{j=0}^{N-1} X_i Y_j 2^{i+j}\right)$$

ADD AND SHIFT

Example: 42 x 11 = 462

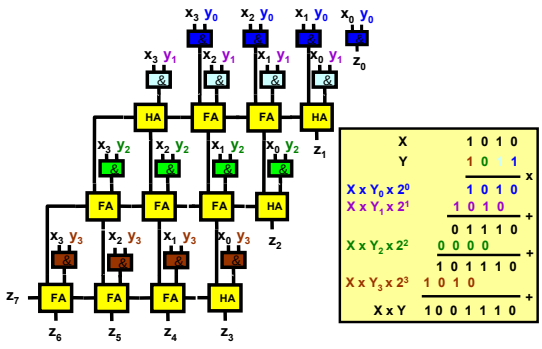
```
  1 0 1 0 1 0
    1 0 1 1 x
  1 0 1 0 1 0
1 0 1 0 1 0
0 0 0 0 0 0
1 0 1 0 1 0 +
1 1 1 0 0 1 1 1 0
```

Each partial product formed by bitwise AND operation

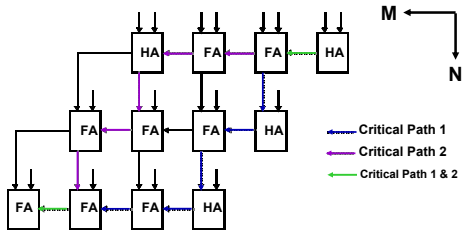
Partial products are shifted before being added

- **Conclusion:** similar to decimal multiplication
- $X_{10} \times Y_{10} = \sum_{i=0}^{M-1}\left(\sum_{j=0}^{N-1} X_i Y_j 10^{i+j}\right)$

The Array Multiplier



The MxN Array Multiplier — Critical Path



- $t_{mult} \approx [(M - 1) + (N - 2)]t_{carry} + (N - 1)t_{sum} + t_{and}$
- Requires comparable carry and sum delays

Adder Cells in Array Multiplier

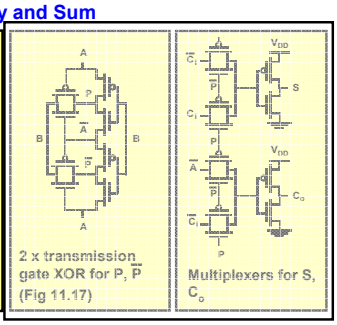
Identical Delays for Carry and Sum

A	B	C_i	S	C_o	Carry status
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

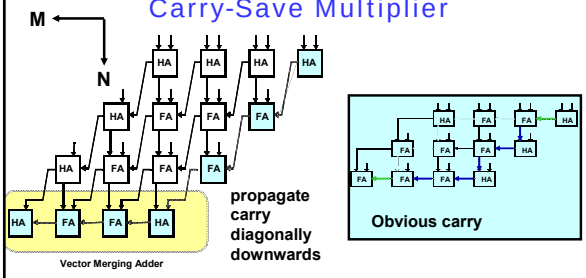
$P = A \oplus B$

If $P = 1$ then $S = \overline{C_i}$, $C_o = C_i$

If $P = 0$ then $S = C_i$, $C_o = A$

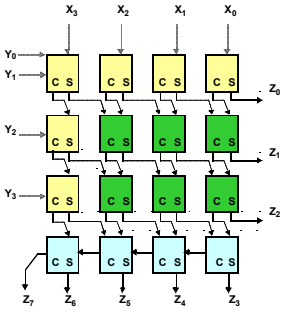


Carry-Save Multiplier



- $t_{mult} \approx (N - 1)t_{carry} + t_{and} + t_{merge}$ (assuming $t_{add} \approx t_{carry}$)
- Use fastest possible adder for final vector merging
- Will be larger, use more power, etc, but need only one row!

Multiplier Floorplan



X signals are routed vertically across each column ("broadcast")

Y signal are broadcasted horizontally across rows

Regularity!

Multipliers — Summary.

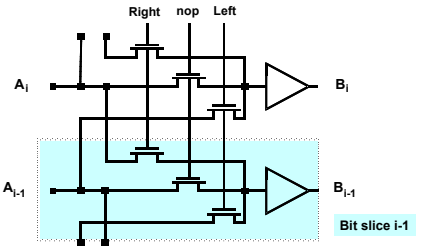
- Optimization Goals Different Vs Binary Adder
- Once Again: Identify Critical Path
- Other possible techniques
  - Logarithmic versus Linear (Wallace Tree Mult)
  - Data encoding (Booth)
  - Pipelining

GLIMPSE AT SYSTEM LEVEL OPTIMIZATION

Shifter Design

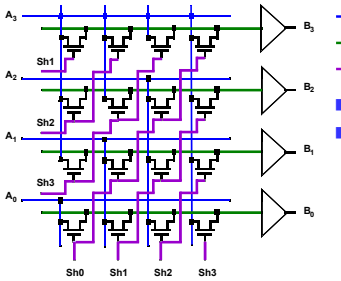
- Shifters are fundamental building blocks too
  - Floating point units
  - Scalers
  - Multiplication by constant numbers (add and shift)
  - …
- Constant shifting is only interconnect
- Programmable shifting requires active circuitry
- Usually dominated by interconnect
- Architectures
  - Barrel Shifter
  - Logarithmic Shifter
  - …
- Design trade-offs, optimization
  - Architecture level, Logic level, Circuit level, Layout level
  - Simpler compared to Adder, Multiplier, hence less rewarding
- Good example of pay-off of structural design

The Binary Shifter



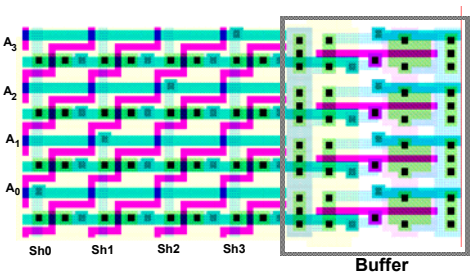
- Multibit shifters by cascading
- M stages for M-bit shift
- Complex and slow for larger M
- More structured approach needed

The Barrel Shifter

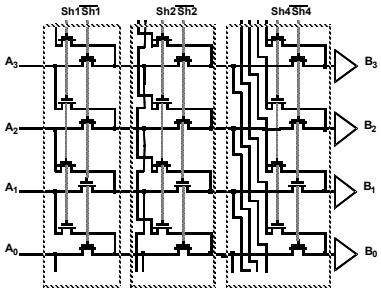


- Shift 1-N positions
- One control bit high
- Need M stages for M-bit shift
- Signal passes only one pass-transistor => delay?
- Area Dominated by Wiring, not (always) by # transistors

4x4 Barrel Shifter

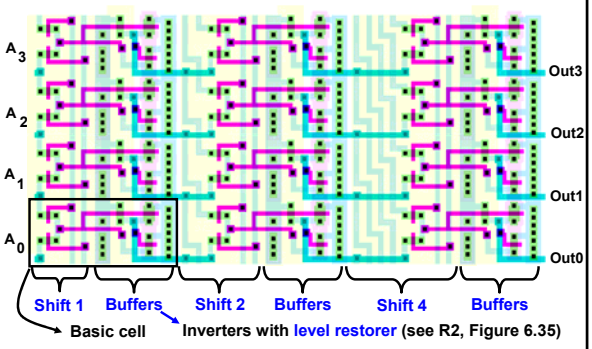


Logarithmic Shifter



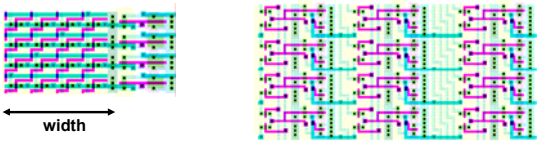
- Section i shifts $2^{(i-1)}$ bits
- Need only $log_2 M$ stages for M-bit shift

0-7 bit Logarithmic Shifter



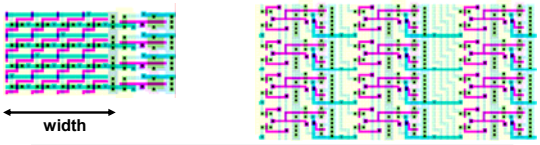
Exercise: decipher layout of basic cell and draw transistor circuit

Size Comparison



- *M* is maximum bit displacement, $K = log_2 M$
- For large *M*, width is dominated by vertical metal wires
- Disregard buffer size, only count vertical wires
- Barrel shifter needs 1 control and 1 data wire per stage
- # Wires: $2M$
- Log shifter needs 2 control + 2^{i-1} data wires for stage *i*
- # Wires: $2K+(1+2+4+\ldots+2^{K-1}) = 2K+2^K-1 = 2\,log_2 M + M - 1$
- Log shifter will have smaller area for larger *M*!

Speed Comparison

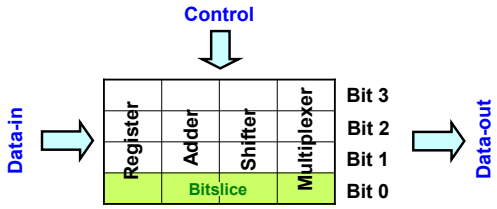


Exercise

- Discuss the relative speeds of both shifters, as a function of *M* (see discussion in book). Consider:
  - Number of sections
  - Input capacitance at the buffers (including diffusion areas of the driving pass-transistors)
  - Number of buffers (necessity of buffers)
  - The number of pass-transistors the signal has to pass
  - …

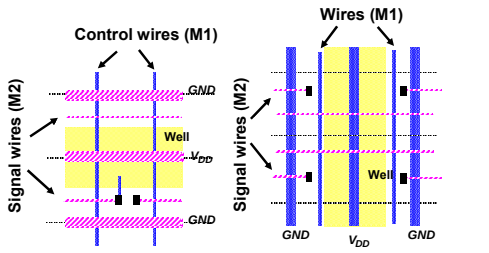
Layout Strategies (regularity)

Bit-Sliced Design



- **Tile** identical processing elements
- Rows for each **bit**
- Columns for each **function**
- **Control** from top (often with ***control-slice***)
- (Example orientation)

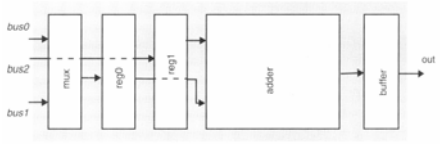
Layout Strategies for Bit-Sliced Datapaths



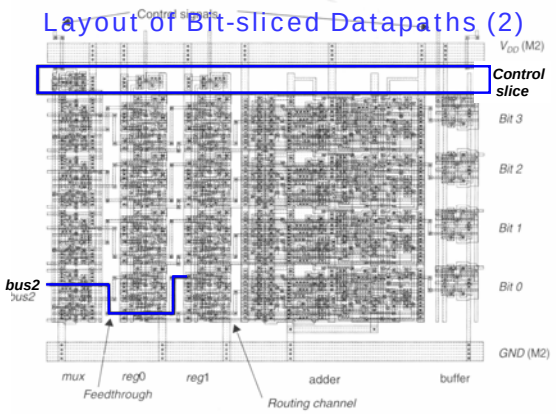
Approach I — Signal and power lines parallel

Approach II — Signal and power lines perpendicular

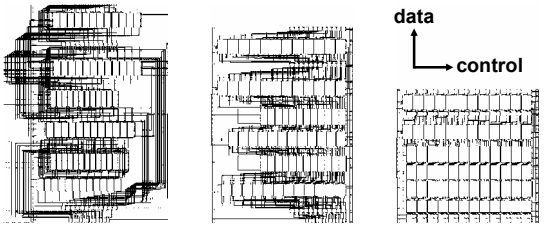
Layout of Bit-sliced Datapaths



Layout of Bit-sliced Datapaths (2)



Layout of Bit-sliced Datapaths (3)



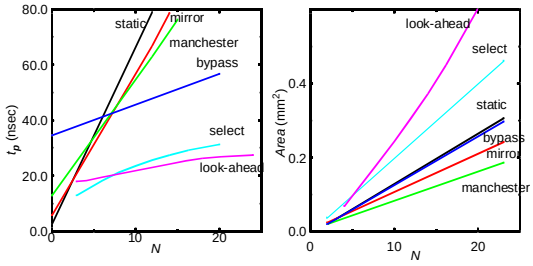
Unoptimized
Area: 4.2mm²

With feedthroughs
Area: 3.2mm²

+ Equalized cell height
Area: 2.2mm²

- Good layout really counts!
- Feedthroughs less (but still) useful with multiple metal layers

Design as a Trade-Off



VLSI Design

- Select right structure
- Determine and optimize critical timing path for speed
- Optimize rest for area (cost) and/or power and/or design time
- Consider layout aspects

Regularity and modularity are a VLSI designer's best friends

Summary

- Background on Modular Design
  - Hierarchy, reuse, regularity
  - Architecture, bit-slicing
- Adder Design
- Multiplier Design
- Shifter Design
- Layout Strategies (regularity)
- Design as a Trade-Off

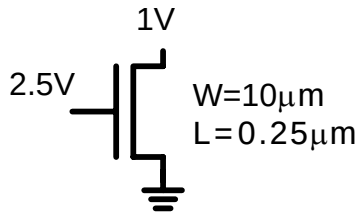
Got further appreciation of some system level design issues?

The End

Oefenopgaven 1 – Devices

Opgave 1.1

Beschouw onderstaande transistor. De technologie is de 0.25μm technologie uit het boek, maar we nemen $\lambda=0$ en $V_{DSAT}=\infty$. (Opm.: De zinsnede '…is de 0.25μm technologie uit het boek' betekent dat alle gegevens, tenzij ze niet expliciet anders gegeven zijn, te vinden zijn op de binnenkanten van de voorflap en achterflap van het boek. Wanneer er geen gegevens vermeld zijn moeten ook de gegevens uit het boek aangenomen worden. Deze uitleg zal meestal niet expliciet vermeld worden,.)



a. Bepaal het werkgebied van de transistor.

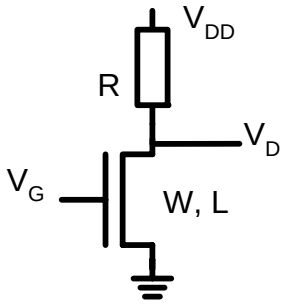
Werkgebied:

b. Bereken de drain stroom I_d. Geef ook de hoofdstappen van de berekening.

I_d =
Berekening:

Opgave 1.2

Beschouw onderstaande schakeling.



a. Neem aan dat de transistor in het lineaire (=triode = resistieve) gebied ingesteld is. Geef de symbolische circuitvergelijking voor de spanning V_D. Weer geldt de technologie uit het boek met $\lambda=0$ en $V_{DSAT}=\infty$. Opm.: met de symbolische circuitvergelijking wordt een vergelijking bedoeld zonder getallen, maar met alleen de parameters.)

b. Neem nu R = 170Ω, $V_{DD} = V_G = 2.5V$, W=10µm, L=0.25µm. Bepaal de spanning V_D, aannemende dat de transistor in het lineaire gebied is ingesteld.

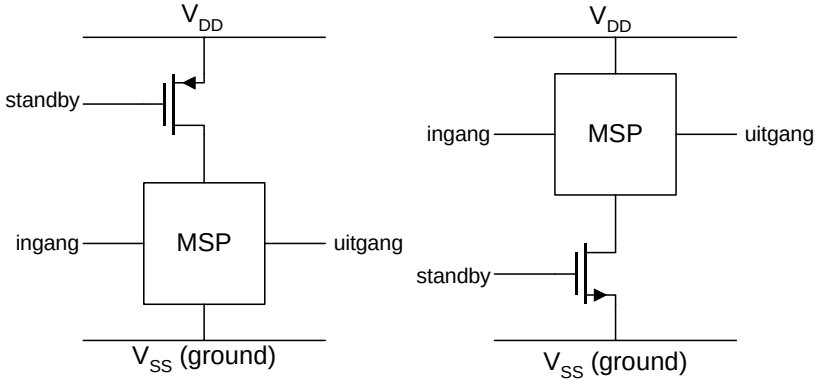
V_D =
Berekening (hoofdstappen):

c. Verifieer dat de transistor bij de uitkomst V_D van het vorige onderdeel inderdaad in het lineaire gebied is ingesteld.

Bewijs:

Opgave 1.3 (tentamen 26 augustus 2004)

Beschouw nu een schakeling die in een accu-gevoed systeem opgenomen wordt, zoals bijvoorbeeld een mobiele telefoon. Ter verlenging van accu levensduur is het van belang om de schakeling in een standby mode te kunnen zetten waarbij er geen (of zo weinig mogelijk) stroom aan de accu ontrokken wordt. Zie onderstaand principe schema. Hier duidt 'MSP' een mixed-signal-processor aan die stroomloos gemaakt moet worden, de functie van dit onderdeel doet er verder niet toe. Dit onderdeel kan stroomloos gemaakt worden door met een transistor te schakelen in de V_{dd} of V_{ss} (aarde=ground) aansluiting van de MSP. Zie onderstaande figuur voor de twee alternatieven.



a) MSP en PMOS standby transistor b) MSP en NMOS standby transistor

De standby transistor, zowel in schakeling a) als b), moet de maximaal benodigde stroom voor de MSP zonder noemenswaardige spanningsval over deze transistor kunnen voeren. De MSP, inclusief de standby transistoren, wordt gemaakt in de 0,25 µm technologie uit de 2e editie van Rabaey. Ga uit van de transistorparameters van de binnenkant achterflap (of bijlage). De voedingsspanning is 2,5V.

Beschouw nu schakeling a) (met de PMOS transistor).

Gevraagd:

a. In welk werkgebied staat de transistor als standby = 0 (oftewel, de gate van de PMOS is laag) en $|V_{ds}| < 0.1V$?

Werkgebied:
Verklaring:

b. Bepaal de minimale breedte van de PMOS transistor (bij L=0.25 µm), zodanig dat $|V_{ds}| < 0.1$ V bij $|I_{ds}| = 10$ mA.

W_{min} =
Berekening:

c. Waarom moet je bovenstaande berekening doen m.b.v. de stroomformule(s) van de transistor en kun je niet werken met R_{eq}?

Verklaring:

d. Waarom is het van belang om de standby transistor (en in het algemeen de hele schakeling) zo klein mogelijk te maken?

Verklaring

Moderne IC fabricage processen bieden soms een keuze voor de drempelspanning van de transistoren. Neem nu aan dat er de volgende mogelijkheden zijn, genaamd 'Standaard' en 'low-Vt'.

	NMOS		***PMOS***	
Standaard	NMOS1	$V_{t0} = 0.43V$	PMOS1	$V_{t0} = -0.4V$
low-V_t	NMOS2	$V_{t0} = 0.3V$	PMOS2	$V_{t0} = -0.3V$

Verder zijn alle transistorparameters gelijk aan de standaardparameters voor NMOS en PMOS uit de 2e editie van Rabaey, de low-V_t transistoren verschillen alleen wat betreft de drempelspanning van hun 'standaard' tegenhangers.

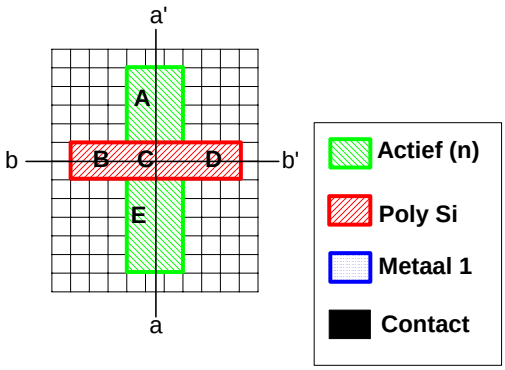
e. Gevraagd: Met welk type transistor kan de standby-transistor het kleinste worden?

❑ NMOS1 (standaard)	❑ NMOS2 (low V_t)	❑ PMOS1 (standaard)	❑ PMOS2 (low V_t)
Verklaring:			

Oefenopgaven 2 – Process

Opgave 2.1

Beschouw nevenstaande layout van een transistor met layer map.



a. Geef voor ieder van de aansluitingen gate, source, drain aan uit welke letters A-E (zie de layout) het gebied bestaat.

G:	S:	D:

b. Teken een doorsnede langs a-a' en b-b'

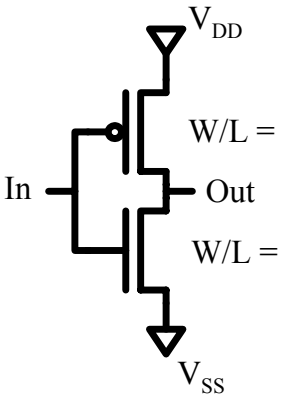
Doorsnede a-a':	Doorsnede b-b':

Opgave 2.2

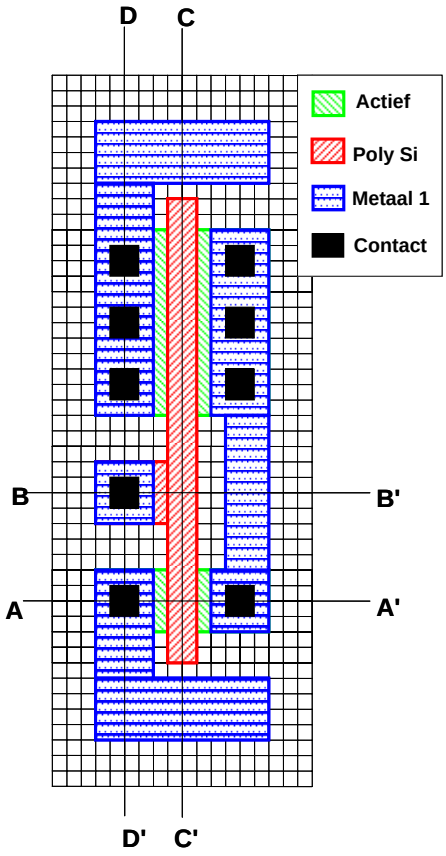
Beschouw nevenstaande layout van een invertor.

a. Teken hieronder de doorsnedes langs A-A', B-B' en C-C'

b. Geef in het equivalente transistorschema hieronder aan wat de W/L verhoudingen van de transistoren zijn. (De bovenste transistor in de layout is de p-transistor, en de onderste in de layout is de n-transistor.)



c. Geef in de layout hiernaast aan waar zich de aansluitingen (uit het schema hierboven) In, Out, V_{DD} en V_{SS} bevinden.



Doorsnede A-A':	Doorsnede B-B':
Doorsnede C-C':	

Oefenopgaven 3 – Interconnect

Opgave 3.1

Een draad is gemaakt van een materiaal met een specifieke weerstand ρ = 4 μΩcm. De draad heeft een dikte (*t*) van1200 Å (1 Angstrom (Å) is 10^{-10} m). De draad heeft een breedte (*w*) van 0.6 μm.

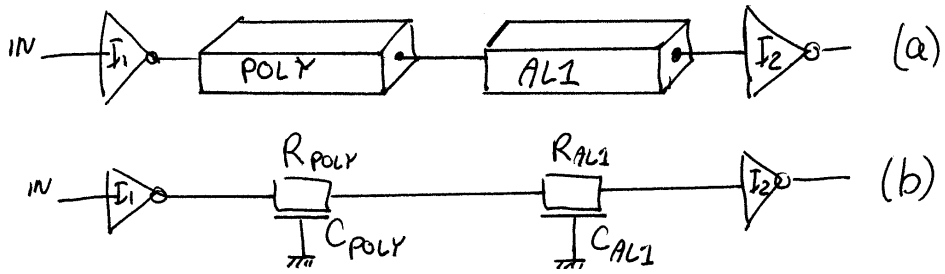
a. Geef de formule voor het berekenen van de sheet weerstand, zonder het invullen van de parameters. Geef daarna het antwoord, zonder berekening. Vergeet niet de eenheid.

Formule: $R_{\square}$ =
Antwoord: $R_{\square}$ =

b.Bereken de weerstand van een draad met een lengte (*l*) van 125 μm. Eerst formule zonder numerieke waarden, en daarna antwoord zonder berekening. Vergeet niet de eenheid.

Formule: R =
Antwoord: R =

Opgave 3.2 (10 juni 2003)



a. Beschouw een deelsysteem op een chip zoals met (a) aangeduid in de bovenstaande figuur. De lengte en breedte van het poly-segment bedragen respectievelijk 100 μm en 1μm, en van het Al_1-segment respectievelijk 1000 μm en 1μm. Deze segmenten lopen op de chip direct boven het substraat (field). Neem voor Poly $R\square = 5\Omega$ en voor Al_1 $R\square = 0.1\Omega$, en voor C de waarden uit de tabellen van Rabaey (binnenkant achterflap of bijlage). Bereken de R en C waarden voor het vervangingsschema wat in de bovenstaande figuur met (b) is aangeduid.

Waarde	**Berekening**
R_{poly} =	
C_{poly} =	
R_{al1} =	
C_{al1} =	

b. Bereken de Elmore delay van In_1 naar de ingang van I_2, als I_1 een uitgangsweerstand van 1kΩ en I_2 een ingangscapaciteit van 25fF heeft.

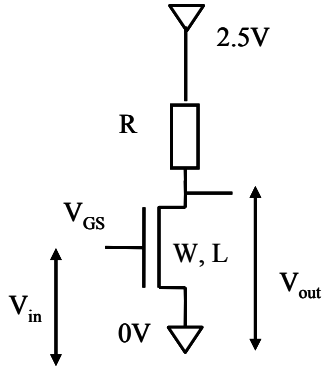
T_{ed} =

Berekening:

Oefenopgaven 4 – Inverter

Opgave 4.1

Beschouw nevenstaande schakeling, een zogenaamde pseudo-NMOS inverter. De transistorgegevens zijn die uit het boek, maar met $\lambda = 0$ (we verwaarlozen kanaallengtemodulatie).



a. Geef hieronder de symbolische formule voor het berekenen van de W/L verhouding voor de schakelspanning V_m wanneer deze in de buurt van de 1.25 Volt dient te liggen.

W/L =

b. Wanneer V_m in de buurt van de 0.6V zou liggen, verandert dan je antwoord op onderdeel **a**?

Het antwoord verandert wel/niet, omdat

c. Stel dat in bovenstaande schakeling R = 10kΩ, W=5µm en L=0.25µm. Bereken dan de T_{pHL} en de T_{pLH}. Je hoeft voor de transistor niet met de stroomformule te rekenen, maar je kunt de equivalente aan-weerstand gebruiken. De belastingcapaciteit is Cload = 1fF. Geef eerst de formules, dan het antwoord.

(formule) T_{pHL} =
(antwoord) T_{pHL} =
(formule) T_{pLH} =
(antwoord) T_{pLH} =

d. Wanneer met behulp van bovenstaande schakeling een ringoscillator gemaakt wordt met 5 trappen, wat is dan de oscillatiefrequentie? Druk je antwoord uit in de symbolische waarden T_{pHL} en de T_{pLH},

f =

e. We nemen weer R = 10kΩ en kiezen W/L zo dat V_{OL} = 0.5V. Wanneer de ingang 70% van de tijd een logische 1 en 30% van de tijd een logische 0 is, wat is dan de (gemiddelde) statische powerdissipatie?

P_{stat} =
Berekening:

f. Waneer de schakelfrequentie 100 MHz is, wat is dan de dynamische powerdissipatie? Weer geldt R = 10kΩ en V_{OL} = 0.5V. Verder nemen C_{load} = 1fF.

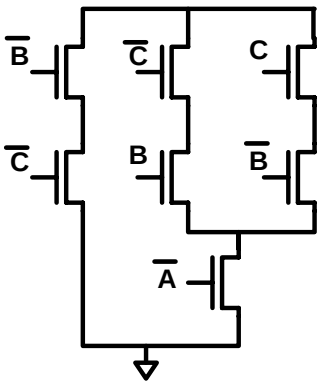
P_{dyn} =
Berekening:

Oefenopgaven 5 – Combinational

Opgave 5.1 (22 juni 2001)

Gegeven is een zogenaamde "democratische schakeling" waarvan de waarheidstabel hiernaast rechts gegeven is. De uitgang is één wanneer de meerderheid van de ingangen één is.

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



a. Het transistorschema van het pull-down netwerk van een complementaire CMOS uitvoering van deze democratische schakeling is hierboven helemaal rechts gegeven. Teken hieronder het bijbehorende pull-up netwerk. Geef bij iedere transistor-gate duidelijk de ingang aan.

b. Dimensioneer de transistoren (geef de W/L verhouding) van het pull-down netwerk, zodanig dat de worst-case effectieve R_{on} overeenkomt met de R_{on} van een inverter met 2 x minimum drive sterkte. Geef uw antwoorden weer in het schema van het pull-down netwerk.

c. (Extra t.o.v. tentamen 22/6) Omcircel de transistoren in het schema van het pull-down netwerk welke last kunnen hebben van het body effect.

d. (Extra t.o.v. tentamen 22/6). Neem aan (niet het antwoord op vraag **b**) dat de W/L verhouding van alle transistoren in het pull-down netwerk gelijk is aan 4. De transistoren zijn gekarakteriseerd door de gegevens uit het boek van Rabaey. Wat zijn dan de effectieve pull-down weerstanden voor de minimale en maximale pull-down vertraging? Geef ook een voorbeeld van een ingangscombinatie (*vector*) voor deze twee situaties.

R_{min} =	R_{max} =
(ABC) =	(ABC) =

Opgave 5.2 (28 augustus 2002)

Beschouw een complementary static CMOS gate voor de formule r = (a'c' + b'c' + abc)'

a. Teken het transistor schema van het pull-down netwerk van een and-or-invert gate wat bovenstaande formule voor *r* realiseert. Neem aan dat ook de inverse signalen a', b' en c' beschikbaar zijn. Een oplossing met 6 transistoren kan 4 punten opleveren, een oplossing met 7 transistoren maximaal 3 punten.

Schema:

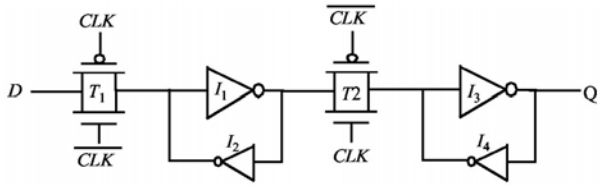
b. Dimensioneer het pull-down netwerk zodanig dat de equivalente sterkte (*drive-strength*) gelijk is aan die van een invertor met minimale afmetingen. Geef W en L bij (naast) iedere transistor in bovenstaand schema, en geef hieronder de berekeningen.

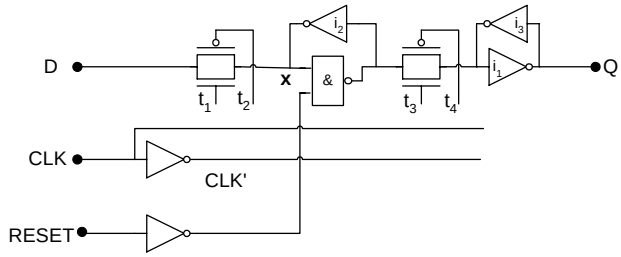
Berekeningen:

Oefenopgaven 6 – Sequential

Opgave 6.1 (28 augustus 2002)

Beschouw de realisatie van een flip-flop. Een variant zoals in het boek gegeven is de zogenaamde 'Ratioed Reduced Clock Load Register' zoals ook hieronder weergegeven, zodanig dat de uitgang verandert op de neergaande klok flank. Een variant is rechts weergegeven.





a. Van deze variant schakeling ontbreken de verbindingen van $t_1 – t_4$ met CLK en CLK'. Voeg deze toe (teken ze erbij in bovenstaande figuur), zodanig dat de uitgang Q verandert op de neergaande klokflank.

b. Wat is de functie van de invertoren i_2 en i_3 (in het tweede schema, onze variant van de flip-flop)?

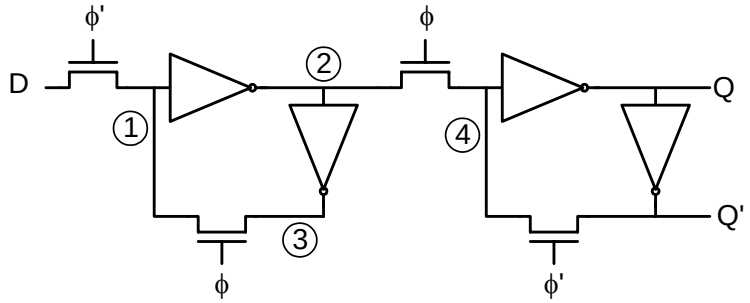
c. Stel dat de *D*-ingang van onze flip-flop gestuurd wordt door een minimum-size inverter, en ook dat de transmissie-gate transistoren de minimum afmetingen hebben. Teken dan hieronder het equivalente transistorschema wat zorgt voor de hoog-naar-laag overgangen op het punt *x*. Geef van de 2 bekende transistoren (die van de sturende invertor en de transmissiegate) de afmetingen van de transistoren in λ. **Tip:** het schema bevat 3 transistoren. Let op het type. Noteer de afmetingen (W en L) naast de transistoren.

d. Bepaal de mimimum afmetingen van de derde transistor zodanig dat het punt *x* beneden VDD/2 getrokken kan worden.

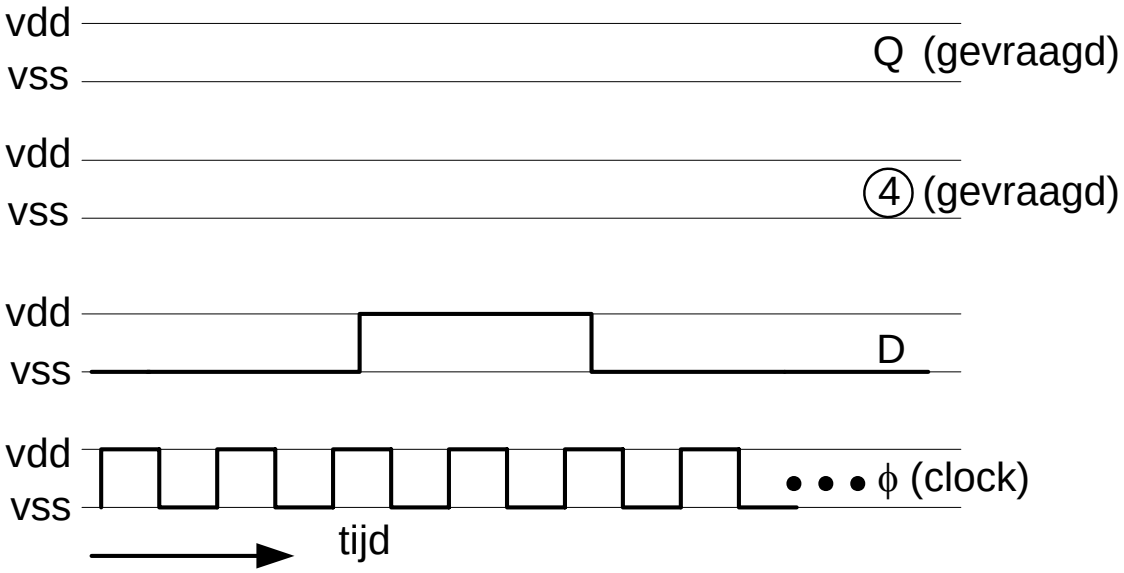
W = λ L = λ
Berekening:

Opgave 6.2 (22 augustus 2005)

Beschouw nu onderstaande implementatie van een master-slave D-flip-flop.



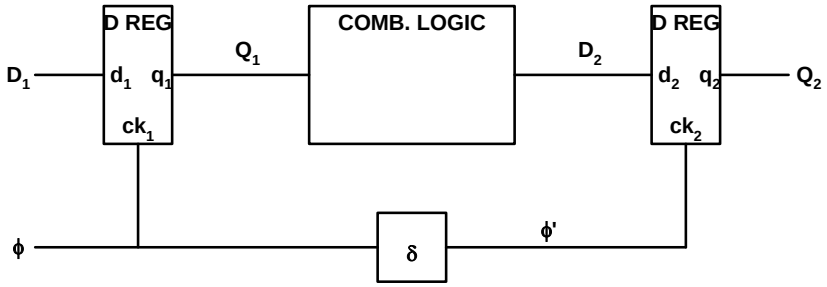
Onderstaand diagram toont het klok signaal en het D-signaal als functie van de tijd. Teken in hetzelfde diagram de signalen op knooppunt 4 en op de Q-uitgang. Beschouw het system als vertragingsloos, maar hou indien van toepassing wel rekening met drempelspanningsverliezen.

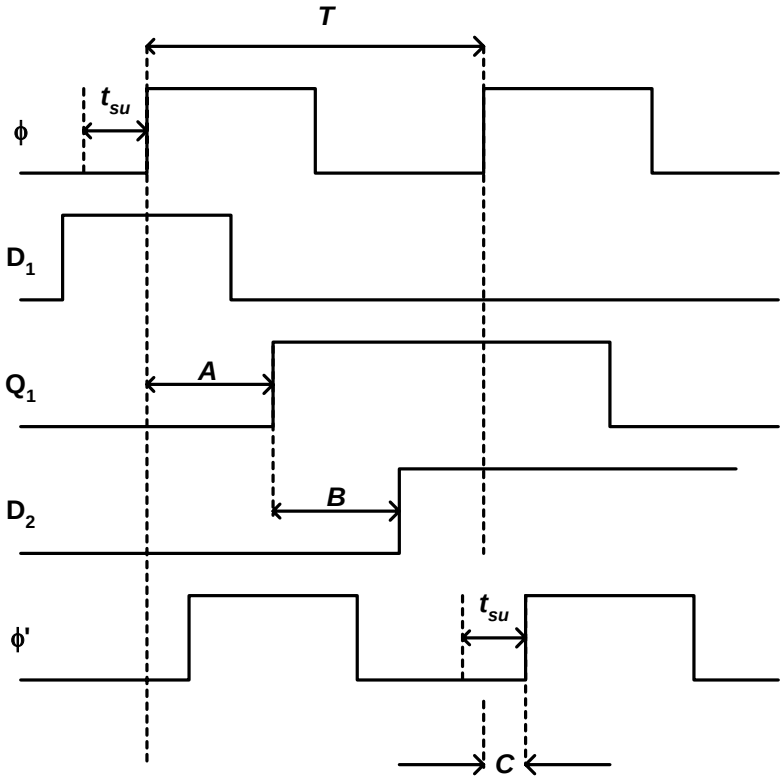


Oefenopgaven 7 – Timing

Opgave 7.1 (16 juni 2004)

Gegeven onderstaande sequentiële schakeling, en bijbehorend timing diagram. In dit timing diagram is t_{su} de setup-time van de registers en T de klok periode.





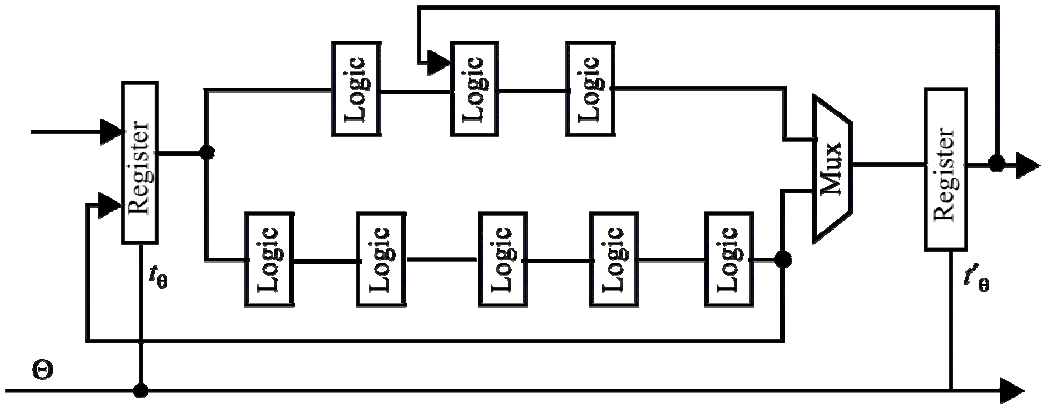
a. De registers hebben een clock-naar-Q delay gegeven door t_{cq}, de logica heeft een propagatietijd t_{logic}, en de clock-skew wordt aangegeven door δ. Geef in onderstaande tabel aan welke van de tijden aangegeven met A, B en C in bovenstaand diagram overeenkomen met t_{cq}, t_{logic} en δ.

A =	B =	C =

b. Als er tijd over is (als de klok niet op maximaal toelaatbare snelheid loopt), spreekt men van 'slack'. Hiermee wordt, bij een gegeven klok frequentie en eventueel bekende skew, de tijd bedoeld die het data signaal eventueel later bij een register aan mag komen zonder dat de correcte werking van de schakeling verloren gaat. Geef in bovenstaande figuur de slack aan op eenzelfde manier als de andere kritieke tijden zijn aangegeven (met de horizontale pijlen).

Opgave 7.2

Beschouw onderstaande schakeling



Neem een eenheids-delay voor de registers en de logic, dus $T_r = T_l = 1$, en een 2 maal zo grote vertraging voor de multiplexer, $T_m = 2\ T_l = 2$. De registers zijn positive-edge-triggered, en hebben een setup-time, $T_s = 1$.

a. Bepaal de 4 verschillende logische paden die in de schakeling voor de timing zorgen. Teken pijlen in het schema.

b. Bepaal voor ieder van de paden de propagatie-vertraging.

c. Bepaal de minimum klok periode wanneer de klok-skew $\delta = t'_\theta - t_\theta = 0$.

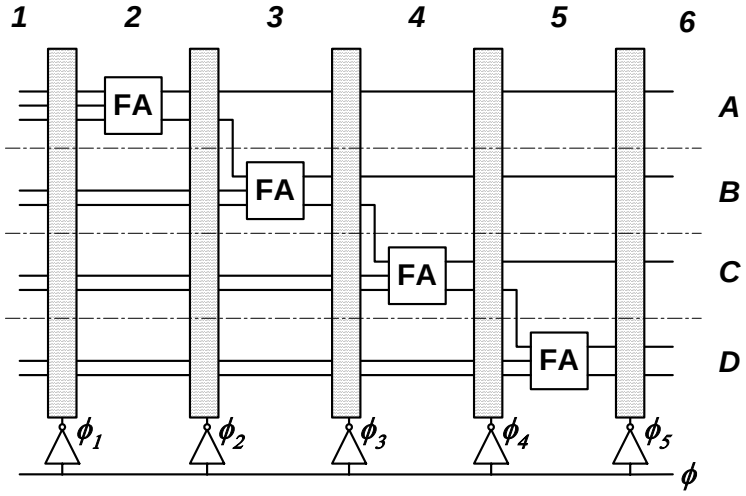
d. Idem, wanneer $\delta = 1$.

e. Idem, wanneer $\delta = 4$.

Oefenopgaven 8 – Modulariteit

Opgave 8.1 (12 juni 2001)

Beschouw onderstaande 4-bit opteller. Deze is onderdeel van een digitale signaalbewerker, en het is belangrijk om de hoogste *throughput* (doorvoersnelheid) te behalen. Daarom is het pijplijn principe doorgevoerd tot op bit-nivo. De verticale balken geven flipflop-kolommen aan (flipflop is latch of register), de stippellijnen en de cijfers en letters buiten de schakeling delen de schakeling in als het kader van een wegenkaart.



a. Geef in bovenstaande figuur aan waar zich de volgende signalen bevinden: A_0-A_3, B_0-B_3 (de ingangssignalen) en S_0-S_4 (de uitgangssignalen).

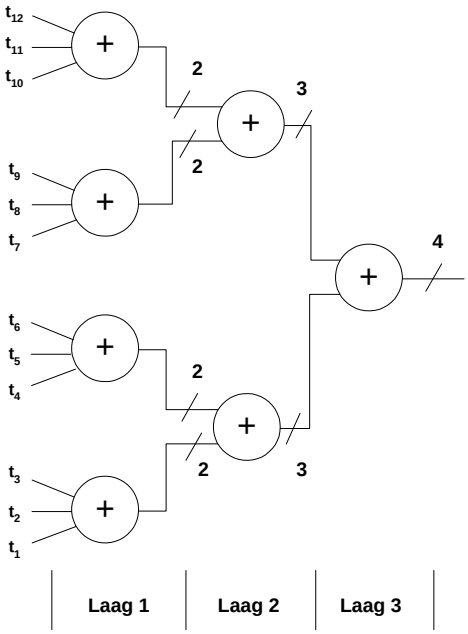
b. Geef (in de figuur) de correcte logische waarde aan het overblijvende signaal.

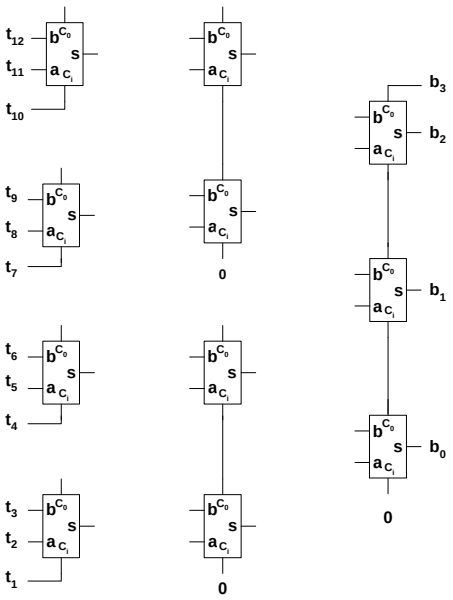
c. Laat T_{carry} de vertraging zijn van de ingangen van de full-adder naar de carry uitgang, en T_{som} hetzelfde voor het som signaal. De maximale kloksnelheid wordt (mede) bepaald door:
   A T_{carry}, maar niet of nauwelijks door T_{som}
   B T_{som}, maar niet of nauwelijks door T_{carry}
   C $T_{carry} + T_{som}$
   D Max (T_{carry}, T_{som})
   E Min (T_{carry}, T_{som})

d. Wanneer het klok-circuit skew geeft, zit de relevante skew tussen
   A ϕ_1 en ϕ_5
   B ϕ_i en ϕ_{i+1}
   Verklaring:

Opgave 8.2

Snelle analoog-digitaal omzetters zetten het analoge signaal in veel gevallen eerst om in een digitaal signaal volgens een zogenaamde ‘thermometer codering’. Dit is een radix 1 code. (Het tellen met je vingers is ook een thermometer code.) Voor het omzetten naar binair (radix 2) kan het aantal enen geteld worden. Het tellen van het aantal enen kan geschieden door ieder bit van de thermometer code te beschouwen als een 1-bit getal, en al die getallen bij elkaar op te tellen. Voor de optellers kun je dan normale full-adder cellen gebruiken, en om een aantal bits bij elkaar op te tellen kun je de optelling onderverdelen in lagen. Iedere laag heeft een aantal optellers, maar dit aantal neemt af bij hogere lagen, terwijl de bitbreedte van iedere opteller toeneemt. In de tekening hieronder links is dit principe weergegeven en zijn de bitbreedtes aangegeven door de schuine streepjes met het cijfer.





a. Geef in de tekening hierboven rechts aan hoe de verschillende Full-Adder cellen met elkaar verbonden moeten worden, m.a.w. maak de schakeling af door de bedrading te tekenen.

b. De schakeling hierboven is, zoals getekend, geschikt voor een 12-bits thermometer code. Hoe kun je de schakeling modificeren, zonder extra componenten (zoals Full-Adders of andere logische poorten) te gebruiken, zodanig dat hij een 15-bits thermometer code kan omzetten naar binair?

Chapter 3
PROBLEMS

For all problems, use the device parameters provided in Chapter 3 (Tables 3.2 and 3.5) and the inside back book cover, unless otherwise mentioned. Also assume T = 300 K by default.

1. [E,SPICE,3.2.2]

a. Consider the circuit of Figure 0.1. Using the simple model, with $V_{Don} = 0.7$ V, solve for I_D.

b. Find I_D and V_D using the ideal diode equation. Use $I_s = 10^{-14}$ A and $T = 300$ K.

c. Solve for V_{D1}, V_{D2}, and I_D using SPICE.

d. Repeat parts *b* and *c* using $I_S = 10^{-16}$ A, $T = 300$K, and $I_S = 10^{-14}$A, $T = 350$ K.

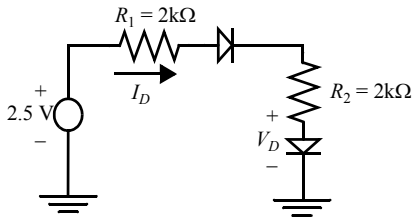


Figure 0.1 Resistor diode circuit.

2. [M, None, 3.2.3] For the circuit in Figure 0.2, $V_s = 3.3$ V. Assume $A_D = 12$ μm^2, $\phi_0 = 0.65$ V, and $m = 0.5$. $N_A = 2.5$ E16 and $N_D = 5$ E15.

a. Find I_D and V_D.

b. Is the diode forward- or reverse-biased?

c. Find the depletion region width, W_j, of the diode.

d. Use the parallel-plate model to find the junction capacitance, C_j.

e. Set V_s = 1.5 V. Again using the parallel-plate model, explain qualitatively why C_j increases.

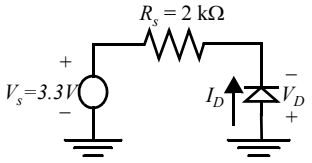


Figure 0.2 Series diode circuit

3. [E, None, 3.3.2] Figure 0.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current I_D for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: $k_n' = 115\mu A/V^2$, $V_{T0} = 0.43$ V, $\lambda = 0.06$ V^{-1}, PMOS: $k_p' = 30$ μA/V^2, $V_{T0} = -0.4$ V, $\lambda = -0.1$ V^{-1}. Assume $(W/L) = 1$.

a. NMOS: $V_{GS} = 2.5$ V, $V_{DS} = 2.5$ V. PMOS: $V_{GS} = -0.5$ V, $V_{DS} = -1.25$ V.

b. NMOS: $V_{GS} = 3.3$ V, $V_{DS} = 2.2$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -1.8$ V.

c. NMOS: $V_{GS} = 0.6$ V, $V_{DS} = 0.1$ V. PMOS: $V_{GS} = -2.5$ V, $V_{DS} = -0.7$ V.

4. [E, SPICE, 3.3.2] Using SPICE plot the *I-V* characteristics for the following devices.

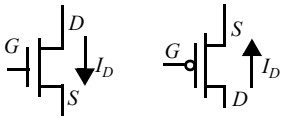


Figure 0.3 NMOS and PMOS devices.

a. NMOS $W = 1.2\mu m$, $L = 0.25\mu m$

b. NMOS $W = 4.8\mu m$, $L = 0.5\mu m$

c. PMOS $W = 1.2\ \mu m$, $L = 0.25\ \mu m$

d. PMOS $W = 4.8\ \mu m$, $L = 0.5\ \mu m$

5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.

a. the regions of operation.

b. the effects of channel length modulation.

c. Which of the devices are in velocity saturation? Explain how this can be observed on the *I-V* plots.

6. [M, None, 3.3.2] Given the data in Table 0.1 for a short channel NMOS transistor with $V_{DSAT} = 0.6\ V$ and $k' = 100\ \mu A/V^2$, calculate V_{T0}, γ, λ, $2|\phi_f|$, and W / L:

Table 0.1 Measured NMOS transistor data

	V_{GS}	V_{DS}	V_{BS}	I_D (μA)
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	–1	1146
5	2	1.8	-2	1039

7. [E, None, 3.3.2] Given Table 0.2 ,the goal is to derive the important device parameters from these data points. As the measured transistor is processed in a deep-submciron technology, the '**unified model**' holds. From the material constants, we also could determine that the saturation voltage V_{DSAT} equals -1V. You may also assume that $-2\Phi_F = -0.6V$.

NOTE: The parameter values on Table 3.3 do NOT hold for this problem.

a. Is the measured transistor a PMOS or an NMOS device? Explain your answer.

b. Determine the value of V_{T0}.

c. Determine γ.

d. Determine λ.

e. Given the obtained answers, determine for each of the measurements the operation region of the transistor (choose from *cutoff, resistive, saturated, and velocity saturated*). Annotate your finding in the right-most column of the above.

Table 0.2 Measurements taken from the MOS device, at different terminal voltages.

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (μA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	
5	-2.5	-2.5	-1	-72.0	
6	-2.5	-1.5	0	-80.625	
7	-2.5	-0.8	0	-66.56	

8. [M, None, 3.3.2] An NMOS device is plugged into the test configuration shown below in Figure 0.4. The input V_{in} =2V. The current source draws a constant current of 50 μA. *R* is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110*10^{-6}$ V/A^2, $V_T = 0.4$, and V_{DSAT} = 0.6V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and channel length modulation can be neglected. i.e λ=0, γ=0. .

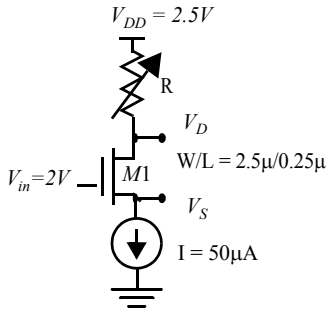


Figure 0.4 Test configuration for the NMOS device.

a. When *R* =10kΩ find the operation region, V_D and V_S.

b. When R= 30kΩ again determine the operation region V_D, V_S

c. For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively

9. [M, None, 3.3.2] Consider the circuit configuration of Figure 0.5.

a. Write down the equations (and only those) which are needed to determine the voltage at node *X*. Do NOT plug in any values yet. Neglect short channel effects and assume that $\lambda_p = 0$.

b. Draw the (approximative) load lines for both MOS transistor and resistor. Mark some of the significant points.

c. Determine the required width of the transistor (for $L = 0.25\mu m$) such that *X* equals 1.5 V.

d. We have, so far, assumed that M_1 is a long-channel device. Redraw the load lines assuming that M_1 is velocity-saturated. Will the voltage at *X* rise or fall?

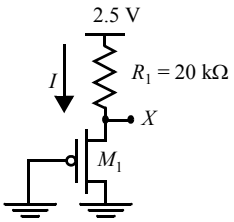


Figure 0.5 MOS circuit.

10. [M, None, 3.3.2] The circuit of Figure 0.6 is known as a *source-follower* configuration. It achieves a DC level shift between the input and output. The value of this shift is determined by the current I_0. Assume $\gamma = 0.4$, $2|\phi_f| = 0.6$ V, $V_{T0} = 0.43$ V, $k' = 115\ \mu A/V^2$, and $\lambda = 0$. The NMOS device has $W/L = 5.4\mu/1.2\mu$ such that the short channel effects are not observed.

a. Derive an expression giving V_i as a function of V_o and $V_T(V_o)$. If we neglect body effect, what is the nominal value of the level shift performed by this circuit.

b. The NMOS transistor experiences a shift in V_T due to the body effect. Find V_T as a function of V_o for V_o ranging from 0 to 1.5V with 0.25 V intervals. Plot V_T vs. V_o.

c. Plot V_o vs. V_i as V_o varies from 0 to 1.5 V with 0.25 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter? At V_o (body effect) = 1.5 V, find V_o (ideal) and, thus, determine the maximum error introduced by body effect.

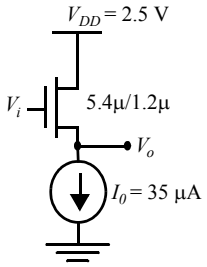


Figure 0.6 Source-follower level converter.

11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.

b. Repeat *a* using SPICE.

c. Repeat *a* and *b* using a MOS transistor with $(W / L) = 4 / 1$. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

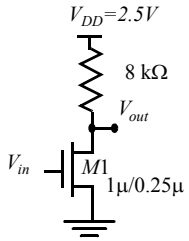


Figure 0.7 MOS circuit.

12. [E, None, 3.3.2]Below in Figure 0.8 is an I-V transfer curve for an NMOS transistor. In this problem, the objective is to use this I-V curve to obtain information about the transistor. The transistor has (W/L)=(1μ/1μ). It may also be assumed that velocity saturation does not play a role in this example. Also assume $-2\Phi_F$ = 0.6V. Using Figure 0.8 determine the following parameters: device V_{TO}, γ, λ.

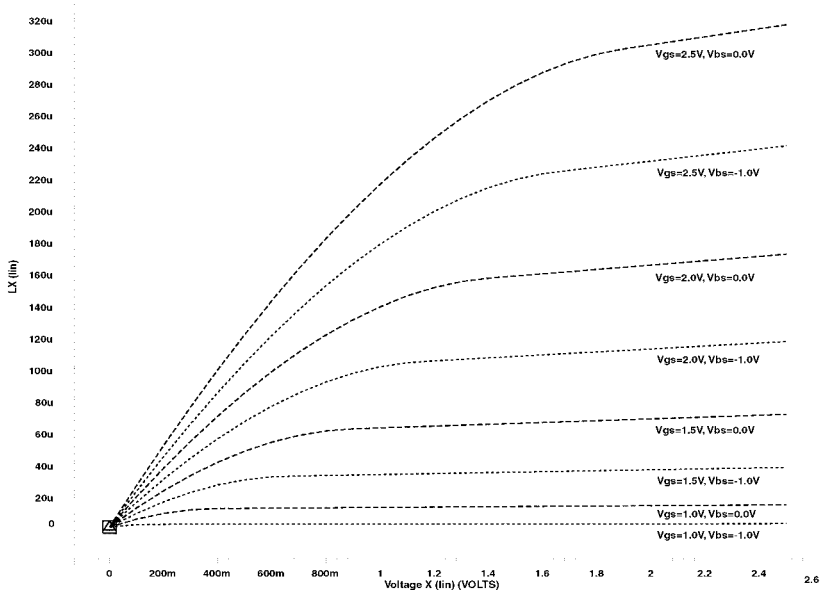


Figure 0.8 I-V curves

13. [E, None , 3.3.2]The curves below in Figure 0.9 represent the gate voltage(V_{GS}) vs. drain current (I_{DS}) of two NMOS devices which are on the same die and operate in subthreshold region. Due to process variations on the same die the curves do not overlap.

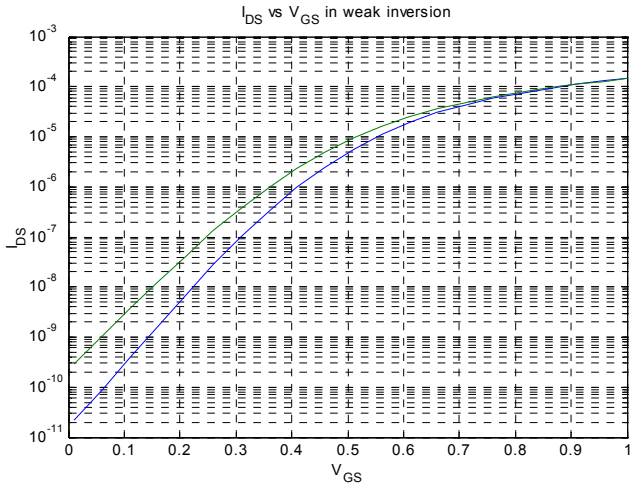


Figure 0.9 Subthreshold current curves. Difference is due to process variations

Also assume that the transistors are within the same circuit configurations as Figure 0.10 in If the in put voltages are both V_{in} = 0.2V. What would be the respective durations to discharge the load of C_L = 1pF attached to the drains of these devices.

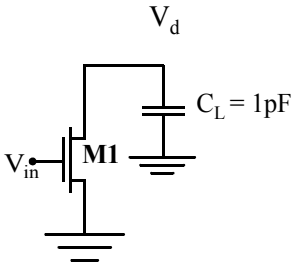


Figure 0.10 The circuit for testing the time to discharge the load capacitance through a device operating in subthreshold region.

14. [M, None, 3.3.2] Short-channel effects:

a. Use the fact that current can be expressed as the product of the carrier charge per unit length and the velocity of carriers (I_{DS} = Q*v)* to derive I_{DS} as a function of *W*, C_{ox}, $V_{GS} - V_T$, and carrier velocity *v.*

b. For a long-channel device, the carrier velocity is the mobility times the applied electric field. The electrical field, which has dimensions of V/m, is simply $(V_{GS} - V_T) / 2L$. Derive I_{DS} for a long-channel device.

c. From the equation derived in *a*, find I_{DS} for a short-channel device in terms of the maximum carrier velocity, v_{max}.

Based on the results of *b* and *c* describe the most important differences between short-channel and long-channel devices.

15. [C, None, 3.3.2] Another equation, which models the velocity-saturated drain current of an MOS transistor is given by

$$I_{dsat} = \frac{1}{1 + (V_{GS} - V_t)/(E_{sat}L)} \left(\frac{\mu_0 C_{ox}}{2} \right) \frac{W}{L} (V_{GS} - V_T)^2$$

Using this equation it is possible to see that velocity saturation can be modeled by a MOS device with a source-degeneration resistor (see Figure 0.11).

a. Find the value of R_S such that $I_{DSAT}(V_{GS}, V_{DS})$ for the composite transistor in the figure matches the above velocity-saturated drain current equation. *Hint: the voltage drop across R_S is typically small.*

b. Given $E_{sat} = 1.5$ V/μm and $k' = \mu_0 C_{ox} = 20$ μA/V^2, what value of R_S is required to model velocity saturation. How does this value depend on W and L?

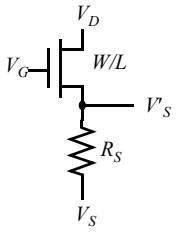


Figure 0.11 Source-degeneration model of velocity saturation.

16. [E, None, 3.3.2] The equivalent resistances of two different devices need to be computed.

a. First, consider the fictive device whose I-V characteristic is given in Figure 0.12. Constant k has the dimension of S (or1/Ω). V_0 is a voltage characteristic to the device. Calculate the equivalent resistance for an output voltage transition from 0 to $2V_0$ by integrating the resistance as a function of the voltage.

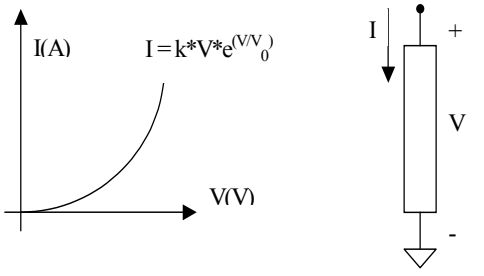


Figure 0.12 Fictive device whose equivalent resistance is to be calculated.

b. Next, obtain the resistance equation 3.43 using the Figure 0.13. Assuming the V_{GS} is kept at V_{DD}, Calculate the Req as output (V_{DS}) transitions from V_{DD} to $V_{DD}/2$.(Figure 0.13).

Hint: Make sure you use the Short channel Unified MOS Model equations. **Hint:** You will need to use the expansion. $ln(1+x) \approx x - x^2/2 + x^3/3$

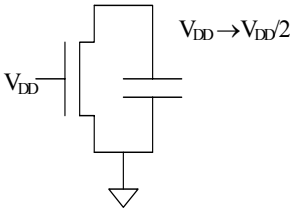


Figure 0.13 The equivalent resistance is to be computed for the H→L transition.

17. [M, None, 3.3.3] Compute the gate and diffusion capacitances for transistor *M*1 of Figure 0.7. Assume that drain and source areas are rectangular, and are 1 μm wide and 0.5 μm long. Use the parameters of Example 3.5 to determine the capacitance values. Assume $m_j = 0.5$ and $m_{jsw} = 0.44$. Also compute the total charge stored at node *In*, for the following initial conditions:

a. $V_{in} = 2.5$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

b. $V_{in} = 0$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

18. [E, None, 3.3.3]Consider a CMOS process with the following capacitive parameters for the NMOS transistor: C_{GSO}, C_{GDO}, C_{OX}, C_J, m_j, C_{jsw}, m_{jsw}, and PB, with the lateral diffusion equal to L_D. The MOS transistor M1 is characterized by the following parameters: W, L, AD, PD, AS, PS.

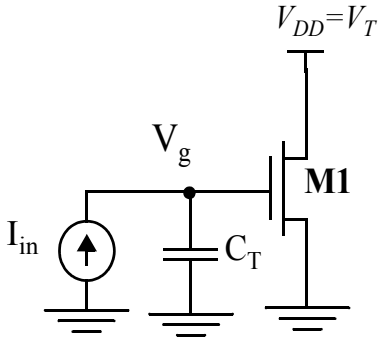


Figure 0.14 Circuit to measure total input capacitance

a. Consider the configuration of Figure 0.14. V_{DD} is equal to V_T (the threshold voltage of the transistor) Assume that the initial value of V_g equals 0. A current source with value I_{in} is applied at time 0. Assuming that all the capacitance at the gate node can be lumped into a single, grounded, linear capacitance C_T, derive an expression for the time it will take for V_g to reach 2 V_T

b. The obvious question is now how to compute C_T. Among, C_{db}, C_{sb}, C_{gs}, C_{gd}, C_{gb} which of these parasatic capacitances of the MOS transistor contribute to C_T. For those that contribute to C_T write down the expression that determines the value of the contribution. Use only the parameters given above. If the transistor goes through different operation regions and this impacts the value of the capacitor, **determine the expression of the contribution for each region (and indicate the region)**.

c. Consider now the case depicted in Figure 0.15. Asssume that V_d is initially at 0 and we want to charge it up to 2 V_T. Again among, C_{db}, C_{sb}, C_{gs}, C_{gd}, C_{gb} which device capacitances contribute to the total drain capacitance? Once again, make sure you differentiate between different operation regions..

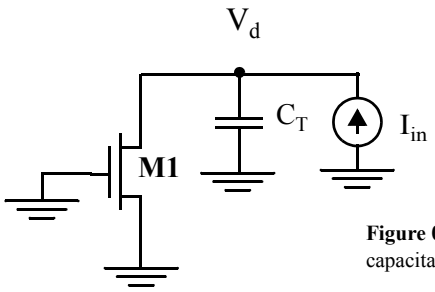


Figure 0.15 Circuit to measure the total drain capacitance

19. [M, None, 3.3.3]For the NMOS transistor in Figure 0.16, **sketch the voltages** at the source and at the drain as a function of time. Initially, both source and drain are at +2.5 volts. Note that the drain is open circuited. The 10 μA current source is turned on at t=0. Device parameters:W/L_{eff} = 125μ/0.25μ ; μC_{ox} = 100 μA/V^2 ; C_{ox} = 6fF/μ^2 ;C_{OL}(per width) = 0.3 fF/μ ; C_{sb} = 100 fF; Cdb = 100fF;V_{DSAT} =1V.

HINT: Do not try to solve this analytically. Just use a qualitative analysis to derive the different operation modes of the circuit and the devices**.**

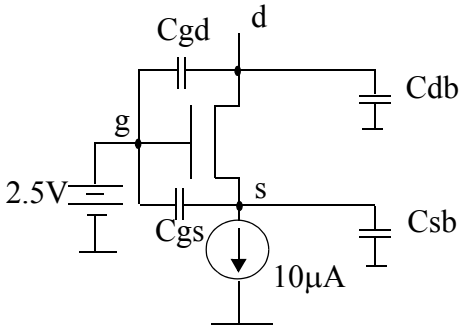


Figure 0.16 Device going through different operation regions over time

20. [C, SPICE, 3.4] Though impossible to quantify exactly by hand, it is a good idea to understand process variations and be able to at least get a rough estimate for the limits of their effects.

a. For the circuit of Figure 0.7, calculate nominal, minimum, and maximum currents in the NMOS device with V_{in} = 0 V, 2.5 V and 5 V. Assume 3σ variations in V_{T0} of 25 mV, in k' of 15%, and in lithographic etching of 0.15 μm.

b. Analyze the impact of these current variations on the output voltage. Assume that the load resistor also can vary by 10%. Verify the result with SPICE.

21. [E, None, 3.5] A state-of-the-art, synthesizable, embedded microprocessor consumes 0.4mW/MHz when fabricated using a 0.18 μm process. With typical standard cells (gates), the area of the processor is 0.7 mm2. Assuming a 100 Mhz clock frequency, and 1.8 V power

supply. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

a. Using fixed voltage scaling and constant frequency, what will the area, power consumption, and power density of the same processor be, if scaled to 0.12 μm technology, assuming the same clock frequency?

b. If the supply voltage in the scaled 0.12 μm part is reduced to 1.5 V what will the power consumption and power density be?

c. How fast could the scaled processor in Part (b) be clocked? What would the power and power density be at this new clock frequency?

d. Power density is important for cooling the chip and packaging. What would the supply voltage have to be to maintain the same power density as the original processor?

22. The superscalar, superpipelined, out-of-order executing, highly parallel, fully x86 compatible JMRII microprocessor was fabricated in a 0.25 m technology and was able to operate at 100 MHZ, consuming 10 watts using a 2.5 V power supply.

a. Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 0.1 μm technology?

b. If the supply voltage on the 0.1 μm part were scaled to 1.0 V, what will the power consumption and speed be?

c. What supply should be used to fix the power consumption at 10 watts? At what speed would the processor operate?

Chapter 4

Problems

1. [M, None, 4.x] Figure 0.1 shows a clock-distribution network. Each segment of the clock network (between the nodes) is 5 mm long, 3 μm wide, and is implemented in polysilicon. At each of the terminal nodes (such as *R*) resides a load capacitance of 100 fF.

a. Determine the average current of the clock driver, given a voltage swing on the clock lines of 5 V and a maximum delay of 5 nsec between clock source and destination node *R*. For this part, you may ignore the resistance and inductance of the network

b. Unfortunately the resistance of the polysilicon cannot be ignored. Assume that each straight segment of the network can be modeled as a Π-network. Draw the equivalent circuit and annotate the values of resistors and capacitors.

c. Determine the dominant time-constant of the clock response at node *R*.

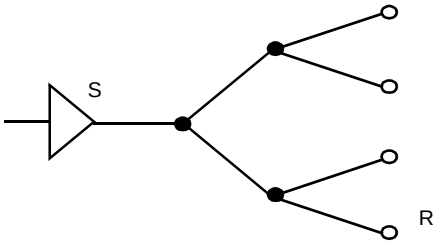


Figure 0.1 Clock-distribution network.

2. [C, SPICE, 4.x] You are designing a clock distribution network in which it is critical to minimize skew between local clocks (*CLK*1, *CLK*2, and *CLK*3). You have extracted the *RC* network of Figure 0.2, which models the routing parasitics of your clock line. Initially, you notice that the path to *CLK*3 is shorter than to *CLK*1 or *CLK*2. In order to compensate for this imbalance, you insert a transmission gate in the path of *CLK*3 to eliminate the skew.

a. Write expressions for the time-constants associated with nodes *CLK*1, *CLK*2 and *CLK*3. Assume the transmission gate can be modeled as a resistance R_3.

b. If $R_1 = R_2 = R_4 = R_5 = R$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C$, what value of R_3 is required to balance the delays to *CLK*1, *CLK*2, and *CLK*3?

c. For $R = 750\Omega$ and $C = 200$fF, what (W/L)'s are required in the transmission gate to eliminate skew? Determine the value of the propagation delay.

d. Simulate the network using SPICE, and compare the obtained results with the manually obtained numbers.

3. [M, None, 4.x]Consider a CMOS inverter followed by a wire of length *L*. Assume that in the reference design, inverter and wire contribute equally to the total propagation delay t_{pref}. You may assume that the transistors are velocity-saturated. The wire is scaled in line with the **ideal wire scaling model**. Assume initially that the wire is **a local wire**.

a. Determine the new (total) propagation delay as a a function of t_{pref}, assuming that technology and supply voltage scale with a factor 2. Consider only first-order effects.

b. Perform the same analysis, assuming now that the wire scales a **global wire**, and the wire length scales inversely proportional to the technology.

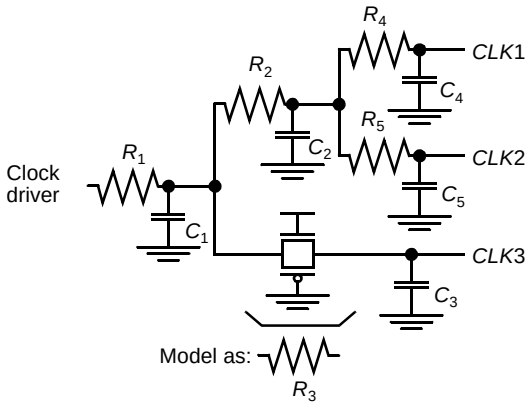


Figure 0.2 *RC* clock-distribution network.

c. Repeat b, but assume now that the wire is scaled along the constant resistance model. You may ignore the effect of the fringing capacitance.

d. Repeat b, but assume that the new technology uses a better wiring material that reduces the resistivity by half, and a dielectric with a 25% smaller permittivity.

e. Discuss the energy dissipation of part a. as a function of the energy dissipation of the original design E_{ref}.

f. Determine for each of the statements below if it is true, false, or undefined, and explain in one line your answer.

- When driving a small fan-out, increasing the driver transistor sizes raises the short-circuit power dissipation.
- Reducing the supply voltage, while keeping the threshold voltage constant decreases the short-circuit power dissipation.
- Moving to Copper wires on a chip will enable us to build faster adders.
- Making a wire wider helps to reduce its RC delay.
- Going to dielectrics with a lower permittivity will make RC wire delay more important.

4. [M, None, 4.x] A two-stage buffer is used to drive a metal wire of 1 cm. The first inverter is of minimum size with an input capacitance Ci=10 fF and an internal propagation delay t_{p0}=50 ps and load dependent delay of 5ps/fF. The width of the metal wire is 3.6 μm. The sheet resistance of the metal is 0.08 Ω/ , the capacitance value is 0.03 fF/μm2 and the fringing field capacitance is 0.04fF/μm.

a. What is the propagation delay of the metal wire?

b. Compute the optimal size of the second inverter. What is the minimum delay through the buffer?

c. If the input to the first inverter has 25% chance of making a 0-to-1 transition, and the whole chip is running at 20MHz with a 2.5 supply voltage, then what's the power consumed by the metal wire?

5. [M, None, 4.x]To connect a processor to an external memory an off -chip connection is necessary. The copper wire on the board is 15 cm long and acts as a transmission line with a characteristic impedance of 100Ω(See Figure 0.3). The memory input pins present a very high impedance which can be considered infinite. The bus driver is a CMOS inverter consisting of very large devices: (50/0.25) for the NMOS and (150/0.25) for the PMOS, where all sizes are

in µm. The minimum size device, (0.25/0.25) for NMOS and (0.75/0.25) for PMOS, has the on resistance 35 kΩ.

a. Determine the time it takes for a change in the signal to propagate from source to destination (time of flight). The wire inductance per unit length equals $75*10^{-8}$ H/m.

b. Determine how long it will take the output signal to stay within 10% of its final value. You can model the driver as a voltage source with the driving device acting as a series resistance. Assume a supply and step voltage of 2.5V. Hint: draw the lattice diagram for the transmission line.

c. Resize the dimensions of the driver to minimize the total delay.

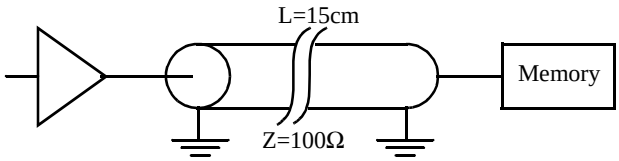


Figure 0.3 The driver, the connecting copper wire and the memory block being accessed.

6. [M, None, 4.x] A two stage buffer is used to drive a metal wire of 1 cm. The first inverter is a minimum size with an input capacitance C_i=10 fF and a propagation delay t_{p0}=175 ps when loaded with an identical gate. The width of the metal wire is 3.6 µm. The sheet resistance of the metal is 0.08 Ω/ , the capacitance value is 0.03 fF/µm2 and the fringing field capacitance is 0.04 fF/µm.

a. What is the propagation delay of the metal wire?

b. Compute the optimal size of the second inverter. What is the minimum delay through the buffer?

7. [M, None, 4.x] For the RC tree given in Figure 0.4 calculate the Elmore delay from node A to node B using the values for the resistors and capacitors given in the below in Table 0.1.

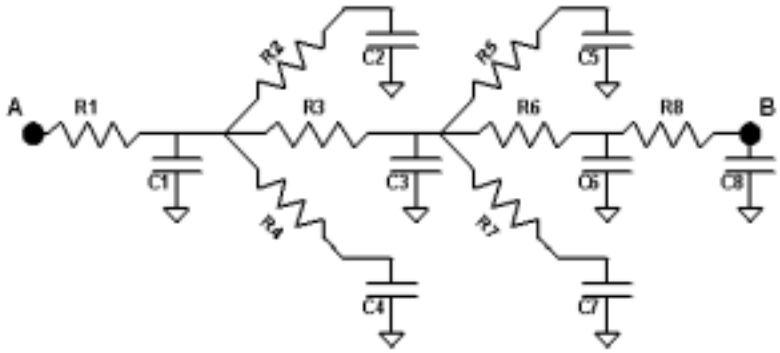


Figure 0.4 RC tree for calculating the delay

Table 0.1 Values of the components in the RC tree of Figure 0.4

Resistor	Value(Ω)	Capacitor	Value(fF)
R1	0.25	C1	250
R2	0.25	C2	750
R3	0.50	C3	250
R4	100	C4	250
R5	0.25	C5	1000
R6	1.00	C6	250
R7	0.75	C7	500
R8	1000	C8	250

8. [M, SPICE, 4.x] In this problem the various wire models and their respective accuracies will be studied.

a. Compute the 0%-50% delay of a 500um x 0.5um wire with resistance of 0.08 Ω/ , with area capacitance of 30aF/um2, and fringing capacitance of 40aF/um. Assume the driver has a 100Ω resistance and negligible output capacitance.

- Using a lumped model for the wire.
- Using a PI model for the wire, and the Elmore equations to find tau. (see Chapter 4, figure 4.26).
- Using the distributed RC line equations from Chapter 4, section 4.4.4.

b. Compare your results in part a. using spice (be sure to include the source resistance). For each simulation, measure the 0%-50% time for the output

- First, simulate a step input to a lumped R-C circuit.
- Next, simulate a step input to your wire as a PI model.
- Unfortunately, our version of SPICE does not support the distributed RC model as described in your book (Chapter 4, section 4.5.1). Instead, simulate a step input to your wire using a PI3 distributed RC model.

9. [M, None, 4.x] A standard CMOS inverter drives an aluminum wire on the first metal layer. Assume Rn=4kΩ, Rp=6kΩ. Also, assume that the output capacitance of the inverter is negligible in comparison with the wire capacitance. The wire is .5um wide, and the resistivity is 0.08 Ω/ ..

a. What is the "critical length" of the wire?

b. What is the equivalent capacitance of a wire of this length? (For your capacitance calculations, use Table 4.2 of your book , assume there's field oxide underneath and nothing above the aluminum wire)

10. [M, None, 4.x] A 10cm long lossless transmission line on a PC board (relative dielectric constant = 9, relative permeability = 1) with characteristic impedance of 50Ω is driven by a 2.5V pulse coming from a source with 150Ω resistance.

a. If the load resistance is infinite, determine the time it takes for a change at the source to reach the load (time of flight).

Now a 200Ω load is attached at the end of the transmission line.

b. What is the voltage at the load at t = 3ns?

c. Draw lattice diagram and sketch the voltage at the load as a function of time. Determine how long does it take for the output to be within 1 percent of its final value.

11. [C, SPICE, 4.x] Assume V_{DD}=1.5V. Also, use short-channel transistor models forhand analysis.

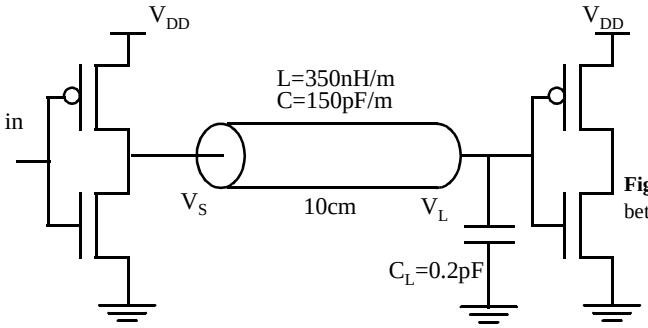


Figure 0.5 Transmission line between two inverters

a. The Figure 0.5 shows an output driver feeding a 0.2 pF effective fan-out of CMOS gates through a transmission line. Size the two transistors of the driver to optimize the delay. Sketch waveforms of V_S and V_L, assuming a square wave input. Label critical voltages and times.

b. Size down the transistors by m times (m is to be treated as a parameter). Derive a first order expression for the time it takes for V_L to settle down within 10% of its final voltage level.Compare the obtained result with the case where no inductance is associated with the wire.Please draw the waveforms of V_L for both cases, and comment.

c. Use the transistors as in part a). Suppose C_L is changed to 20pF. Sketch waveforms of V_S and V_L, assuming a square wave input. Label critical voltages and instants.

d. Assume now that the transmission line is lossy. Perform Hspice simulation for three cases: R=100 Ω/cm; R=2.5 Ω/cm; R=0.5 Ω/cm. Get the waveforms of V_S, V_L and the middle point of the line. Discuss the results.

12. [M, None, 4.x] Consider an isolated 2mm long and 1μm wide M1(Metal1)wire over a silicon substrate driven by an inverter that has zero resistance and parasitic output capccitance. How will the wire delay change for the following cases? Explain your reasoning in each case.

a. If the wire width is doubled.

b. If the wire length is halved.

c. If the wire thickness is doubled.

d. If thickness of the oxide between the M1 and the substrate is doubled.

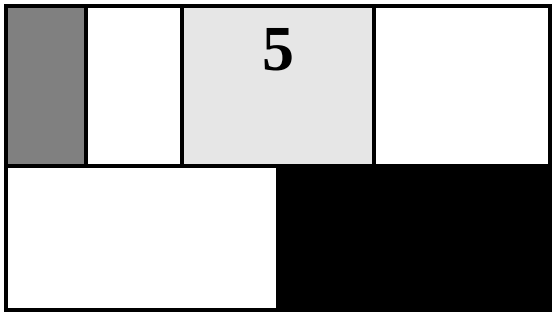
13. [E, None, 4.x] In an ideal scaling model, where all dimensions and voltages scale with a factor of S >1 :

a. How does the delay of an inverter scale?

b. If a chip is scaled from one technology to another where all wire dimensions,including the vertical one and spacing, scale with a factor of S, how does the wire delayscale? How does the overall operating frequency of a chip scale?

c. Repeat b) for the case where everything scales, except the vertical dimension of wires (it stays constant).

CHAPTER



THE CMOS INVERTER

Quantification of integrity, performance, and energy metrics of an inverter
Optimization of an inverter design

5.1 Exercises and Design Problems

1. [M, SPICE, 3.3.2] The layout of a static CMOS inverter is given in Figure 5.1. (λ = 0.125 µm).

a. Determine the sizes of the NMOS and PMOS transistors.

b. Plot the VTC (using HSPICE) and derive its parameters (V_{OH}, V_{OL}, V_M, V_{IH}, and V_{IL}).

c. Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates?.

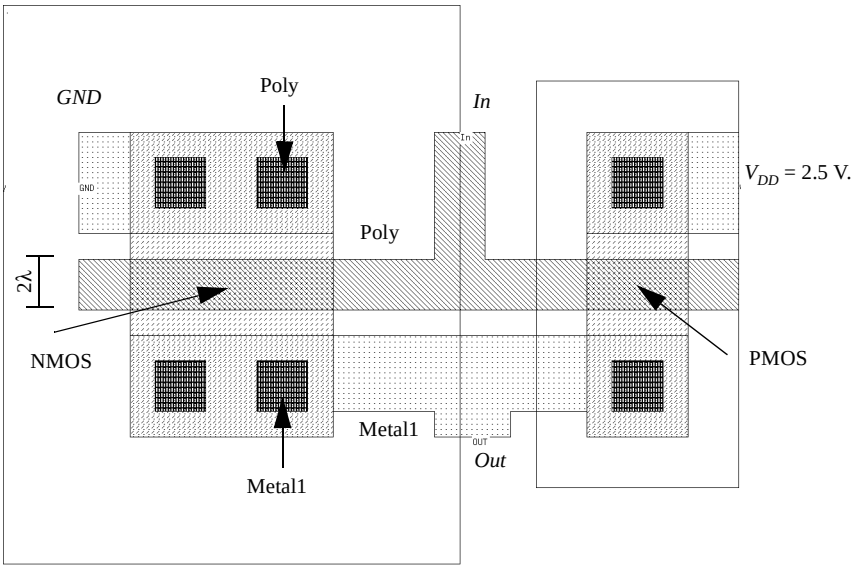


Figure 5.1 CMOS inverter layout.

d. Resize the inverter to achieve a switching threshold of approximately 0.75 V. Do not lay-out the new inverter, use HSPICE for your simulations. How are the noise margins affected by this modification?

2. Figure 5.2 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at V_M. The intersection of this line with the V_{OH} and the V_{OL} lines defines V_{IH} and V_{IL}.

a. The noise margins of a CMOS inverter are highly dependent on the sizing ratio, $r = k_p/k_n$, of the NMOS and PMOS transistors. Use HSPICE with $V_{Tn} = |V_{Tp}|$ to determine the value of r that results in equal noise margins? Give a qualitative explanation.

b. Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for NM_H and NM_L in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at V_M. For what range of r is this assumption valid? What is the resulting range of V_M?

c. Derive expressions for the inverter gain at V_M for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region: $r_{o,sat} = 1/(\lambda I_D)$.

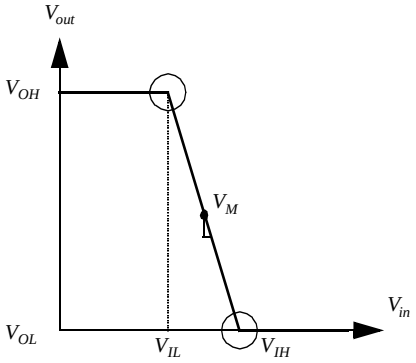


Figure 5.2 A different approach to derive V_{IL} and V_{IH}.

3. [M, SPICE, 3.3.2] Figure 5.3 shows an NMOS inverter with resistive load.

a. Qualitatively discuss why this circuit behaves as an inverter.

b. Find V_{OH} and V_{OL} calculate V_{IH} and V_{IL}.

c. Find NM_L and NM_H, and plot the VTC using HSPICE.

d. Compute the average power dissipation for: (i) V_{in} = 0 V and (ii) V_{in} = 2.5 V

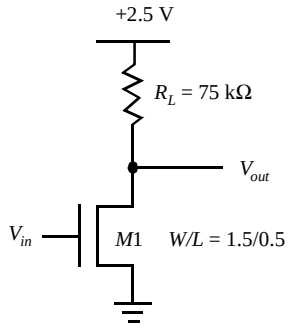


Figure 5.3 Resistive-load inverter

e. Use HSPICE to sketch the VTCs for R_L = 37k, 75k, and 150k on a single graph.

f. Comment on the relationship between the critical VTC voltages (i.e., V_{OL}, V_{OH}, V_{IL}, V_{IH}) and the load resistance, R_L.

g. Do high or low impedance loads seem to produce more ideal inverter characteristics?

4. [E, None, 3.3.3] For the inverter of Figure 5.3 and an output load of 3 pF:

a. Calculate t_{plh}, t_{phl}, and t_p.

b. Are the rising and falling delays equal? Why or why not?

c. Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible.

5. The next figure shows two implementations of MOS inverters. The first inverter uses only NMOS transistors.

a. Calculate V_{OH}, V_{OL}, V_M for each case.

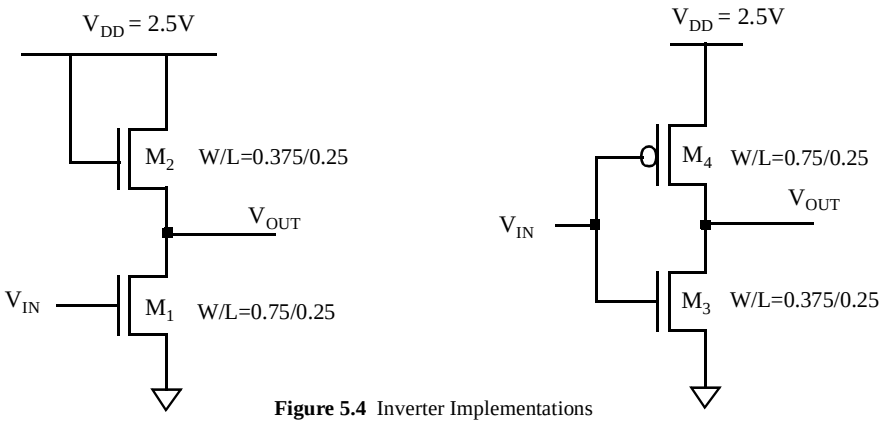


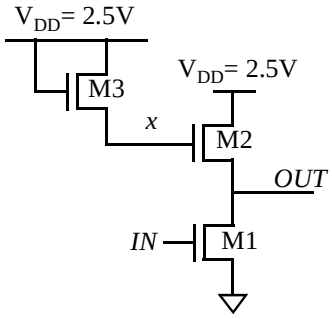
Figure 5.4 Inverter Implementations

b. Use HSPICE to obtain the two VTCs. You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0.125$ μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

c. Find V_{IH}, V_{IL}, NM_L and NM_H for each inverter and comment on the results. How can you increase the noise margins and reduce the undefined region?

d. Comment on the differences in the VTCs, robustness and regeneration of each inverter.

6. Consider the following NMOS inverter. Assume that the bulk terminals of all NMOS device are connected to GND. Assume that the input IN has a 0V to 2.5V swing.



a. Set up the equation(s) to compute the voltage on node *x*. Assume γ=0.5.

b. What are the modes of operation of device M2? Assume γ=0.

c. What is the value on the output node *OUT* for the case when *IN* =0V?Assume γ=0.

d. Assuming γ=0, derive an expression for the switching threshold (V_M) of the inverter. Recall that the switching threshold is the point where $V_{IN}= V_{OUT}$. Assume that the device sizes for M1, M2 and M3 are $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ respectively. What are the limits on the switching threshold?

For this, consider two cases:

i) $(W/L)_1 >> (W/L)_2$

ii) $(W/L)_2 >> (W/L)_1$

7. Consider the circuit in Figure 5.5. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of -0.4V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input *IN* has a 0V to 2.5V swing.

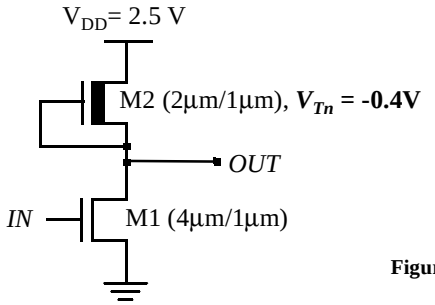


Figure 5.5 A depletion load NMOS inverter

a. Device M2 has its gate terminal connected to its source terminal. If V_{IN} = 0V, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?

b. Compute the output voltage for V_{IN} = 2.5V. You may assume that V_{OUT} is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?

c. Assuming $Pr_{(IN=0)}$= 0.3, what is the static power dissipation of this circuit?

8. [M, None, 3.3.3] An NMOS transistor is used to charge a large capacitor, as shown in Figure 5.6.

a. Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to 2.5V at the input node.

b. Assume that a resistor R_S of 5 kΩ is used to discharge the capacitance to ground. Determine t_{pHL}.

c. Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1. How much is dissipated in the pull-down resistance during discharge? How does this change when R_S is reduced to 1 kΩ.

d. The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

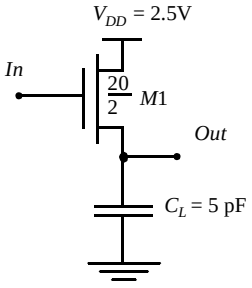


Figure 5.6 Circuit diagram with annotated *W/L* ratios

9. The circuit in Figure 5.7 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0. Assume x_d=0, γ=0.4, $2|\phi_f|$=0.6V, V_{T0}=0.43V, k_n'=115μA/V^2 and λ=0.

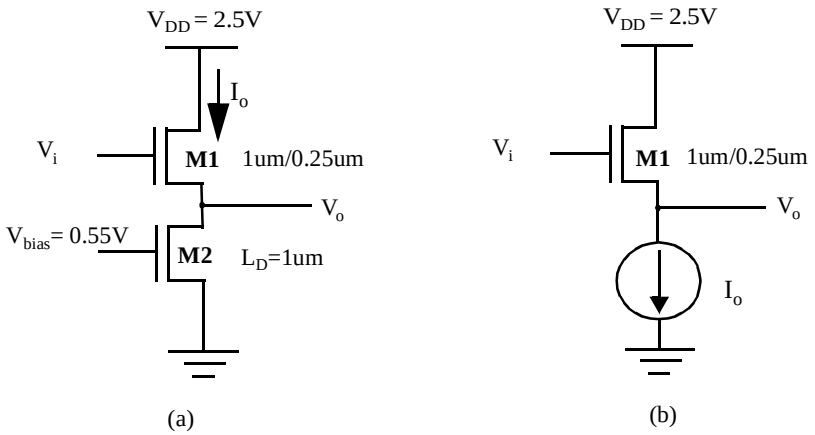


Figure 5.7 NMOS source follower configuration

a. Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Figure 5.7 (a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate V_i to V_o in terms of I_o).

b. Now assume that an ideal current source replaces M2 (Figure 5.7 (b)). The NMOS transistor M1 experiences a shift in V_T due to the backgate effect. Find V_T as a function of V_o for V_o ranging from 0 to 2.5V with 0.5V intervals. Plot V_T vs. V_o

c. Plot V_o vs. V_i as V_o varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter?

d. At V_o(with body effect) = 2.5V, find V_o(ideal) and thus determine the maximum error introduced by the body effect.

10. For this problem assume:

V_{DD} = 2.5V, W_P/L = 1.25/0.25, W_N/L = 0.375/0.25, $L=L_{eff}$ =0.25μm (i.e. x_d= 0μm), $C_L=C_{inv\text{-}gate}$, k_n' = 115μA/V^2, k_p'= -30μA/V^2, V_{tn0} = | V_{tp0} | = 0.4V, λ = 0V^{-1}, γ = 0.4, 2|ϕ_f|=0.6V, and t_{ox} = 58A. Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gd0}, C_j, C_{jsw}), and assume that V_{SB}=0V for all problems except part **(e)**.

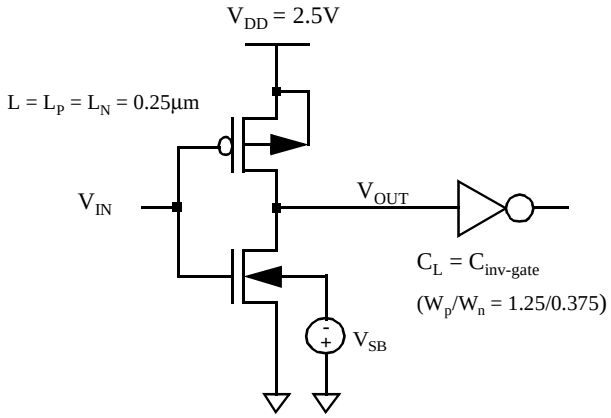


Figure 5.8 CMOS inverter with capacitive

Parasitic Capacitance Parameters (F/m)##
NMOS: CGDO=3.11x10^{-10}, CGSO=3.11x10^{-10}, CJ=2.02x10^{-3}, CJSW=2.75x10^{-10}
PMOS: CGDO=2.68x10^{-10}, CGSO=2.68x10^{-10}, CJ=1.93x10^{-3}, CJSW=2.23x10^{-10}

a. What is the V_m for this inverter?

b. What is the effective load capacitance C_{Leff} of this inverter? (include parasitic capacitance, refer to the text for K_{eq} and m.) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, λ = 0.125 µm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

c. Calculate t_{PHL}, t_{PLH} assuming the result of (b) is 'C_{Leff} = 6.5fF'. (Assume an ideal step input, i.e. t_{rise}=t_{fall}=0. Do this part by computing the average current used to charge/discharge C_{Leff}.)

d. Find (W_p/W_n) such that $t_{PHL} = t_{PLH}$.

e. Suppose we increase the width of the transistors to reduce the t_{PHL}, t_{PLH}. Do we get a proportional decrease in the delay times? Justify your answer.

f. Suppose V_{SB} = 1V, what is the value of V_{tn}, V_{tp}, V_m? How does this qualitatively affect C_{Leff}?

11. Using Hspice answer the following questions.

a. Simulate the circuit in Problem 10 and measure t_P and the average power for input V_{in}: pulse(0 V_{DD} 5n 0.1n 0.1n 9n 20n), as V_{DD} varies from 1V - 2.5V with a 0.25V interval. [t_P = (t_{PHL} + t_{PLH}) / 2]. Using this data, plot 't_P vs. V_{DD}', and 'Power vs. V_{DD}'.

Specify AS, AD, PS, PD in your spice deck, and manually add C_L = 6.5fF. Set V_{SB} = 0V for this problem.

b. For Vdd equal to 2.5V determine the maximum fan-out of identical inverters this gate can drive before its delay becomes larger than 2 ns.

c. Simulate the same circuit for a set of 'pulse' inputs with rise and fall times of $t_{in\_rise,fall}$ =1ns, 2ns, 5ns, 10ns, 20ns. For each input, measure (1) the rise and fall times t_{out_rise} and

t_{out_fall} of the inverter output, (2) the total energy lost E_{total}, and (3) the energy lost due to short circuit current E_{short}.

Using this data, prepare a plot of (1) $(t_{out\_rise}+t_{out\_fall})/2$ vs. $t_{in\_rise,fall}$, (2) E_{total} vs. $t_{in\_rise,fall}$, (3) E_{short} vs. $t_{in\_rise,fall}$ and (4) E_{short}/E_{total} vs. $t_{in\_rise,fall.}$

d. Provide simple explanations for:

(i) Why the slope for (1) is less than 1?
(ii) Why E_{short} increases with $t_{in\_rise,fall}$?
(iii) Why E_{total} increases with $t_{in\_rise,fall}$?

12. Consider the low swing driver of Figure 5.9:

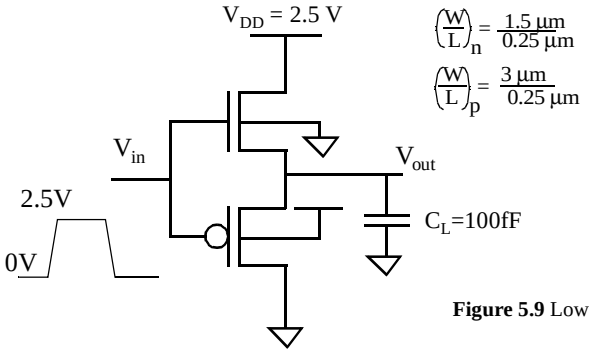


Figure 5.9 Low Swing Driver

a. What is the voltage swing on the output node (V_{out})? Assume γ=0.

b. Estimate (i) the energy drawn from the supply and (ii) energy dissipated for a 0V to 2.5V transition at the input. Assume that the rise and fall times at the input are 0. Repeat the analysis for a 2.5V to 0V transition at the input.

c. Compute t_{pLH} (i.e. the time to transition from V_{OL} to $(V_{OH} + V_{OL})/2$). Assume the input rise time to be 0. V_{OL} is the output voltage with the input at 0V and V_{OH} is the output voltage with the input at 2.5V.

d. Compute V_{OH} taking into account body effect. Assume $\gamma = 0.5V^{1/2}$ for both NMOS and PMOS.

13. Consider the following low swing driver consisting of NMOS devices M1 and M2. Assume an NWELL implementation. Assume that the inputs IN and $\overline{IN}$ have a 0V to 2.5V swing and that V_{IN} = 0V when $V_{\overline{IN}}$ = 2.5V and vice-versa. Also assume that there is no skew between IN and $\overline{IN}$ (i.e., the inverter delay to derive $\overline{IN}$ from IN is zero).

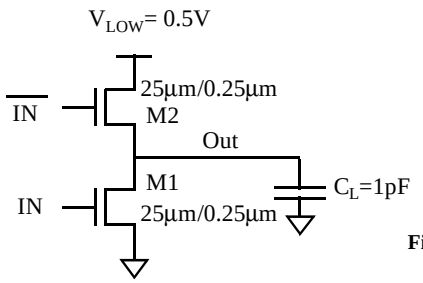


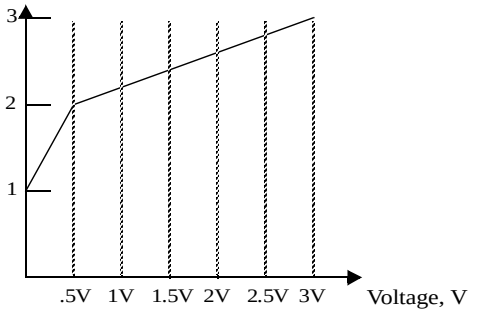
Figure 5.10 Low Swing Driver

a. What voltage is the bulk terminal of M2 connected to?

b. What is the voltage swing on the output node as the inputs swing from 0V to 2.5V. Show the low value and the high value.

c. Assume that the inputs IN and $\overline{IN}$ have zero rise and fall times. Assume a zero skew between IN and $\overline{IN}$. Determine the low to high propagation delay for charging the output node measured from the the 50% point of the input to the 50% point of the output. Assume that the total load capacitance is 1pF, including the transistor parasitics.

d. Assume that, instead of the 1pF load, the low swing driver drives a non-linear capacitor, whose capacitance vs. voltage is plotted below. Compute the energy drawn from the low supply for charging up the load capacitor. Ignore the parasitic capacitance of the driver circuit itself.



14. The inverter below operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I_0 and n.

a. Calculate the switching threshold (V_M) of this inverter.

b. Calculate V_{IL} and V_{IH} of the inverter.

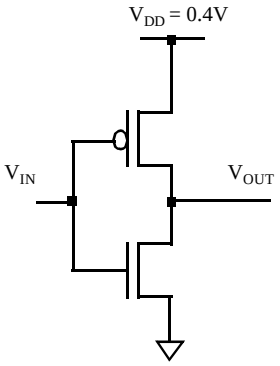


Figure 5.11 Inverter in Weak Inversion Regime

15. Sizing a chain of inverters.

a. In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume

that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

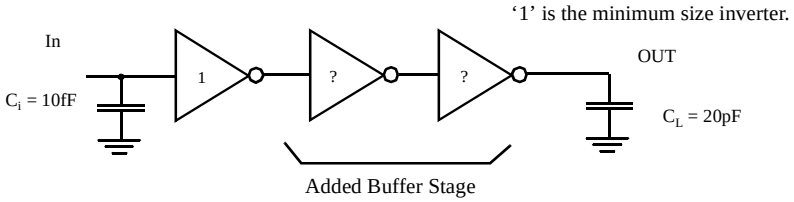


Figure 5.12 Buffer insertion for driving large loads.

b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

16. [M, None, 3.3.5] Consider scaling a CMOS technology by $S > 1$. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a. In traditional constant voltage scaling, transistor widths scale inversely with S, $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for *W*. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).

b. How does delay scale under this new methodology?

c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

DESIGN PROBLEM

Using the 0.25 μm CMOS introduced in Chapter 2, design a static CMOS inverter that meets the following requirements:

1. Matched pull-up and pull-down times (i.e., $t_{pHL} = t_{pLH}$).
2. $t_p = 5$ nsec ($\pm$ 0.1 nsec).

The load capacitance connected to the output is equal to 4 pF. Notice that this capacitance is substantially larger than the internal capacitances of the gate.

Determine the W and L of the transistors. To reduce the parasitics, use minimal lengths ($L = 0.25$ μm) for all transistors. Verify and optimize the design using SPICE after proposing a first design using manual computations. Compute also the energy consumed per transition. If you have a layout editor (such as MAGIC) available, perform the physical design, extract the real circuit parameters, and compare the simulated results with the ones obtained earlier.

Chapter 6
PROBLEMS

1. [E, None, 4.2] Implement the equation $X = ((\overline{A} + \overline{B})\ (\overline{C} + \overline{D} + \overline{E}) + \overline{F})\ \overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 6$. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?

2. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

$$\overline{Y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

3. Consider the circuit of Figure 6.1.

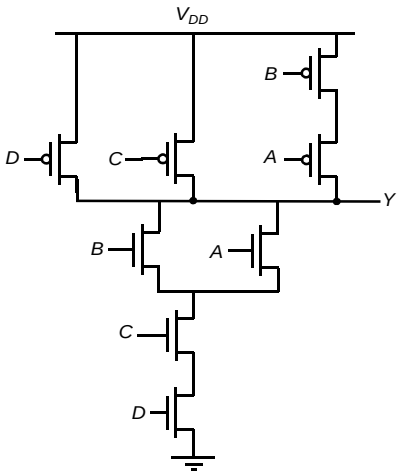


Figure 6.1 CMOS combinational logic gate.

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

c. Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).

d. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

4. [M, None, 4.2] CMOS Logic

a. Do the following two circuits (Figure 6.2) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b. Will these two circuits' output resistances always be equal to each other?

c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?

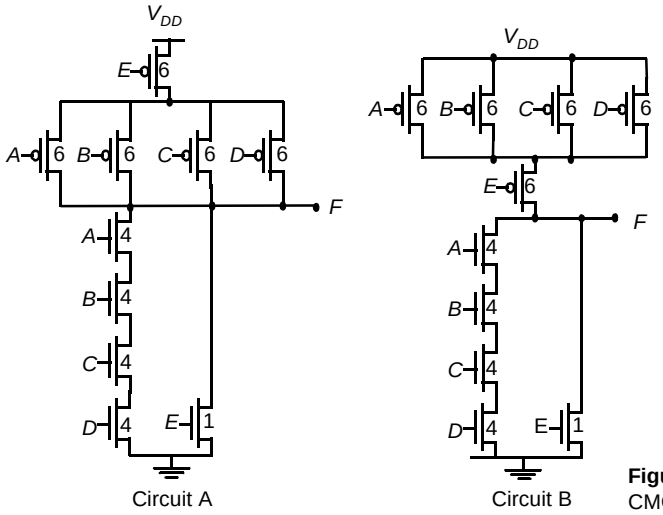


Figure 6.2 Two static CMOS gates.

5. [E, None, 4.2] The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.

a. What input patterns (*A*–*E*) give the lowest output resistance when the output is low? What is the value of that resistance?

b. What input patterns (*A*–*E*) give the lowest output resistance when the output is high? What is the value of that resistance?

6. [E, None, 4.2] What is the logic function of circuits A and B in Figure 6.3? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.

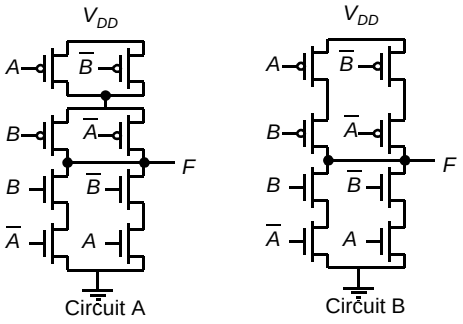


Figure 6.3 Two logic functions.

7. [E, None, 4.2] Compute the following for the pseudo-NMOS inverter shown in Figure 6.4:

a. V_{OL} and V_{OH}

b. NM_L and NM_H

c. The power dissipation: (1) for V_{in} low, and (2) for V_{in} high

d. For an output load of 1 pF, calculate t_{pLH}, t_{pHL}, and t_p. Are the rising and falling delays equal? Why or why not?

8. [M, SPICE, 4.2] Consider the circuit of Figure 6.5.

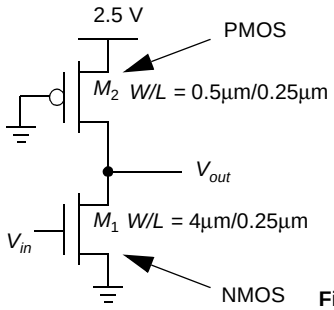


Figure 6.4 Pseudo-NMOS inverter.

a. What is the output voltage if only one input is high? If all four inputs are high?

b. What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

c. Compare your analytically obtained results to a SPICE simulation.

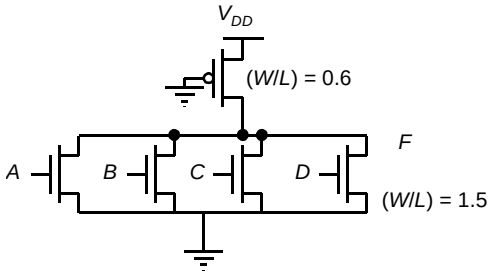


Figure 6.5 Pseudo-NMOS gate.

9. [M, None, 4.2] Implement $F = A\overline{BC} + \overline{A}CD$ (and $\overline{F}$) in DCVSL. Assume *A*, *B*, *C*, *D*, and their complements are available as inputs. Use the minimum number of transistors.

10. [E, Layout, 4.2] A complex logic gate is shown in Figure 6.6.

a. Write the Boolean equations for outputs *F* and *G*. What function does this circuit implement?

b. What logic family does this circuit belong to?

c. Assuming *W*/*L* = 0.5u/0.25u for *all nmos* transistors and *W*/*L* = 2u/0.25u for the *pmos* transistors, produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1.

d. Extract and netlist the layout. Load both outputs (F,G) with a 30fF capacitance and simulate the circuit. Does the gate function properly? If not, explain why and resize the transistors so that it does. Change the sizes (and areas and perimeters) in the HSPICE netlist.

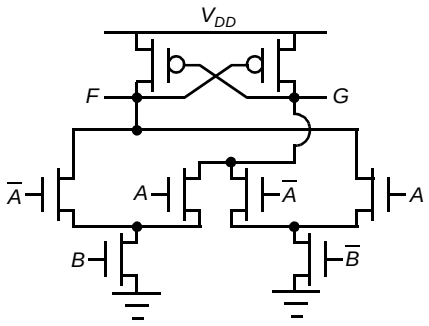


Figure 6.6 Two-input complex logic gate.

11. Design and simulate a circuit that generates an optimal differential signal as shown in Figure 6.7. Make sure the rise and fall times are equal.

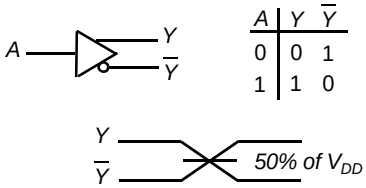


Figure 6.7 Differential Buffer.

12. What is the function of the circuit in Figure 6.8?

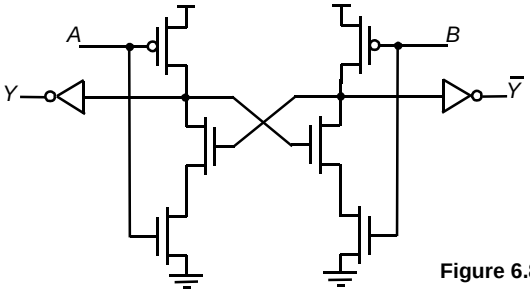


Figure 6.8 Gate.

13. Implement the function $S = ABC + A\overline{BC} + \overline{AB}C + \overline{A}B\overline{C}$, which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume *A*, *B*, *C*, and their complements are available as inputs.

14. Describe the logic function computed by the circuit in Figure 6.9. Note that all transistors (except for the middle inverters) are NMOS. Size and simulate the circuit so that it achieves a

100 ps delay (50-50) using 0.25μm devices, while driving a 100 fF load on both differential outputs. (V_{DD} = 2.5V) Assume *A*, *B* and their complements are available as inputs.

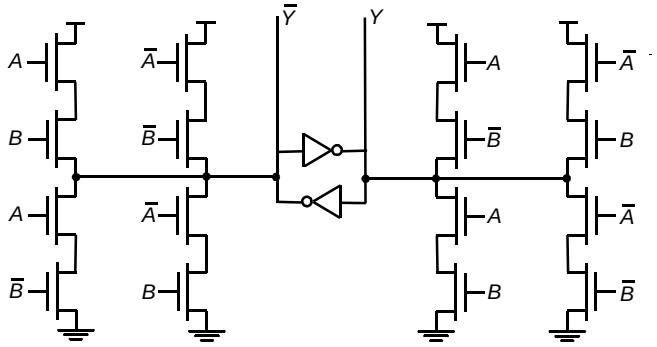


Figure 6.9 Cascoded Logic Styles.

For the drain and source perimeters and areas you can use the following approximations: AS=AD=W*0.625u and PS=PD=W+1.25u.

15. [M, None. 4.2] Figure 6.10 contains a pass-gate logic network.

a. Determine the truth table for the circuit. What logic function does it implement?

b. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a V_{OL} = 0.3 V.

c. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

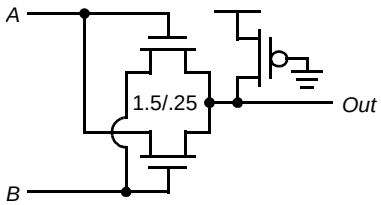


Figure 6.10 Pass-gate network.

16. [M, None, 4.2] This problem considers the effects of process scaling on pass-gate logic.

a. If a process has a t_{buf} of 0.4 ns, R_{eq} of 8 kΩ, and *C* of 12 fF, what is the optimal number of stages between buffers in a pass-gate chain?

b. Suppose that, if the dimension of this process are shrunk by a factor *S*, R_{eq} scales as $1/S^2$, *C* scales as $1/S$, and t_{buf} scales as $1/S^2$. What is the expression for the optimal number of buffers as a function of *S*? What is this value if *S* = 2?

17. [C, None, 4.2] Consider the circuit of Figure 6.11. Let C_x = 50 fF, M_r has *W*/*L* = 0.375/0.375, M_n has W/L_{eff} = 0.375/0.25. Assume the output inverter doesn't switch until its input equals $V_{DD}/2$.

a. How long will it take M_n to pull down node *x* from 2.5 V to 1.25 V if *In* is at 0 V and *B* is at 2.5V?

b. How long will it take M_n to pull up node *x* from 0 V to 1.25 V if V_{In} is 2.5 V and V_B is 2.5 V?

c. What is the minimum value of V_B necessary to pull down V_x to 1.25 V when V_{In} = 0 V?

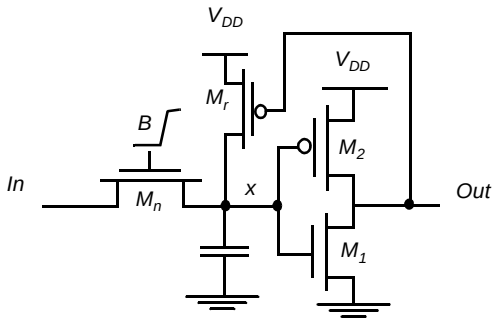
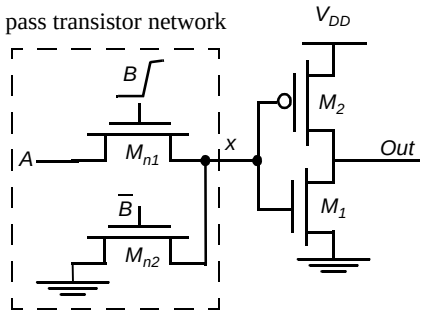


Figure 6.11 Level restorer.

18. Pass Transistor Logic



V_{DD} = 2.5V
$(W/L)_2$ = 1.5um/0.25um
$(W/L)_1$ = 0.5um/0.25um
$(W/L)_{ni}$ = 0.5um/0.25um

k_n' = 115uA/V^2, kp' = -30uA/V^2
V_{tN} = 0.43V, V_{tP} = -0.4V

Figure 6.12 Level restoring circuit.

Consider the circuit of Figure 6.12. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

a. What is the logic function performed by this circuit?

b. Explain why this circuit has non-zero static dissipation.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d. Implement the same circuit using transmission gates.

e. Replace the pass-transistor network in Figure 6.12 with a pass transistor network that computes the following function: $x = ABC$ at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

19. [M, None, 4.3] Sketch the waveforms at *x*, *y*, and *z* for the given inputs (Figure 6.13). You may approximate the time scale, but be sure to compute the voltage levels. Assume that V_T = 0.5 V when body effect is a factor.

20. [E, None, 4.3] Consider the circuit of Figure 6.14.

a. Give the logic function of *x* and *y* in terms of *A*, *B*, and *C*. Sketch the waveforms at *x* and *y* for the given inputs. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain.

b. Redesign the gates using *np*-CMOS to eliminate any race conditions. Sketch the waveforms at *x* and *y* for your new circuit.

21. [M, None, 4.3] Suppose we wish to implement the two logic functions given by $F = A + B + C$ and $G = A + B + C + D$. Assume both true and complementary signals are available.

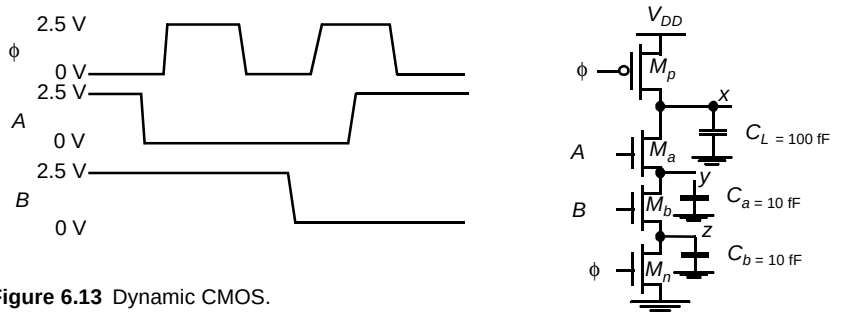


Figure 6.13 Dynamic CMOS.

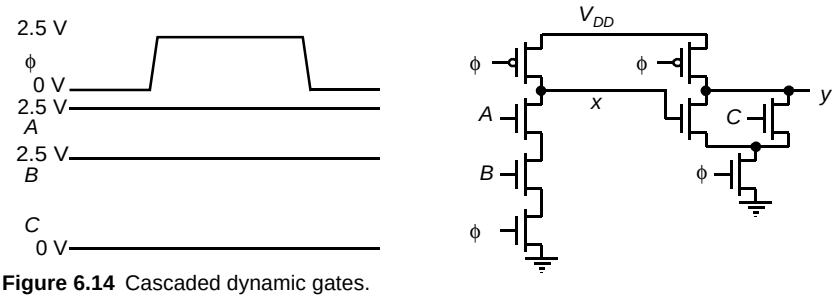


Figure 6.14 Cascaded dynamic gates.

a. Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.

b. Design an *np*-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part (a)?

22. Consider a conventional 4-stage Domino logic circuit as shown in Figure 6.15 in which all precharge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times).

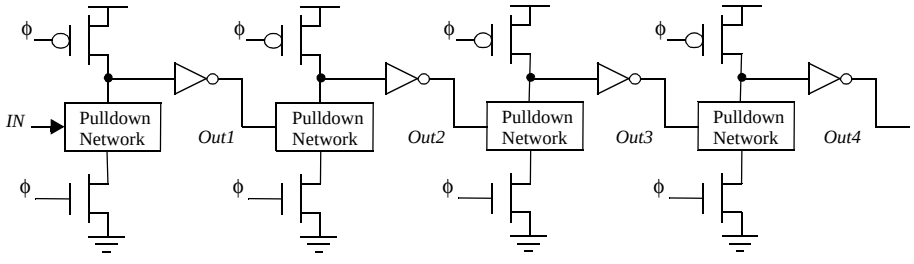


Figure 6.15 Conventional DOMINO Dynamic Logic.

a. Complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units.

b. Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

c. Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the precharge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

23. [C, Spice, 4.3] Figure 6.16 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a. What Boolean functions are implemented at outputs *F* and *G*? If *A* and *B* are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output *G*?

b. Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case..

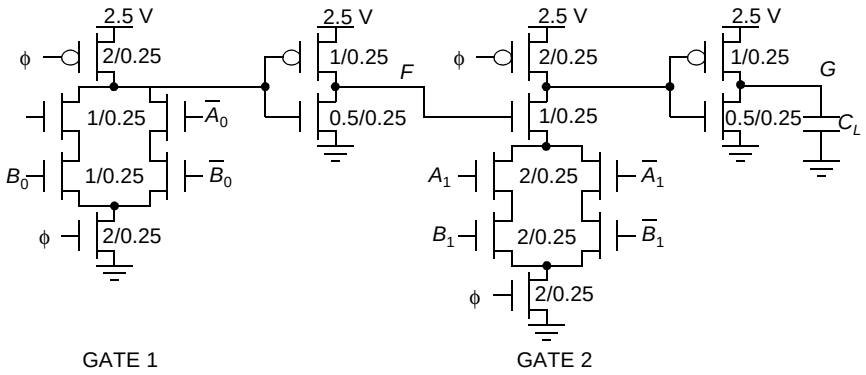


Figure 6.16 DOMINO logic circuit.

24. [M, Spice, 4.3] In this problem you will consider methods for eliminating charge sharing in the circuit of Figure 6.16. You will then determine the performance of the resulting circuit.

a. In problem 24 you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock ϕ and its source connected to V_{DD}) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

b. For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit.

Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

c. Using SPICE on the new circuit and applying the sequence of inputs found in part (b), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (*A*, *B* and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

25. [C, None, 4.2–3] For this problem, refer to the layout of Figure 6.17.

a. Draw the schematic corresponding to the layout. Include transistor sizes.

b. What logic function does the circuit implement? To which logic family does the circuit belong?

c. Does the circuit have any advantages over fully complementary CMOS?

d. Calculate the worst-case V_{OL} and V_{OH}.

e. Write the expresions for the area and perimeter of the drain and source for all of the FETs in terms of λ. Assume that the capacitance of shared diffuusions divides evenly between the sharing devices. Copy the layout into Magic, extract and simulate to find the worst-case t_{pHL} time. For what input transition(s) does this occur? Name all of the parasitic capacitances that you would need to know to calculate this delay by hand (you do not need to perform the calculation).

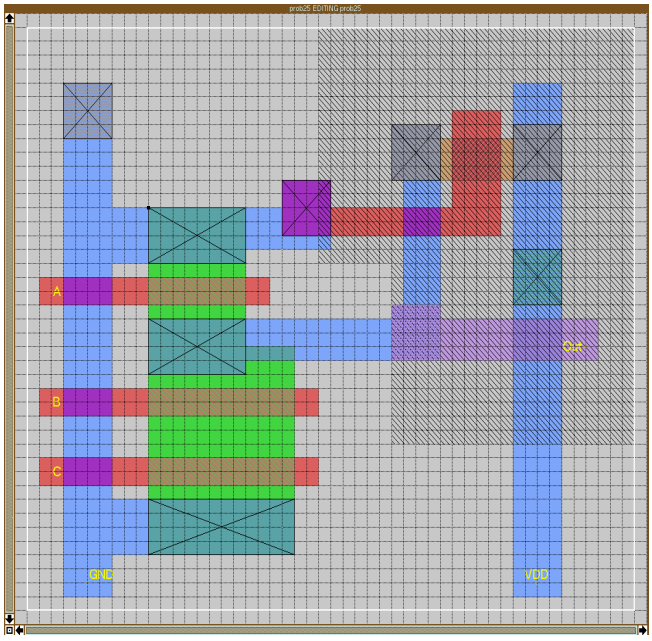


Figure 6.17 Layout of complex gate.

26. [E, None, 4.4] Derive the truth table, state transition graph, and output transition probabilities for a three-input XOR gate with independent, identically distributed, uniform white-noise inputs.

27. [C, None, 4.4] Figure 6.18 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.

a. Does this schematic contain reconvergent fan-out? Explain your answer.

b. Find the exact signal (P_1) and transition ($P_{0\rightarrow 1}$) formulas for nodes *X*, *Y*, and *Z* for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.

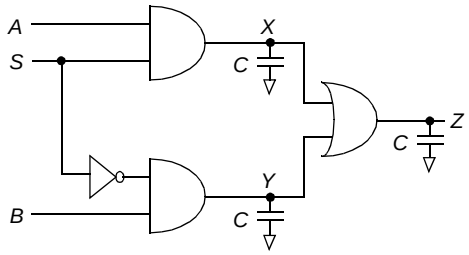


Figure 6.18 Two-input multiplexer

28. [M, None, 4.4] Compute the switching power consumed by the multiplexer of Figure 6.18, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where C = 0.3 pF. Assume that V_{DD} = 2.5 V and independent, identically-distributed uniform white noise inputs, with events occuring at a frequency of 100 MHz. Perform this calculation for the following:

a. A static, fully-complementary CMOS implementation

b. A dynamic CMOS implementation

29. Consider the circuit shown Figure 6.19.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5µm/0.25µm.

b. Let the drain current for each device (NMOS and PMOS) be 1µA for NMOS at V_{GS}= V_T and PMOS at V_{SG}= V_T. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL**.**

c. Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A\ =1)}$ = 0.5, $Pr_{(B=1)}$ = 0.5, $Pr_{(C=1)}$ = 0.5) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power?

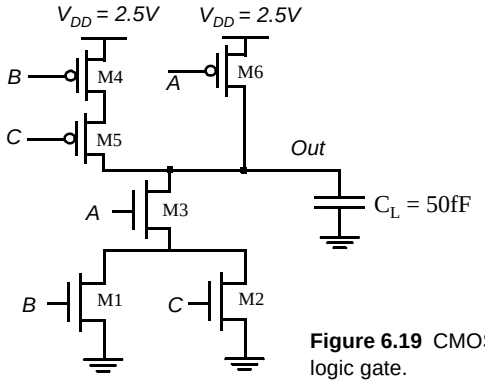


Figure 6.19 CMOS logic gate.

DESIGN PROJECT

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of $A \times t_p^2$, the product of the area of your design and the square of the delay for the worst-case transition.

Chapter 7
PROBLEMS

1. [M, None, 7.4] Figure 1 shows a practical implementation of a pulse register. Clock *Clk* is ideal with 50% duty cycle.

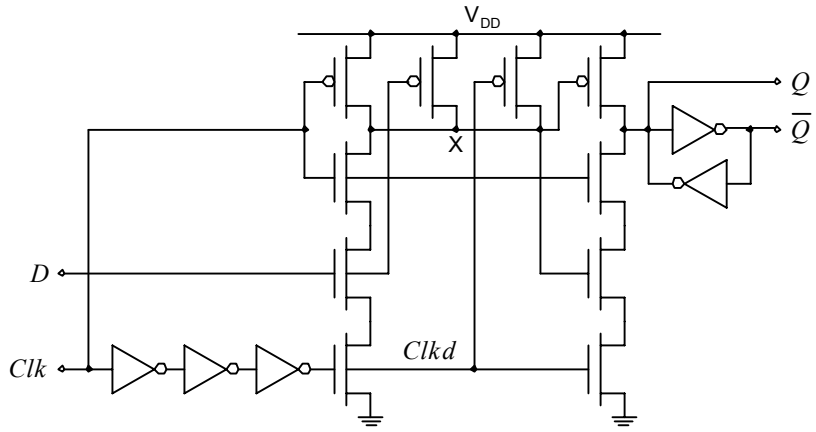


Figure 0.1 Pulse register.

Data : V_{DD} = 2.5V, $t_{p,inv}$ = 200ps, node capacitances are C_{Clkd} = 10fF, C_x = 10fF, both true and complementary outputs node capacitances are 20fF.

a. Draw the waveforms at nodes *Clk*, *Clkd*, *X* and *Q* for two clock cycles, with $D = 0$ in one cycle and $D = 1$ in the other.

b. What is the approximate value of setup and hold times for this circuit?

c. c)If the probability that *D* will change its logic value in one clock cycle is α, with equal probability of being 0 or 1, what is the power consumption of this circuit? (exclude the power consumption in the clock line) f_{clk} = 100 MHz.

2. [M, None, 7.4] Figure 2 shows a register that attempts to statistically reduce power consumption using a data-transition look-ahead technique.

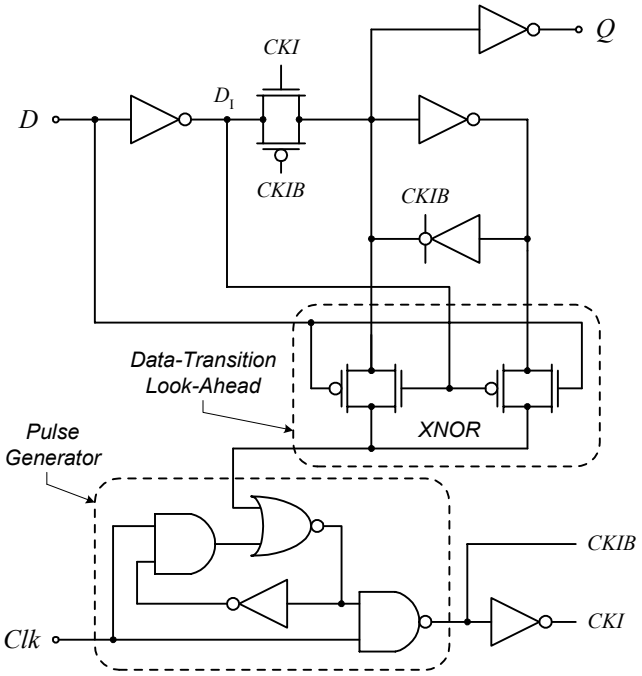


Figure 0.2 Pulse register.

a. Briefly describe the operation of the circuit.

b. If all the NMOS transistors are of the same size, and all of the PMOS transistors are of the same size, two times wider than the NMOS, roughly determine the input switching probability under which this flip-flop reduces power, compared to an equivalent flip-flop without data-transition look-ahead circuitry.

3. [E, None, 7.6] Shown in Figure 3 is a novel design of a Schmitt trigger. Determine the W/L ratio of transistor M_1 such that $V_{M+} = 3V_{Tn}$. $V_{DD} = 2.5\text{V}$. The W/L ratios of other transistors are shown in figure. You may ignore the body effect in this question. The other transistor parameters are as given in Chapter 3.

NMOS: $V_{Tn} = 0.4\text{V}$, $k_n' = 115\mu\text{A/V}^2$, $V_{DSAT} = 0.6\text{V}$, $\lambda = 0$, $\gamma = 0\text{V}^{1/2}$

PMOS: V_{Tp} = -0.4V, k_p' = -30μA/V^2, V_{DSAT} = -1V, λ = 0, γ = -0V$^{1/2}$

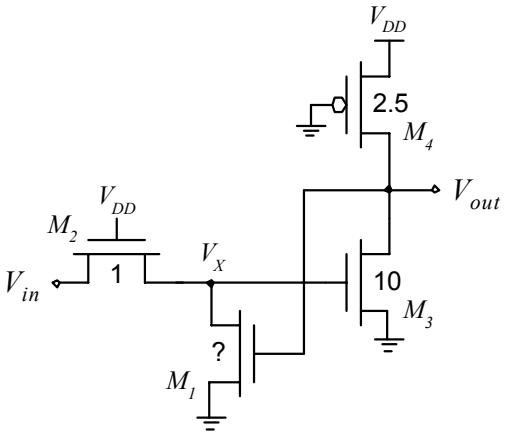


Figure 0.3 Schmitt trigger.

4. [M, None, 7.6] Consider the circuit in Figure 4. The inverter is ideal, with V_M=V_{DD}/2 and infinite slope. The transistors have $V_{T\_}$=0.4V, k_n'=120 μA/V^2 and k_p= 40 μA/V^2. M_1 has $(W/L)_1$=1. Ignore all other parasitic effects in the transistors.

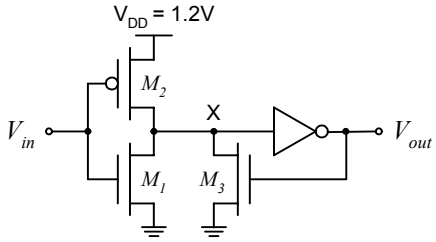


Figure 0.4 Schmitt trigger.

a. As V_{IN} goes from 0 to V_{DD} and back to 0 explain the sequence of events which makes this circuit operate as a Schmitt Trigger.

b. Find the value of $(W/L)_2$ such that when V_{IN} increases from 0 to V_{DD} the output will switch at V_{in} = 0.8V.

c. Find the value of $(W/L)_3$ such that when V_{in} decreases from V_{DD} to 0 the output will switch at V_{in} = 0.4V. If you don't trust your value from b., you may use $(W/L)_2$=5.

5. [M, None, 7.6] Figure 5 shows an astable multivibrator. Calculate and draw voltage waveforms at the capacitor V_C and at the output V_{out}. What is the oscillation frequency of the multivibrator?

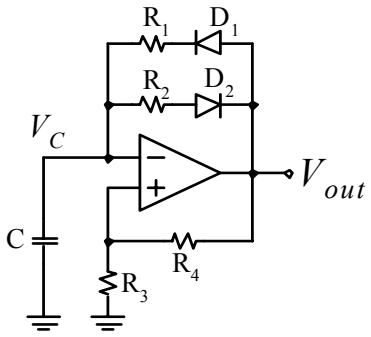


Figure 0.5 Astable multivibrator.

Assume that the amplifier is ideal, with symmetric supplies ($V_{out}^{max} = V_{DD}$, $V_{out}^{min} = -V_{SS}$) $R_1 = 1k\Omega$, $R_2 = 3k\Omega$, $R_3 = R_4 = 4k\Omega$, C = 1nF, $V_{DD} = -V_{SS} == 5V$, diode voltage $V_D = 0.6V$ (ideal diode), $V_{out}(t = 0^-) = -V_{SS}$.

6. [E, None, 7.6] An oscillator is shown in Figure 6. Draw the signal waveforms for this circuit at nodes X, Y, Z, A, and B. Determine the oscillation frequency. You may assume that the delay of the inverters, the resistances of the MOS transistors, and all internal capacitors can be ignored. The inverter switch point is set at 1.25V. Assume that nodes Y and Z are initially at 0V and 2.5V, respectively.

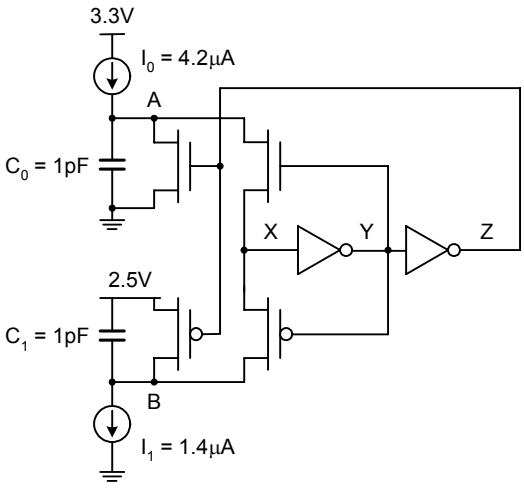


Figure 0.6 Oscillator.

7. [E, None, 7.6] Consider the oscillator in Figure 7. Assume that the "n" switches turn "on" for voltages above $V_{DD}/2$, and the "p" switches turn "on" for voltages below $V_{DD}/2$. Assume that the current sources stop when the node voltage charges to either V_{DD} or ground.

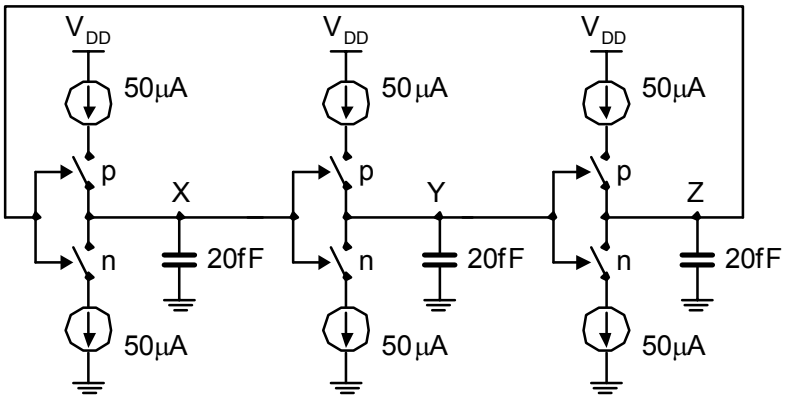


Figure 0.7 Oscillator.

a. Find the oscillation period for $V_{DD} = 3V$.

b. Draw the waveforms at nodes X, Y, and Z for two periods.

c. Find the oscillation period.

8. [M, None, 7.6] The circuit in Figure 8 operates at a supply voltage of 3V and uses two Schmitt triggers with the following threshold voltages: $V_{M+} = 2V$, $V_{M-} = 1V$.

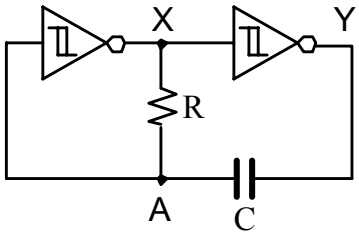


Figure 0.8 A circuit composed of Schmitt triggers.

a. Identify whether the circuit is monostable, bistable, or astable?

b. Draw the waveforms at nodes X, Y, and A. Mark all important voltage levels.

c. Calculate the key timing parameter for this circuit (propagation delay for bistable, pulse width for monostable, and time period for astable) in terms of R and C. You can assume that gate delays are negligible compared to the delay of the RC network.

Chapter 10
PROBLEMS

1. [C, None, 9.2] For the circuit in Figure 0.1, assume a unit delay through the Register and Logic blocks (i.e., $t_R = t_L = 1$). Assume that the registers, which are positive edge-triggered, have a set-up time t_S of 1. The delay through the multiplexer t_M equals 2 t_R.

a. Determine the minimum clock period. Disregard clock skew.

b. Repeat part a, factoring in a nonzero clock skew: $\delta = t'_\theta - t_\theta = 1$.

c. Repeat part a, factoring in a non-zero clock skew: $\delta = t'_\theta - t_\theta = 4$.

d. Derive the maximum positive clock skew that can be tolerated before the circuit fails.

e. Derive the maximum negative clock skew that can be tolerated before the circuit fails.

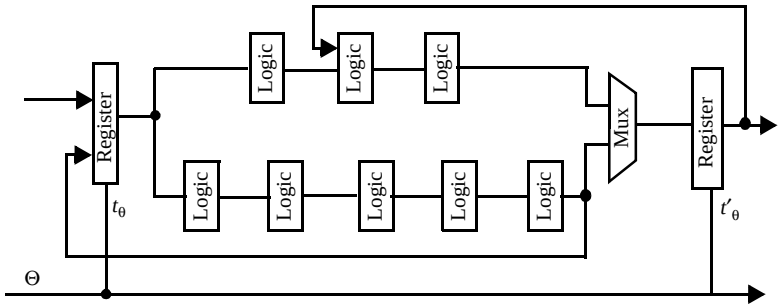


Figure 0.1 Sequential circuit.

2. This problem examines sources of skew and jitter.

a. A balanced clock distribution scheme is shown in Figure 0.2. For each source of variation, identify if it contributes to skew or jitter. Circle your answer in Table 0.1

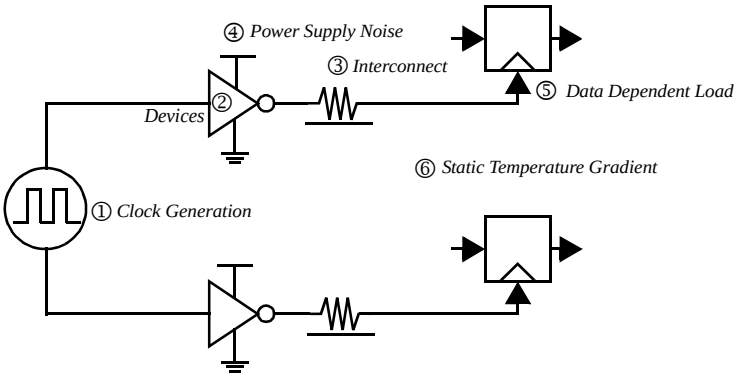


Figure 0.2 Sources of Skew and Jitter in Clock Distribution.

1) Uncertainty in the clock generation circuit	Skew	Jitter
2) Process variation in devices	Skew	Jitter
3) Interconnect variation	Skew	Jitter
4) Power Supply Noise	Skew	Jitter
5) Data Dependent Load Capacitance	Skew	Jitter
6) Static Temperature Gradient	Skew	Jitter

Table 0.1 Sources os Skew and Jitter

b. Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown in Figure 0.3. (i.e., $Enable_1$,..., $Enable_N$ can take on dif-

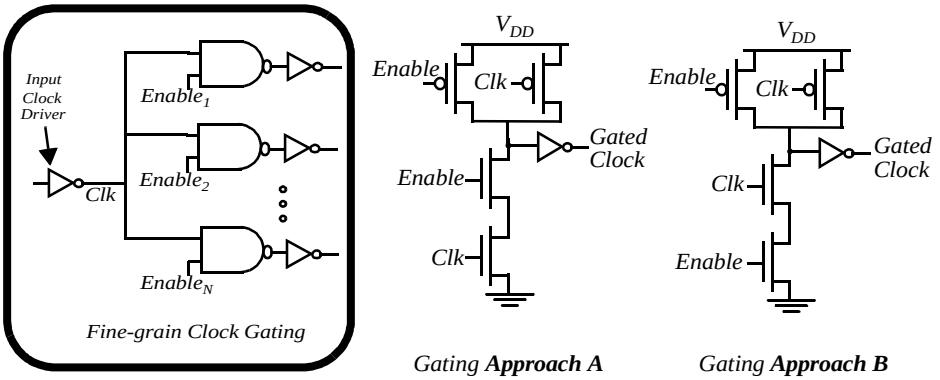


Figure 0.3 Jitter in clock gating

ferent values on a cycle by cycle basis). Which approach (*A* or *B*) results in lower *jitter* at the output of the input clock driver? (hint: consider gate capacitance) Explain.

3. Figure 0.4 shows a latch based pipeline with two combinational logic units.

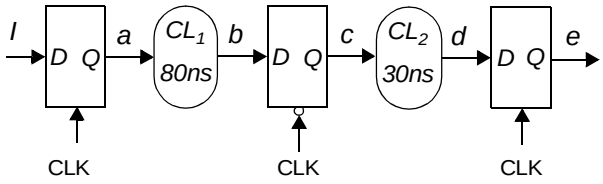


Figure 0.4 Latch Based Pipeline

Recall that the timing diagram of a combinational logic block and a latch can be drawn as follows, where the shaded region represents that the data is not ready yet.

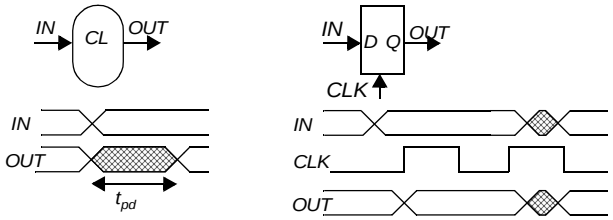


Figure 0.5 Timing diagrams of combinational logic and latch

Assume that the contamination delay t_{cd} of the combinational logic block is zero, and the $t_{clk\text{-}q}$ of the latch is zero too.

a. Assume the following timing for the input *I*. Draw the timing diagram for the signals *a*, *b*, *c*, *d* and *e*. Include the clock in your drawing.

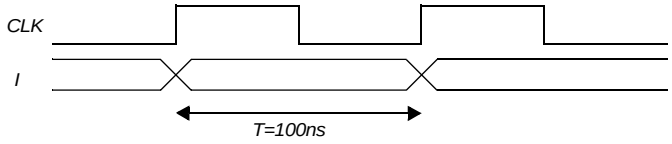


Figure 0.6 Input timing

b. State the deadline for the computation of the signal *b* and *d*, i.e. when is the latest time they can be computed, relative to the clock edges. In your diagram for (a), label with a "< >" the "slack time" that the signals *b* and *d* are ready before the latest time they must be ready.

c. Hence deduce how much the clock period can be reduced for this shortened pipeline. Draw the modified timing diagram for the signals *a*, *b*, *c*, *d*, and *e*. Include the clock in your drawing.

4. Consider the circuit shown in Figure 0.7.

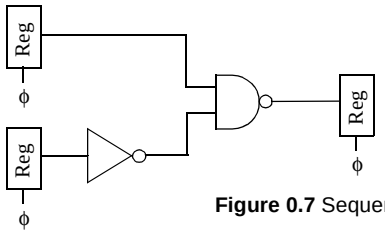


Figure 0.7 Sequential Circuit

a. Use SPICE to measure t_{max} and t_{min}. Use a minimum-size NAND gate and inverter. Assume no skew and a zero rise/fall time. For the registers, use the following:

- A TSPC Register.
- A C^2MOS Register.

b. Introduce clock skew, both positive and negative. How much skew can the circuit tolerate and still function correctly?

c. Introduce finite rise and fall time to the clocks. Show what can occur and describe why.

5. Consider the following latch based pipeline circuit shown in Figure 0.8.

Assume that the input, *IN*, is valid (i.e., set up) 2ns before the falling edge of *CLK* and is held till the falling edge of *CLK* (there is no guarantee on the value of *IN* at other times). Determine the maximum *positive* and *negative* skew on *CLK'* for correct functionality.

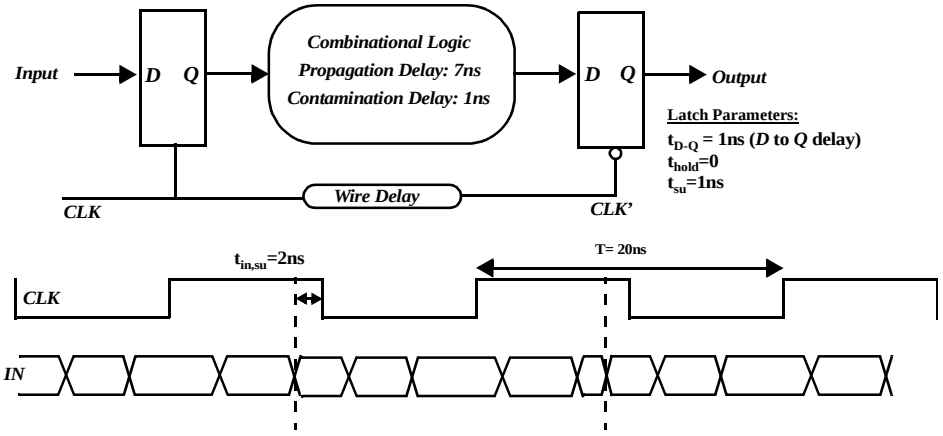


Figure 0.8 Latch based pipeline

6. For the L1-L2 latch based system from Figure 0.9**,** with two overlapping clocks derive all the necessary constraints for proper operation of the logic. The latches have setup times T_{SU1} and T_{SU2}, data-to-output delays $T_{D\text{-}Q1}$ and $T_{D\text{-}Q2}$, clock-to-output delays $T_{Clk\text{-}Q1}$ and $T_{Clk\text{-}Q2}$, and hold times T_{H1} and T_{H2}, respectively. Relevant clock parameters are also illustrated in Figure 0.9. The constraints should relate the logic delays, clock period, overlap time T_{OV}, pulse widths *PW*1 and *PW*2 to latch parameters and skews.

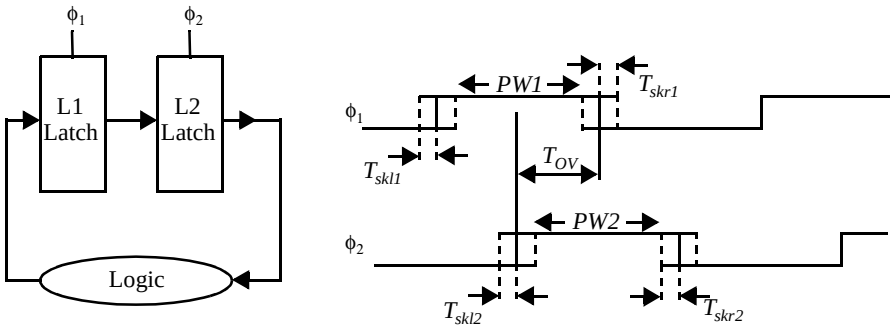


Figure 0.9 Timing constraints

7. For the self-timed circuit shown in Figure 0.10, make the following assumptions. The propagation through the NAND gate can be 5 nsec, 10 nsec, or 20 nsec with equal probability. The logic in the succeeding stages is such that the second stage is always ready for data from the first.

a. Calculate the average propagation delay with t_{hs} = 6 nsec.

b. Calculate the average propagation delay with t_{hs} =12 nsec.

c. If the handshaking circuitry is replaced by a synchronous clock, what is the smallest possible clock frequency?

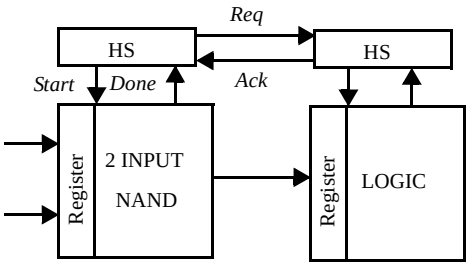


Figure 0.10 Self-timed circuit.

8. Lisa and Marcus Allen have a luxurious symphony hall date. After pulling out of their driveway, they pull up to a four-way stop sign. They pulled up to the sign at the same time as a car on the cross-street. The other car, being on the right, had the right-of-way and proceeded first. On the way they also have to stop at traffic signals. There is so much traffic on the freeway, the metering lights are on. Metering lights regulate the flow of merging traffic by allowing only one lane of traffic to proceed at a time. With all the traffic, they arrive late for the symphony and miss the beginning. The usher does not allow them to enter until after the first movement.

On this trip, Lisa and Marcus proceeded through both synchronizers and arbiters. Please list all and explain your answer.

9. Design a self-timed FIFO. It should be six stages deep and have a two phase handshakin with the outside world. The black-box view of the FIFO is given in Figure 0.11.

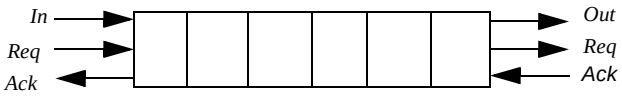


Figure 0.11 Overall structure of FIFO.

10. System Design issues in self-timed logic

One of the benefits of using self-timed logic is that it delivers average-case of performance rather than the worst-case performance that must be assumed when designing synchronous circuits. In some applications where the average and worst cases differ significantly you can have significant improvements in terms of performance. Here we consider the case of ripple carry addition. In a synchronous design the ripple carry adder is assumed to have a worst case performance which means a carry-propagation chain of length N for an N-bit adder. However, as we will prove during the course of this problem the average length of the carry-propagation chain assuming uniformly distributed input values is in fact O(log N)!

a. Given that $p_n(v)$ = Pr(carry-chain of an n-bit addition is ≥ v bits), what is the probability that the carry chain is of length *k* for an *n*-bit addition?

b. Given your answer to part (a), what is the average length of the carry chain (i.e., a_n)? Simplify your answer as much as possible.

Now $p_n(v)$ can be decomposed into two mutually-exclusive events, A and B. Where A represents that a carry chain of length ≥ v occurs in the first *n*-1 bits, and B represents that a carry chain of length *v* ends on the *n*th bit.

c. Derive an expression for Pr(A).

d. Derive an expression for Pr(B). (HINT: a carry bit i is propagated only if $a_i \neq b_i$, and a carry chain begins only if $a_i = b_i = 1$).

e. Combine your results from (c) and (d) to derive an expression for $p_n(v) - p_{n-1}(v)$ and then bound this result from above to yield an expression in terms of only the length of the carry chain (i.e., v).

f. Using what you've shown thus far, derive an upper bound for the expression:

$$\sum_{i=v}^{n} (p_i(v) - p_{i-1}(v))$$

Use this result, coupled with the fact that $p_n(v)$ is a probability (i.e., it's bounded from above by 1), to determine a two-part upper bound for $p_n(v)$.

g. (The magic step!) Bound n by a clever choice of k such that $2^k \leq n \leq 2^{k+1}$ and exploit the fact that $log_2\, x$ is concave down on $(0, \infty)$ to ultimately derive that $a_n \leq log_2\, n$, which concludes your proof!

h. Theoretically speaking, how much faster would a self-timed 64-bit ripple carry adder be than its synchronous counterpart? (You may assume that the overhead costs of using self-timed logic are negligible).

11. Figure 0.12 shows a simple synchronizer. Assume that the asynchronous input switches at a rate of approximately 10 MHz and that t_r = 2 nsec, f_ϕ = 50 MHz, $V_{IH} - V_{IL}$=0.5 V, and V_{DD} = 2.5 V.

a. If all NMOS devices are minimum-size, find $(W/L)p$ required to achieve V_{MS} = 1.25 V. Verify with SPICE.

b. Use SPICE to find τ for the resulting circuit.

c. What waiting time T is required to achieve a MTF of 10 years?

d. Is it possible to achieve an MTF of 1000 years (where $T > T_\phi$)? If so, how?

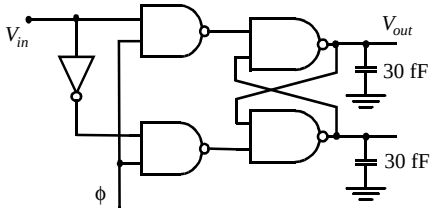


Figure 0.12 Simple synchronizer

12. Explain how the phase-frequency comparator shown in Figure 0.13 works.

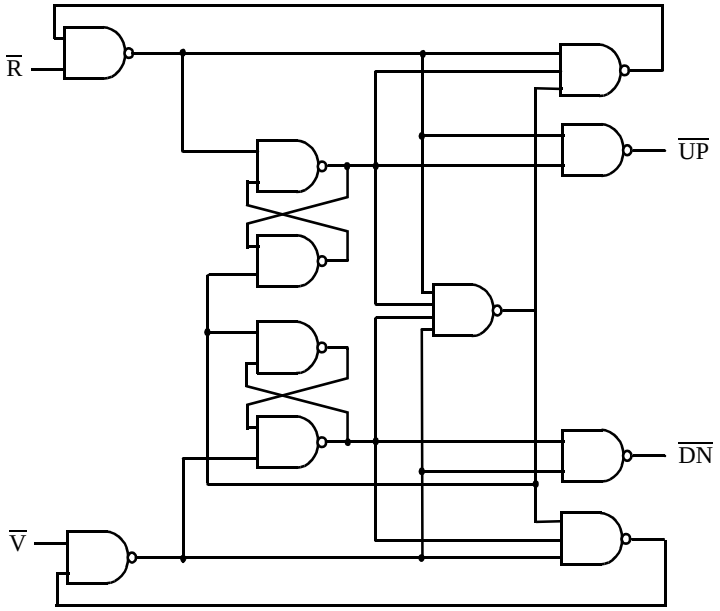


Figure 0.13 Phase-frequency comparator

13. The heart of any static latch is the cross-coupled structure shown in Figure 0.14 (part a).

a. Assuming identical inverters with *Wp/Wn =kn'/kp'*, what is the metastable point of this circuit? Give an expression for the time trajectory of V_Q, assuming a small initial *Vd0* centered around the metastable point of the circuit, V_M**.**

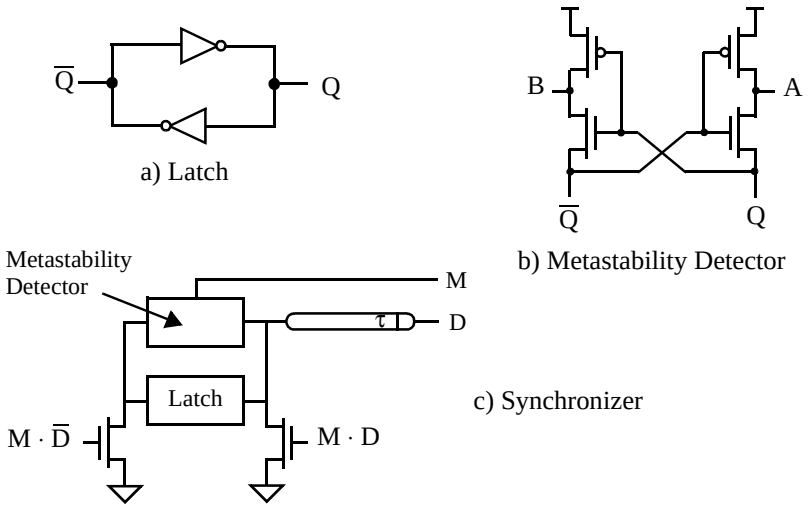


Figure 0.14 Simple synchronizer

b. The circuit in part b has been proposed to detect metastability. How does it work? How would you generate a signal M that is high when the latch is metastable?

c. Consider the circuit of part c. This circuit was designed in an attempt to defeat metastability in a synchronizer. Explain how the circuit works? What ís the function of the delay element?

14. An adjustable duty-cycle clock generator is shown in Figure 0.15. Assume the delay through the delay element matches the delay of the multiplexer.

a. Describe the operation of this circuit

b. What is the range of duty-cycles that can be achieved with this circuit.

c. Using an inverter and an additional multiplexer, show how to make this circuit cover the full range of duty cycles.

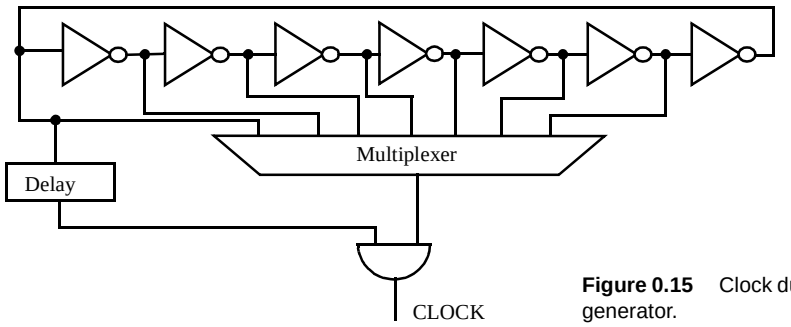


Figure 0.15 Clock duty-cycle generator.

15. The circuit style shown in Figure 0.17.a has been proposed by Acosta et. al. as a new self-timed logic style. This structure is known as a Switched Output Differential Structure[1].

a. Describe the operation of the SODS gate in terms of its behavior during the pre-charge phase, and how a valid completion signal can be generated from its outputs.

b. What are the advantages of using this logic style in comparison to the DCVSL logic style given in the notes?

c. What are the disadvantages of using this style in comparison to DCVSL?

d. Figure 0.16.b shows a 2-input AND gate implemented using a SODS style. Simulate the given circuit using Hspice. Do you notice any problems? Explain the cause of any problems that you may observe and propose a fix. Re-simulate your corrected circuit and verify that you have in fact fixed the problem(s).

[1] A.J. Acosta, M. Valencia, M.J. Bellido, J.L. Huertas, "SODS: A New CMOS Differential-type Structure," *IEEE Journal of Solid State Circuits*, vol. 30, no. 7, July 1995, pp. 835-838

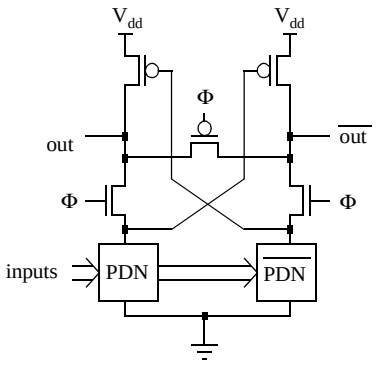


Figure 0.17 a - SODS Logic Style

V_{dd} = 2.5V

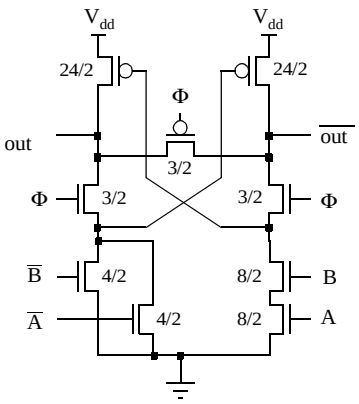


Figure 0.16 b - 2-input And Gate in SODS Style

16. Voltage Control Ring Oscillator.

In this problem, we will explore a voltage controlled-oscillator that is based upon John G. Maneatis' paper in Nov. 1996, entitled "Low Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," appeared in the Journal of Solid-State Circuits. We will focus on a critical component of the PLL design: the voltage-controlled ring oscillator. Figure 0.17 shows the block diagram of a voltage controlled ring oscillator:

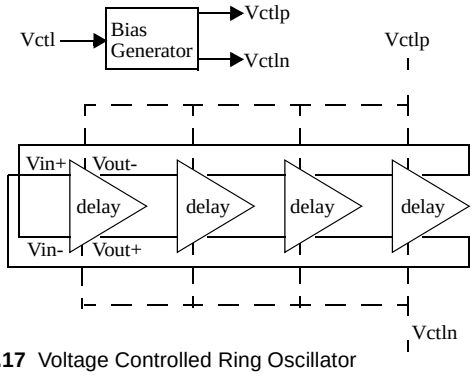


Figure 0.17 Voltage Controlled Ring Oscillator

The control voltage, Vctl, is sent to a bias generator that generates two voltages used to properly bias each delay cell equally, so that equal delay (assuming no process variations) appear across each delay cell. The delay cells are simple, "low-gain" fully differential input and output operational amplifiers that are connected in such a way that oscillations will occur at any one of the outputs with a frequency of 1/(4*delay). Each delay is modeled as an RC time constant; C comes from parasitic capacitances at the output nodes of the delay element,

and R comes from the variable resistor that is the load for the delay cell. Below is a circuit schematic of a typical delay cell.

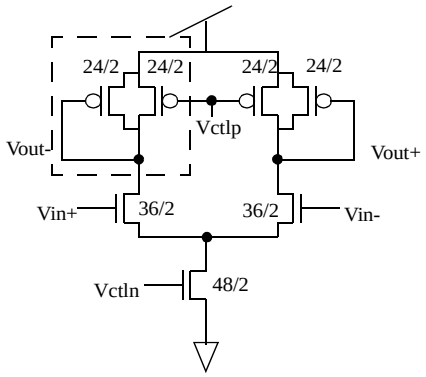


Figure 0.18 One delay Cell

As mentioned before, the value of R is set by a variable resistor. How can one make a variable resistor? The object in the delay cell that is surrounded by a dotted line is called a "symmetric load," and provides the answer to a voltage-controlled variable resistor. R should be linear so that the differential structure cancels power supply noise. We will begin our analysis with the symmetric load.

a. In Hspice, input the circuit below and plot Vres on the X axis and Ires on the Y axis, for the following values of Vctlp: 0.5, 0.75, 1.0, 1.25, 1.5, 1.75, and 2.0 volts, by varying Vtest from Vctlp to Vdd, all on the same graph. For each curve, plot Vres from 0 volts to Vdd-Vctlp. When specifying the Hspice file, be sure to estimate area and perimeter of drains/sources.

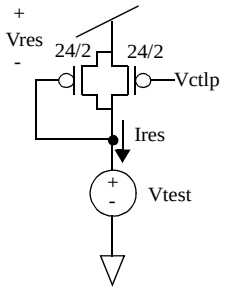


Figure 0.19 :Symmetric Load Test Circuit

After you have plotted the data and printed it out, use a straight edge to connect the end points for each curve. What do you notice about intersection points between the line you drew over each curve, and the curves themselves? Describe any symmetries you see.

b. For each Vctlp curve that you obtained in a), extract the points of symmetries (Vres, Ires), and find the slope of the line around these points of symmetry. These are the effective resistances of the resistors. Also, for each Vctl curve, state the maximum amplitude the output swing can be, without running into asymmetries. Put all of this data in an worksheet format.

c. Using the estimations you made for area and perimeter of drain ad source that you put in your Hspice file, calculate the effective capacitance. (Just multiply area and perimeter by CJ and CJSW from the spice deck). Since we are placing these delay elements in a cas-

caded fashion, remember to INCLUDE THE GATE CAPACITANCE of the following stage. Each delay element is identical to one another. Now, calculate the delay in each cell, according to each setting of Vctlp that you found in a): delay=0.69*R*C. Then, write a general equation, in terms of R and C, for the frequency value that will appear at each delay output. Why is it necessary to cross the feedback lines for the ring oscillator in the first figure? Finally, draw a timing/transient analysis of each output node of the delay lines. How many phases of the base frequency are there?

d. Now, we will look at the bias generator. The circuit for the bias generator is as follows:

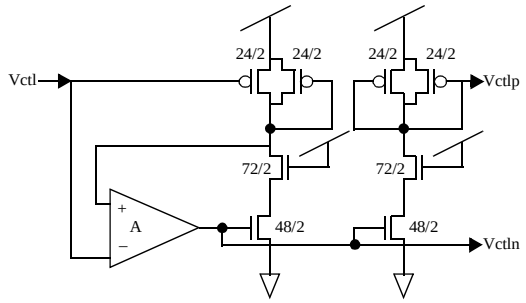


Figure 0.20 :Bias Generator

Implement this circuit in Hspice, and use the ideal voltage controlled voltage source for your amplifier. Use a value of 20 for A. This circuit automatically sets the Vctln and Vctlp voltages to the buffer delays to set the DC operating points of the delay cells such that the symmetric load is swinging reflected around its point of symmetry for a given Vctl voltage. Also, it is important to note that Vctl is the same as Vctlp. It must go through this business to obtain Vctln (which sets the bias current to the correct value, which sets the DC operating point of the buffer). Do a transient run in Hspice to verify that Vctlp is indeed very close to Vctl over a range of inputs for Vctl. Show a Spice transient simulation that goes for 1uS, and switches Vctl in a pwl waveform across a range of inputs between 0.5V and 2.0V. For extra points, explain how this circuit works.

e. Now, hook up the bias generator you just built with 4 delay cells, as shown in the first figure. For each control voltageVctlp from part c), verify your hand calculations with spice simulations. Show a spreadsheet of obtained frequencies vs. hand-calculation predictions, and in a separate column, calculate % error. Give a brief analysis of what you see. Print out all of the phases (4) of the clock, for a Vctl value of your choice.

Chapter 11
PROBLEMS

1. [E, None, 11.6] For this problem you are given a cell library consisting of full adders and two-input Boolean logic gates (i.e. AND, OR, INVERT, etc.).

a. Design an N-bit two's complement subtracter using a minimal number of Boolean logic gates. The result of this process should be a diagram in the spirit of Figure 11.5 . Specify the value of any required additional signals (e.g., C_{in}).

b. Express the delay of your design as a function of N, t_{carry}, t_{sum}, and the Boolean gate delays (t_{and}, t_{or}, t_{inv}, etc.).

2. [M, None, 11.6] A magnitude comparator for unsigned numbers can be constructed using full adders and Boolean logic gates as building blocks. For this problem you are given a cell library consisting of full adders and arbitrary fan-in logic gates (i.e., AND, OR, INVERTER, etc.).

a. Design an N-bit magnitude comparator with outputs $A \geq B$ and $A = B$ using a minimal number of Boolean logic gates. The result of this process should be a diagram in the spirit of Figure 11.5. Specify the value of any required control signals (e.g., C_{in}).

b. Express the delay of your design in computing the two outputs as a function of N, t_{carry}, t_{sum}, and the Boolean gate delays (t_{and}, t_{or}, t_{inv}, etc.).3.

3. [E, None, 11.6] Show how the arithmetic module in Figure 0.1 can be used as a comparator. Derive an expression for its propagation delay as a function of the number of bits.

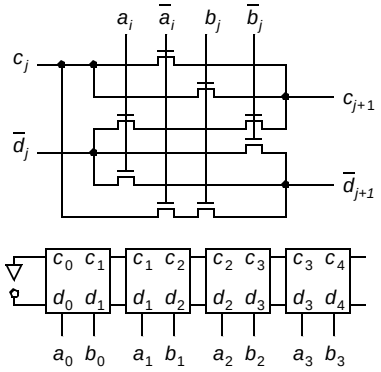


Figure 0.1 Arithmetic module.

4. [E, None, 11.6] The circuit of Figure 11.2 implements a 1-bit datapath function in dynamic (precharge/evaluate) logic.

a. Write down the Boolean expressions for outputs F and G. On which clock phases are outputs F and G valid?

b. To what datapath function could this unit be most directly applied (e.g., addition, subtraction, comparison, shifting)?

5. [M, None, 11.3] Consider the dynamic logic circuit of Figure 0.2 .

a. What is the purpose of transistor M_1? Is there another way to achieve the same effect, but with reducing capacitive loading on the clock Φ?

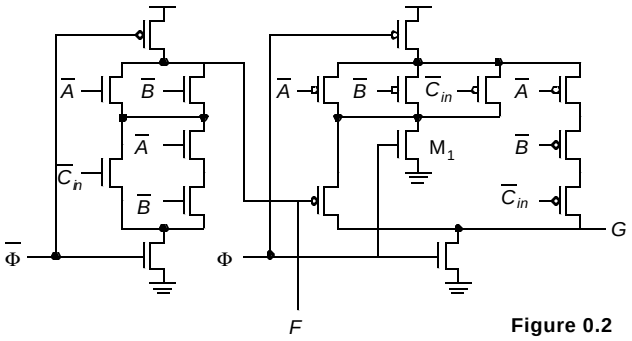


Figure 0.2 Datapath module bit-slice.

b. How can the evaluation phase of *F* be sped up by rearranging transistors? No transistors should be added, deleted, or resized.

c. Can the evaluation of *G* be sped up in the same manner? Why or why not?

6. [M, SPICE, 11.3] The adder circuit of Figure 0.3 makes extensive use of the transmission gate XOR. V_{DD} = 2.5 V.

a. Explain how this gate operates. Derive the logic expression for the various circuit nodes. Why is this a good adder circuit?

b. Derive a first-order approximation of the capacitance on the C_o-node in equivalent gate-capacitances. Assume that gate and diffusion capacitances are approximately identical. Compare your result with the circuit of Figure 11-6 .

c. Assume that all transistors with the exception of those on the carry path are minimum-size. Use 4/0.25 NMOS and 8/0.25 PMOS devices on the carry-path. Using SPICE simulation, derive a value for all important delays (input-to-carry, carry-to-carry, carry-to-sum).

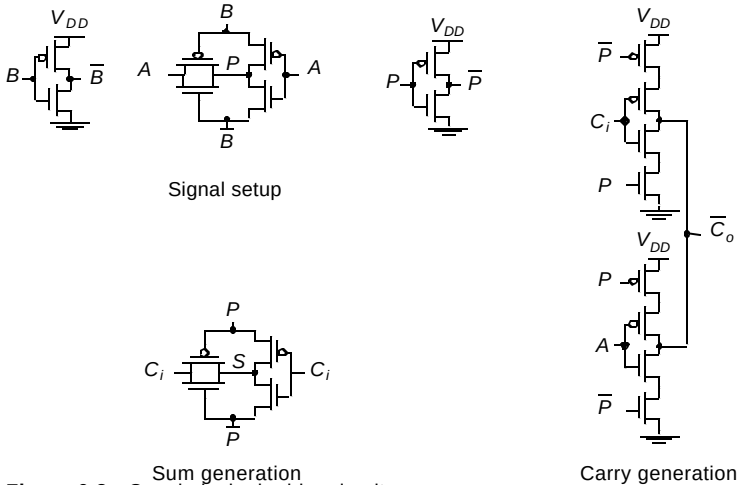


Figure 0.3 Quasi-clocked adder circuit.

7. [M, None, 11.3] The dynamic implementation of the 4-bit carry-lookahead circuitry from Fig. 11-21 can significantly reduce the required transistor count.

a. Design a domino-logic implementation of Eq. 11.17 . Compare the transistor counts of the two implementations.

b. What is the worst-case propagation delay path through this new circuit?

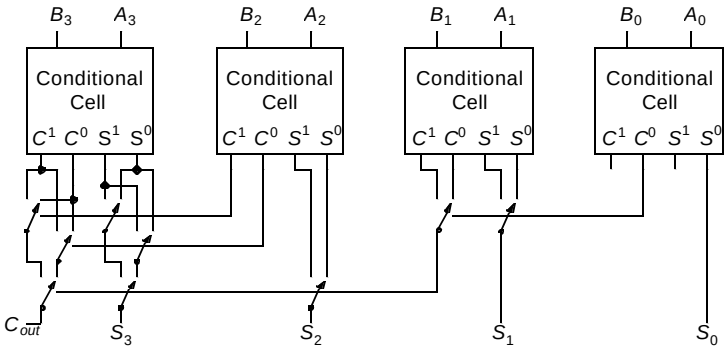
c. Are there any charge-sharing problems associated with your design? If so, modify your design to alleviate these effects.

8. [C, None, 11.3] Figure 0.4 shows a popular adder structure called the conditional-sum adder. Figure 0.4.a shows a four-bit instance of the adder, while 0.4.b gives the schematics of the basic adder cell. Notice that only pass-transistors are used in this implementation.

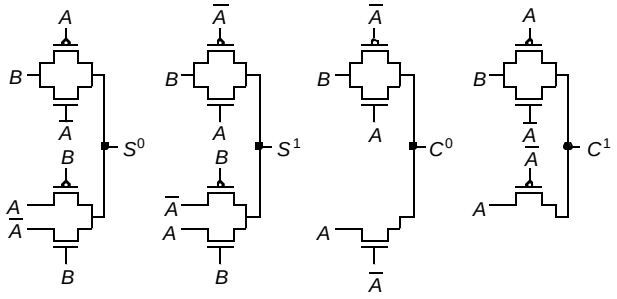
a. Derive Boolean descriptions for the four outputs of the one-bit conditional adder cell.

b. Based on the results of describe how the schematic of 0.4.a results in an addition.

c. Derive an expression for the propagation delay of the adder as a function of the number of bits *N*. You may assume that a switch has a constant resistance R_{on} when active and that each switch is identical in size.



(a) Four-bit conditional-sum adder



(b) Conditional adder cell

Figure 0.4 Conditional-sum adder.

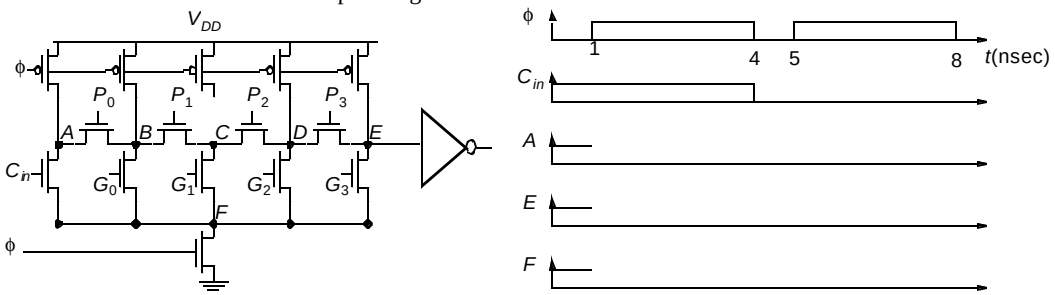
9. [M, None, 11.3] Consider replacing all of the NMOS evaluate transistors in a dynamic Manchester carry chain with a single common pull-down as shown in Fgure 0.5.a. Assume that each NMOS transistor has $(W/L)_N$ = 0.5/0.25 and each PMOS has $(W/L)_P$ = 0.75/0.25. Further assume that parasitic capacitances can be modeled by a 10 fF capacitor on each of the

internal nodes: *A*, *B*, *C*, *D*, *E*, and *F*. Assume all transistors can be modeled as linear resistors with an on-resistance, R_{on} = 5 kΩ.

a. Does this variation perform the same function as the original Manchester carry chain? Explain why or why not.

b. Assuming that all inputs are allowed only a single zero-to-one transition during evaluation, will this design involve charge-sharing difficulties? Justify your answer.

c. Complete the waveforms in Figure 0.5b for $P_0 = P_1 = P_2 = P_3 = 2.5$ V and $G_0 = G_1 = G_2 = G_3 = 0$ V. Compute and indicate t_{pHL} values for nodes *A*, *E*, and *F*. Compute and indicate when the 90% precharge levels are obtained.



(a) Circuit schematic (b) Partial waveforms

Figure 0.5 Alternative dynamic Manchester carry-chain adder.

10. [M, None, 11.3] Consider the two implementations of Manchester carry gates in Figure 11-8.

a. Compare the delay per segment of the two implementations

b. Compare the layout complexities of the two gates using stick diagrams.

c. In the precharged Manchester carry chain using the gate from b. find the probability that the carry signal is propagated from the 15^{th} to the 16^{th} bit of a 32-bit adder, assuming random inputs.

11. [C, None, 11.3] Consider the Radix-4 and Radix-2 Kogge-Stone adders from Figures 11-22 and 11-27 extended to 64-bits. All gates are implemented in domino and all gates in a stage have the same size. The adders have an overall fanout (electrical effort) of 6.

a. Using logical effort, identify the critical path.

b. Size the gates for minimum delay (hint: don't forget to factor in branching). Which adder is faster?

c. Let's now consider sparse versions of each of the above trees. In a tree with a sparseness of 2, only every other carry is computed and it is used to select 2 sums. Similarly, a tree with a sparseness of 4 computes every fourth carry - and that carry signal is used to select 4 sums. Repeat a. and b. for Radix-2 and Radix-4 trees with sparseness of 2 and 4 and compare their speed. Which adder is fastest?

d. Compare the switching power of all adders analyzed in this problem.

12. [C, None, 11.3] In this problem we will analyze a carry-lookahead adder proposed by H. Ling more than 20 years ago, but still among the fastest adders available. In a conventional adder, in order to add two numbers

$$A = a_{n-1}2^{n-1} + a_{n-2}2^{n-2} + ... + a_0 2^0$$
$$B = b_{n-1}2^{n-1} + b_{n-2}2^{n-2} + ... + b_0 2^0$$

we first compute the local carry generate and propagate terms:

$g_i = a_i b_i$

$p_i = a_i + b_i$

then, with a ripple or a tree circuit we form the global carry-out terms resulting from the recurrence relation:

$G_i = g_i + p_i G_{i-1}$

Finally, we form the sum of A and B using local expressions:

$S_i = p_i \oplus G_{i-1}$

In the conventional adder, the terms G_i have, as described, a physical significance. However, an arbitrary function could be propagated, as long as sum terms could be derived. Ling's approach is to replace G_i with:

$H_i = G_i + G_{i-1}$

i.e. H_i is true if "something happens at bit i" - there is a carry out or a carry in. H_i is so-called "Ling's pseudo-carry".

a. Show that:

$H_i = g_i + t_{i-1} H_{i-1}$

where $p_i = a_i + b_i$ (it was Ling's idea to change the notation).

b. Find a formula for computing the sum out of the operands and Ling's pseudo-carry.

c. Unroll the recursions for G_i and H_i for $i = 3$. You should get the expressions fpr G_3 and H_3 as a function of the bits of input operands. Simplify the expressions as much as possible.

d. Implement the two functions using n-type dynamic gates. Draw the two gates and size the transistors. Which one helps us build a faster adder? Explain your answer.

13. [M, None, 11.4] An array multiplier consists of rows of adders, each producing partial sums that are subsequently fed to the next adder row. In this problem, we consider the effects of pipelining such a multiplier by inserting registers between the adder rows.

a. Redraw Figure 11-31 by inserting word-level pipeline registers as required to achieve maximal benefit to throughput for the 4x4 multiplier. Hint: you must use additional registers to keep the input bits synchronized to the appropriate partial sums.

b. Repeat for a carry-save, as opposed to ripple-carry, architecture.

c. For each of the two multiplier architectures, compare the critical path, throughput, and latency of the pipelined and nonpipelined versions.

d. Which architecture is better suited to pipelining, and how does the choice of a vector-merging adder affect this decision?

14. [M, None, 11.4] Estimate the delay of a 16x16 Wallace tree multiplier with the final adder implemented using a Radix-4 tree. One FA has a delay of t_p, a HA $2/3 * t_p$ and a CLA stage $\frac{1}{2} * t_p$.

15. [E, None, 11.5] The layout of shifters is dominated by the number of wires running through a cell. For both the barrel shifter and the logarithmic shifter, estimate the width of a shifter cell as a function of the maximum shift-width M and the metal pitch p.

16. [E, None, 11.7] Consider the circuit from Figure 0.7 . Modules A and B have a delay of 10 ns and 32 ns at 2.5V, and switch 15 pF and 56 pF respectively. The register has a delay of 2 ns and switches 0.1 pF. Adding a pipeline register allows for reduction of the supply voltage while maintaining throughput. How much power can be saved this way? Delay with respect to V_{DD} can be approximated from Figure 11-57.

17. [E, None, 11.7] Repeat Problem 16, using parallelism instead of pipelining. Assume that a 2-to-1 multiplexer has a delay of 4 ns at 2.5 V and switches 0.3 pF. Try parallelism levels of 2 and by 4. Which one is preferred?

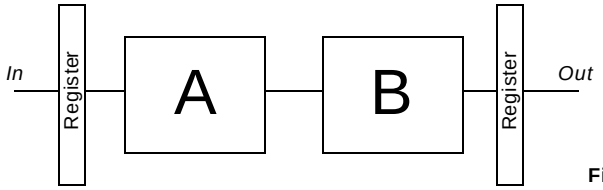


Figure 0.6 Pipelined datapath.

DESIGN PROBLEM

Using the 0.25 µm CMOS technology, design a static 32-bit adder, with the following constraints:

1. input capacitance on each bit is limited to not more than 50fF.
2. each bit is loaded with 100fF.

Use a carry lookahead tree of your choice for implementation. The goal is to achieve the shortest propagation delay.

Determine the logic design of the adder and W and L of all transistors. Initially size the design using the method of logical effort. Estimate the capacitance of carry signal wires based on the floorplan. Verify and optimize the design using SPICE. Compute also the energy consumed per transition. If you have a layout editor available, perform the physical design, extract the real circuit parameters, and compare the simulated results with the ones obtained earlier. For implementation use the 144λ-bit-slice pitch, that corresponds to 36 metal-1 tracks. Use metal 1 for cell-level power distrbution and intra-cell routing, metal-2 for short interconnect and metal-3 and metal-4 for long carries.