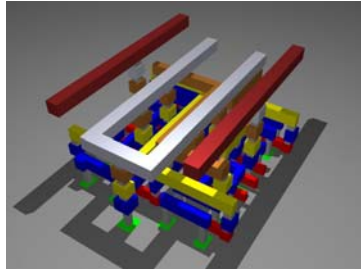


MODULE 6



SEQUENTIAL ELEMENTS

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6 sequential 1

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§ 7.5 Will be discussed with module 08 timing design

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Sequential Elements - Outline

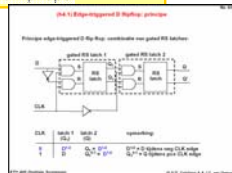
- **Background**
 - Timing, terminology, classification
- **Static Flipflops**
 - Latches
 - Registers
- **Dynamic Flipflops**
 - Latches
 - Registers
- **Non-bistable elements**
 - Schmitt Trigger

■ Much of this material has already been covered in CS1 (v Genderen), Lecture 4(?), Katz Section 6.1

■ Here we will add transistor-level implementation, dynamic flipflops



[Sorin Cotofana]

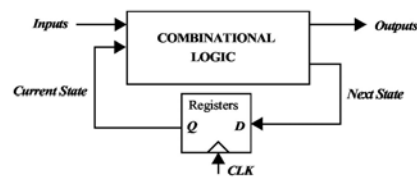


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FSM with Positive Edge Triggered Registers



- Flip-flops provide **memory/state**
- VLSI uses predominantly **D-type flip-flops**

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Memory elements

- Store a **temporary value**, remember a **state**
- Typically controlled by **clock**.
- May have load signal, etc.
- In CMOS, memory is created by:
 - **capacitance** (dynamic);
 - **feedback** (static).
- Also see [http://en.wikipedia.org/wiki/Flip-flop_\(electronics\)](http://en.wikipedia.org/wiki/Flip-flop_(electronics))

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Variations in memory elements

- Form of required clock signal.
- How behavior of data input around clock affects the stored value.
- When the stored value is presented to the output.
- Whether there is ever a combinational path from input to output.

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Timing Metrics Reminder

t_{c-q} : delay from clock (edge) to Q
 t_{su} : setup time
 t_{hold} : hold time
 t_{plogic} : worst case propagation delay of logic
 t_{cd} : best case propagation delay (contamination delay)
 T : clock period

$$T \geq t_{c-q} + t_{plogic} + t_{su}$$

$$t_{cdregister} + t_{cdlogic} \geq t_{hold}$$

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Nomenclature

Beware for confusion

	Katz (CS1)	Rabaey
Latch	Level sensitive storage element	Level sensitive storage element
Register	Group of storage elements	Edge triggered storage element
Flip Flop	Edge triggered storage element	Bistable element using feedback

$CLK = CK = \phi$

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Latches vs. Registers

<p>Latch</p> <div style="border: 1px solid black; padding: 5px;"> <p>Level-sensitive</p> <p>Transparent when clock is active</p> <p>Clock active high: positive latch</p> <p>Clock active low: negative latch</p> <p>Faster, smaller</p> </div>	<p>Register</p> <div style="border: 1px solid black; padding: 5px;"> <p>Edge-triggered</p> <p>Input and output isolated</p> <p>Sampling on 0 → 1 clock: positive edge triggered</p> <p>Sampling on 1 → 0 clock: negative edge triggered</p> <p>Safer</p> </div>
--	--

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Static vs. Dynamic Memory Elements

<p>Static</p> <div style="border: 1px solid black; padding: 5px;"> <p>Operate through positive feedback</p> <p>Preserve state as long as power is on</p> <p>Can work when clock is off</p> <p>More robust</p> </div>	<p>Dynamic</p> <div style="border: 1px solid black; padding: 5px;"> <p>Store charge on (parasitic) capacitor</p> <p>Charge leaks away (in milliseconds)</p> <p>Clock must be kept running (for periodic refresh)</p> <p>Faster, smaller</p> </div>
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Rabaey: bistable elements are called Flip Flops

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Static Latches and Registers

- Latches → can be gated or not
- Registers

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Positive Feedback: Bi-Stability

- Loop-gain in A,B << 1
- A,B: stable points
- Loop-gain in C >> 1
- C: meta-stable point

§ 7.2.1

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SR-Latch

Truth Table 1:

S	R	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	1	0
0	1	0	1
1	1	0	0

← forbidden

Truth Table 2:

S	R	Q	\bar{Q}
1	1	Q	\bar{Q}
0	1	1	0
1	0	0	1
0	0	1	1

← forbidden

§ 7.2.5

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Clocked SR-Latch

Truth Table:

S	R	Q	\bar{Q}
1	1	Q	\bar{Q}
0	1	1	0
1	0	0	1
0	0	1	1

← forbidden

- Katz: gated latch
- Positive latch (active on CK high)
- Naïve implementation
- 16 transistors
- D latch requires 9xN, 9xP
- Larger area, cost, power

Construction of D-latch

- D-latch, D-register most common in VLSI

§ 7.2.2

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CMOS Clocked SR-Latch

$\phi = CK$

- Save 6 (incl. 4 large) PMOS transistors and 2 NMOS
- D-latch requires 7 x N, 3 x P (instead of 9xN, 9xP)

Q: Is this a **ratioed** design or not?
Does it consume static power?

§ 7.2.2

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Multiplexer-Based Latches

Negative Latch

Multiplexer

Restoration

Recirculating latch

§ 7.2.2

Mux-based latches much more common in modern dig. IC's

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Recirculating latch

- Quasi-static, static on one phase
- Feedback restores value
- Requires 4 x N, 4 x P, minimum size (compare 7 x N, 3 x P, non-minimum size)
- ϕ_1 and ϕ_2 inverse but should be non-overlapping
- Can suffer from charge sharing (when ϕ not non-overlapping)
- C_{in} and C_{load} form communicating vessels when Output connected directly to input

§ 7.2.2

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Insensitive for Charge Sharing

- Non ratioed
- High load to CLK

Uni-directionality of this inverter prevents coupling between Q and D

§ 7.2.2

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Recirculating NMOS Latch.

- Degraded 1 at X
- Lower noise margin, higher delay, power

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Latch Designs can Suffer from Race Problems

Signal can race around during $\phi = 1$

§ 7.2.3

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Registers

- Not transparent—use multiple storage elements to isolate output from input.
- Master-slave, edge triggered principle

§ 7.2.3

§ 6.1.4-5

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Master-slave operation

$\phi = 0$:

- master latch is disabled;
- slave latch is enabled, but master latch output is stable,
- so output does not change.

$\phi = 1$:

- master latch is enabled, loading value from input;
- slave latch is disabled, maintaining old output value.

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CMOS Flip-Flop Construction

CMOS technology allows a very different approach to flip-flop design and construction. Instead of using logic gates to connect the clock signal to the master and slave sections of the flip-flop, a CMOS flip-flop uses transmission gates to control the data connections. (See the CMOS gate electronics page for a closer look at the transmission gate structure.)

The result is that a controllable flip-flop can be built with only inverters and transmission gates — a very small and simple structure for an IC.

The basic CMOS D flip-flop is shown below:

www.play-hookey.com

clickable

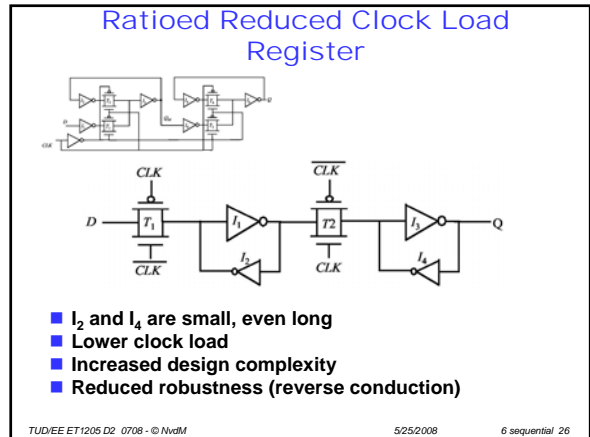
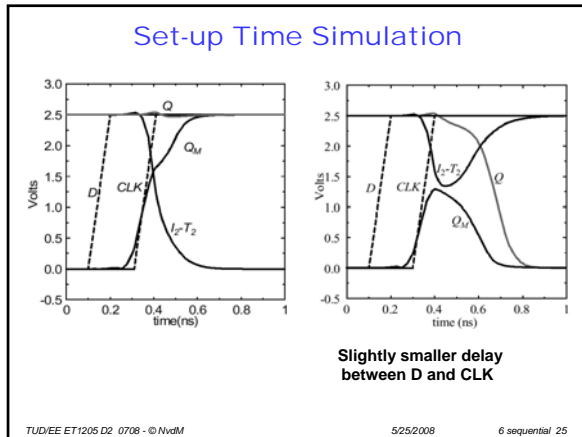
link

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Transistor Level Master Slave Positive Edge Triggered Register

- Robust Design
- Can eliminate I_1 and I_4 , however, they make design more robust (avoid charge sharing, robust input)
- High Clock Load (8 x)

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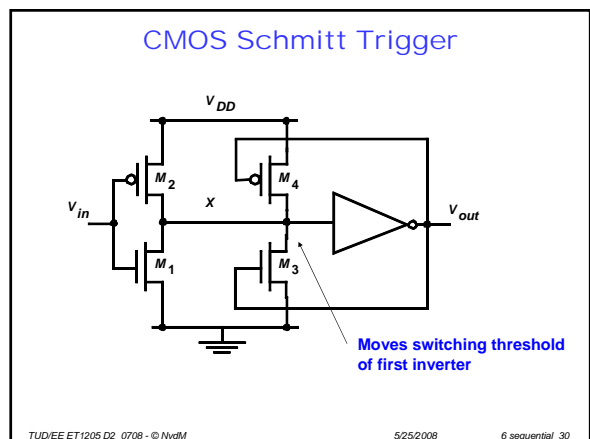
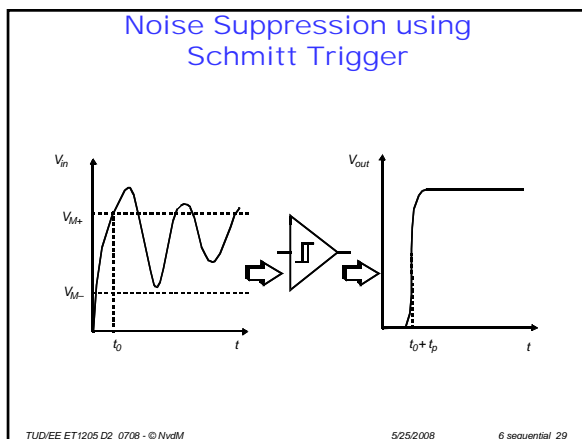
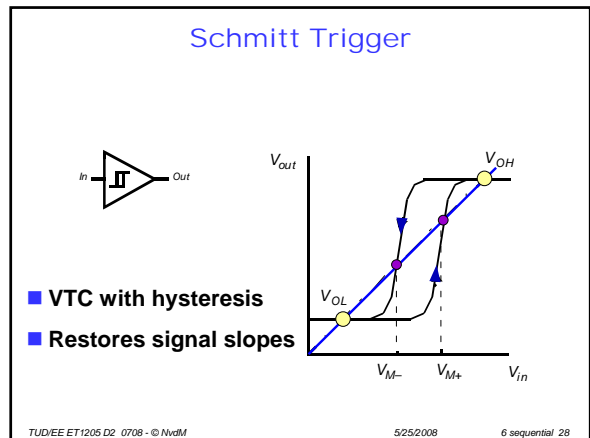


Non-bistable Elements

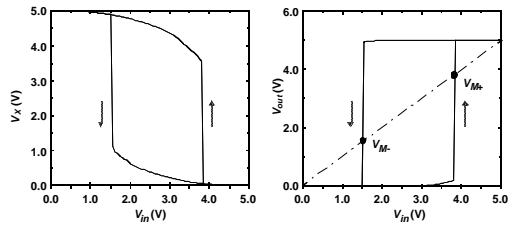
- Schmitt Trigger

Was discussed in P-lab

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Schmitt Trigger Simulated VTC

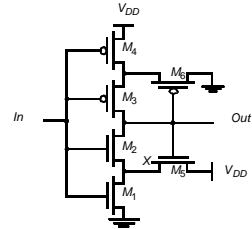


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CMOS Schmitt Trigger (2)



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Summary

- Background
 - Timing, terminology, classification
- Static Flipflops
 - Latches
 - Registers
- Dynamic Flipflops
 - Latches
 - Registers
- Non-bistable elements
 - Schmitt Trigger

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