

Course Material for Interconnect

Chapter 4, 2nd ed.

P = primair, I = Illustratie, O = overslaan

P	4.1	Introduction	136
P	4.2	A First Giance	136 – 138
P	4.3	Interconnect Parameters	138 – e.v.
O		So far we have (onder example 4.2)	147 – 148
O	4.3.3	Inductance	148 – 150
P	4.4	Electrical Wire Models	150 – 156
I	4.4.4	Distributed rc line – <i>hiervoor is vervangende stof</i>	156 – 159 (1)
O	4.4.5	The transmission line	159 – e.v.
O	4.5	Spice wire models	170 – 171
I	4.5.3	Perspective: a look into the future	171 – 174

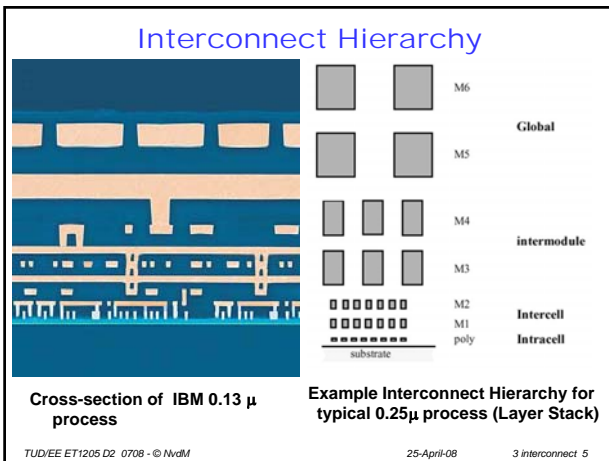
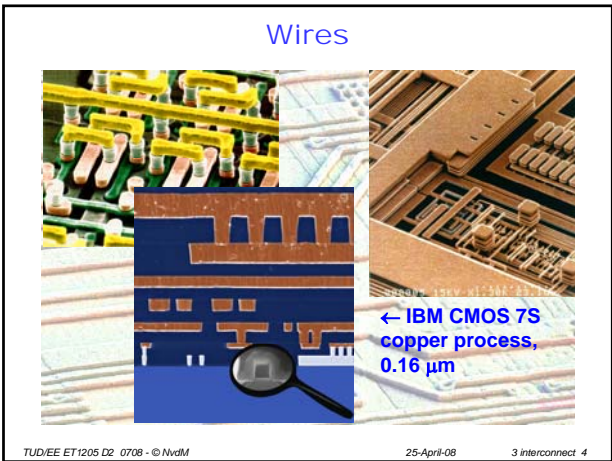
Replacement voor Distributed RC line: Elmore Delay

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Interconnect

- Wires are **not ideal** interconnections
- They may have non-negligible **capacitance, resistance, inductance**
- These are called **wire parasitics**
- Can **dominate** performance of chip
- Must be accounted for during **design**
- Using **approximate models**
- Detailed **post-layout verification** also necessary

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- ## Outline
- **Capacitance**
Area/perimeter model, coupling
 - **Resistance**
Sheet resistance
 - **Interconnect delay**
Delay metrics, rc delay, Elmore delay
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Capacitance

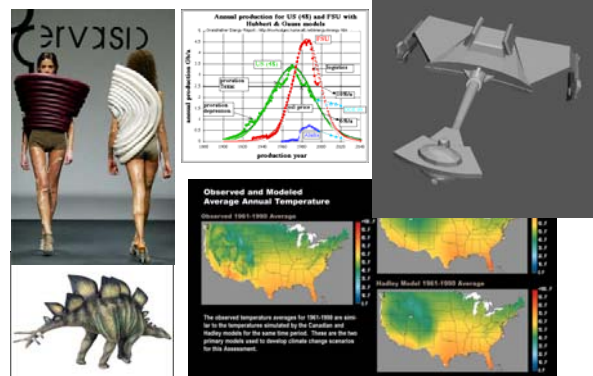
- Area/perimeter model, coupling

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Wake Up! Models ahead!



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Merriam-Webster Online Dictionary

6 critics found for **model**. To select an entry, click on it.

model (noun)
 modeler (verb)
 modeled (adjective)
 animal model
 role model
 WebstersClick model

Main Entry: **ˈmɒ-dəl**

Pronunciation: **mɒ-dəl**
 Function: **noun**

Etymology: Middle French *modèle*, from Old Italian *modellino*, from (assumed) Vulgar Latin *modellus*, from Latin *modulus* small measure, from *modus*

1 **obsolete**: a set of plans for a building
 2 dialect *British*: a very, very, small one
 3 structural design: a home on the *model* of an old farmhouse
 4 a usually miniature representation of something; also: a pattern of something to be made
 5 an example for imitation or emulation
 6 a person or thing that serves as a pattern for an artist, especially: one who poses for an artist
 7 ARCHETYPE
 8 an organism whose appearance a mimic imitates
 9 one who is employed to display clothes or other merchandise

(as an acronym) **MODEL** can be directly observed

12: a system of postulates, data, and inferences presented as a mathematical description of an entity or state of affairs

12: VERSION

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Modeling

- An **abstraction** of (the properties) of something to help **understanding and predicting** its behavior
- **Domain Specific**: weather, climate, economy, stock market, ...
- Different models for something to **answer different questions**
- **Black-Box** modeling vs. **Physically Based**

After Einstein:

a model should be as simple as possible, but not simpler

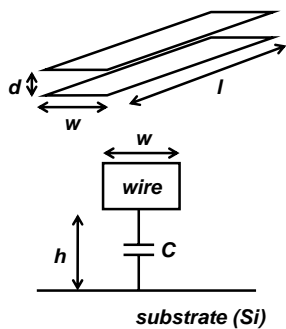


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Wire Capacitance - Parallel Plate



$$C = \frac{\epsilon_0 \epsilon_r w l}{d}$$

$$\frac{C}{l} = \epsilon_0 \epsilon_r \frac{w}{h}$$

$$\epsilon_0 = 8.85 \text{ pF/m}$$

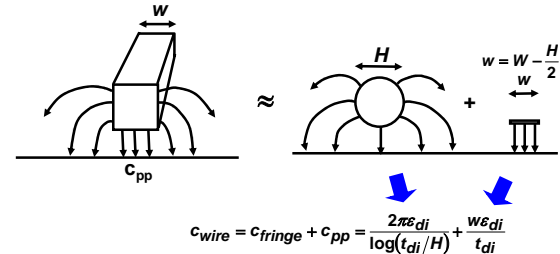
$$\epsilon_r = 3.9 \text{ (SiO}_2\text{)}$$

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Wire Capacitance - Fringing Fields



$$C_{\text{wire}} = C_{\text{fringe}} + C_{\text{pp}} = \frac{2\pi\epsilon_0 d_i}{\log(t_{di}/H)} + \frac{w\epsilon_0 d_i}{t_{di}}$$

- Works reasonably well in practice
- Not directly applicable for interconnects with varying widths

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Wire Capacitance – Area/Perimeter Model

- C_a was calculated with modified wire width
- Formula inapplicable for irregular interconnects (non-constant width)



- More practical approximation

$$C = A \times C_a + P \times C_p$$

A = Area	units	alternative
	m^2	μm^2
C_a = Area capacitance	F/m^2	$aF/\mu m^2$
P = Perimeter	m	μm
C_p = Perimeter capacitance	F/m	$aF/\mu m$

$$1\mu \downarrow \begin{array}{|c|} \hline \text{---} \\ \hline \end{array} \begin{array}{|c|} \hline \text{---} \\ \hline \end{array} \quad C = \square \times C_a + \square \times C_p$$

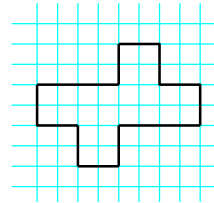
10μ

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Area / Perimeter Capacitance Model



$$C = \square \times C_a + \square \times C_p$$

- **Question:** How to derive C_a, C_p ?

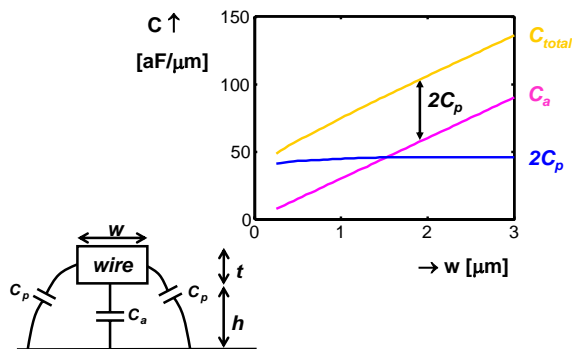
How accurate is this model?

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Derivation of C_a, C_p



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Derivation of C_a, C_p

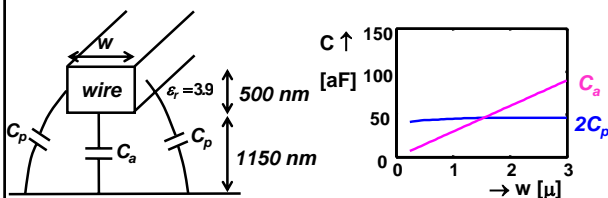
- 2D (cross-section) numerical computation (or measurement)
- C_l : total wire capacitance per unit length
- $C_a = \epsilon_0 \epsilon_r / h$
- $C_p = 1/2(C_l - C_a \times w)$
- C_p depends on t, h → determined by technology, layer
- C_p would depend slightly on w (see previous graph), this dependence is often ignored in practice

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Area / Perimeter Capacitance



- C_p dominates for many wires
- C_p may not be neglected
- A constant value for C_p is usually a good approximation
- C_p is sometimes called C_f (fringe capacitance)

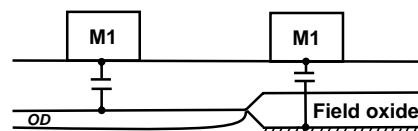
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Interconnect Capacitance Design data

- See Table 4.2 (or inside backside cover)
- Example: M1 over Field vs. M1 over Active (hypothetical)



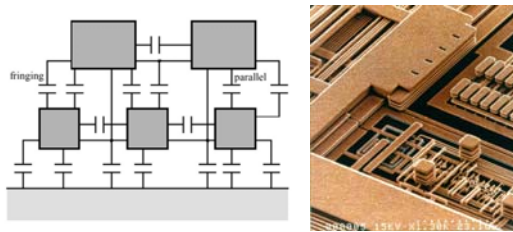
M1 over Active	M1 over Field	Unit
$C_a = 41$	$C_a = 30$	$aF/\mu m^2$
$C_p = 47$	$C_p = 40$	$aF/\mu m$

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Coupling Capacitances

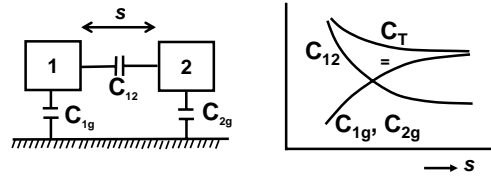


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Coupling Capacitances (2)



- $C_T = C_{1g} + C_{12} = C_{2g} + C_{12}$ fairly constant
- Use that as first order model
- Interconnect capacitance design data (e.g. Table 4.3)

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Resistance

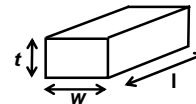
- Sheet resistance

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Wire Resistance



- Proportional to l
- Inversely proportional to w and t (cross-sectional area)
- Proportional to ρ : specific resistance, material property [Ωm]
- $R = \rho l / wt$
- Aluminum: $\rho = 2.7 \times 10^{-8} \Omega\text{m}$
- Copper: $\rho = 1.7 \times 10^{-8} \Omega\text{m}$

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Sheet Resistance

- $R = \rho l / wt$
- t, ρ constant for layer, technology
- $R = R_s l / w$
- R_s : sheet resistance [Ω/\square]
resistance of a square piece of interconnect
other symbol: R_s
- Interconnect resistance design data e.g. Table 4.5 (or inside back-cover)

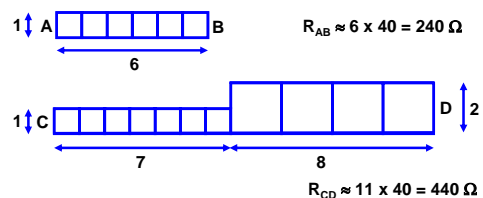
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Interconnect Resistance

- Assume $R_{\square} = 40 \Omega$
- Estimate the resistance between A and B in the wire below.



Engineering is about making controlled approximations to something that is too complicated to compute exactly, while ensuring that the approximate answer still leads to a working (functional, safe, ...) system

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Exercise

An interconnect line is made from a material that has a resistivity of $\rho = 4 \mu\Omega\text{-cm}$. The interconnect is 1200 Å thick, where 1 Angstrom (Å) is 10^{-10}m . The line has a width of $0.6 \mu\text{m}$.

- Calculate the sheet resistance R_{\square} of the line.
- Find the line resistance for a line that is $125 \mu\text{m}$ long.

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Interconnect delay

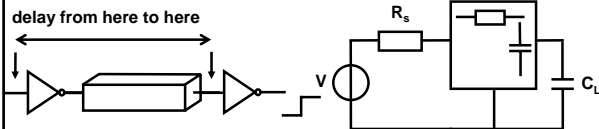
- Delay metrics, rc delay, Elmore delay

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Delay



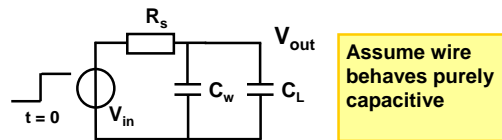
- Model driver as linearized Thevenin source V , R_s , assume step input
- Model load as C_L
- Wire is an RC network (two-port)

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Wire Capacitance



Assume wire behaves purely capacitive

$$(C_w + C_L) \frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_s} = 0$$

$$V_{out} = V_{in} - \tau \frac{dV_{out}}{dt} \quad \tau = R_s(C_w + C_L)$$

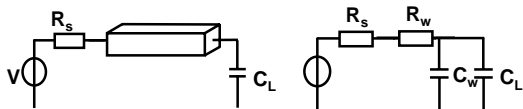
$$V_{out} = (1 - e^{-t/\tau}) V_{in}$$

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Wire Resistance



Now, assume wire capacitance and resistance

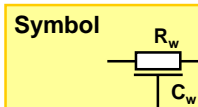
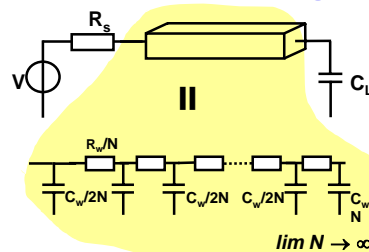
- $\tau = (R_s + R_w)(C_w + C_L)$
- Is this a good model?
- R and C are distributed along the wire

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Uniform RC Line



[Always] use first order model

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RC Delay (Uniform RC Line)

Basic π -model of wire

- $\tau?$

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Equivalent Time Constant

- Multiple time-constants
- Need for one "equivalent" number
- Offered by **Elmore Delay T_D**

$T_D = R_S C_W / 2 + (R_S + R_W)(C_W / 2 + C_L)$

- Effective "one number" model for delay

How to compute Elmore Delay?

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Equivalent Time Constant

$T_D = R_S C_W / 2 + (R_S + R_W)(C_W / 2 + C_L)$

$T_D = \Sigma \left\{ \begin{array}{l} \tau_1 \Rightarrow \\ \tau_2 \Rightarrow \end{array} \right.$

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Shared Path Resistance

- Define: R_{ij} = Resistance from node i to input
- Example: $R_{11} = R_1$ $R_{22} = R_1 + R_2$ $R_{33} = R_1 + R_2 + R_3$
- Define: R_{ik} = Shared path resistance to input for node i and k
- $R_{12} = R_1$ $R_{13} = R_1$ $R_{23} =$

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Elmore Delay for RC ladders

- Define: $T_{Di} = \sum_{k=1}^N R_{ik} C_k$
- $T_{D1} = R_{11}C_1 + R_{12}C_2 + R_{13}C_3 = R_1C_1 + R_1C_2 + R_1C_3$
- $T_{D3} = R_{31}C_1 + R_{32}C_2 + R_{33}C_3 = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$
- $T_{D2} =$

Elmore Delay

We will use $0.69 \times T_{di}$ as approximation of wire delay ($t_{50\%}$)

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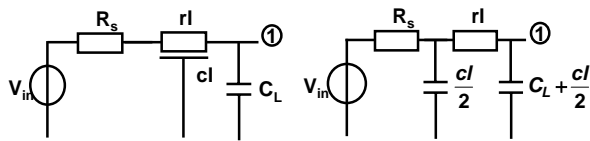
Elmore Delay for Distributed RC Lines

Symbol Symmetric π -model

- Theorem:** For Elmore Delay calculations, each uniform distributed RC section is equivalent to a symmetric π -model

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Canonical Driver-Line-Load



$$T_{D1} = R_s \frac{cl}{2} + (R_s + rl) \left(C_L + \frac{cl}{2} \right)$$

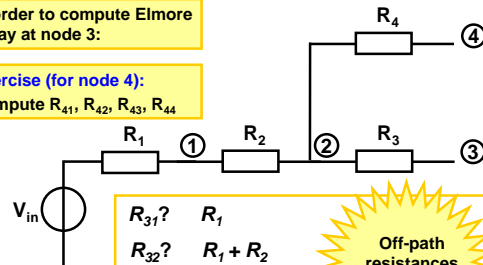
$$= R_s (cl + C_L) + rl C_L + \frac{1}{2} rcl^2$$

■ Delay quadratic in line length

Shared Path Resistance for Tree Structures

In order to compute Elmore Delay at node 3:

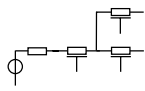
Exercise (for node 4):
Compute R_{41} , R_{42} , R_{43} , R_{44}



- $R_{31}?$ R_1
- $R_{32}?$ $R_1 + R_2$
- $R_{33}?$ $R_1 + R_2 + R_3$
- $R_{34}?$ $R_1 + R_2$

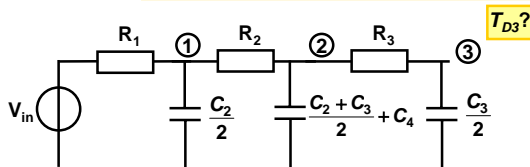
Off-path resistances don't count

Elmore Delay for Tree Structures



- Replace RC lines by π -sections
- Given observation node i , then only resistances along the path from input to node i can possibly count
- Make others zero
- Compute as if RC ladder

Exercise: Compute T_{D1} , T_{D2} , T_{D3} , T_{D4}



Summary

- Capacitance
 - Area/perimeter model, coupling
- Resistance
 - Sheet resistance
- Interconnect delay
 - Delay metrics, rc delay, Elmore delay