Dynamic Power Consumption

Power = Energy/transition • Transition rate

$= C_L V_{DD}^2 \bullet f_{0\to1}$

$= C_L V_{DD}^2 \bullet f \bullet P_{0\to1}$

$= C_{switched} V_{DD}^2 \bullet f$

- -Transistor Sizing
  - Physical capacitance
- -Input and output rise/fall times
  - Short-circuit power
- -Threshold and temperature
  - Leakage power
- -Switching activity

- **Power dissipation is data dependent – depends on the switching probability**
- **Switched capacitance $C_{switched} = P_{0\to1} C_L = \alpha\, C_L$ (α is called the switching activity)**

Signal Probabilities in Simple Gates

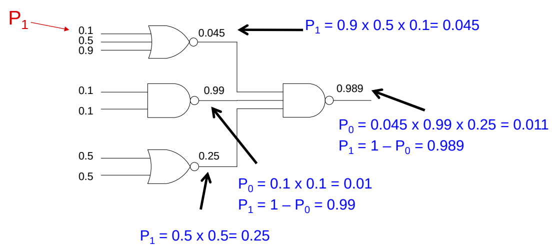
Let $P_x(s)$, $x \in \{0,1\}$, be the probability of signal s being x
Obviously, $P_0(s) = 1 - P_1(s)$

Observe:
- Output of NOR is low iff all inputs are high
- Output of NAND is high iff all inputs are low

Conclude:
- $P_0(\text{NOR}) = \prod P_1(\text{input } i)$
- $P_1(\text{NAND}) = \prod P_0(\text{input } i)$

Signal Probabilities Example

Example: propagate signal probabilities to outputs
Assume P_1 of primary inputs given and *independent*

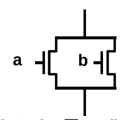


This fails upon reconvergent fanout, correlation of inputs

Signal Probabilities in AOI gates

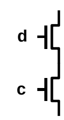
Consider probabilities of blocks being on or off, rather than logic levels
Output is 1 if the pull-down network is off and vice versa

Observe:
- A parallel block (NOR) is off if all constituting blocks are off
- A series block (NAND) is on if all constituting blocks are on



$P_{off}(\text{NOR}) = \prod P_{off}(\text{block } i)$

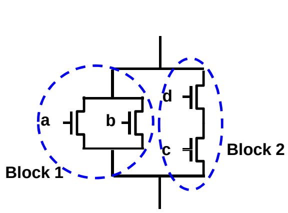
$P_{off} = P_0(a) \times P_0(b)$



$P_{on}(\text{NAND}) = \prod P_{on}(\text{block } i)$

$P_{on} = P_1(c) \times P_1(d)$

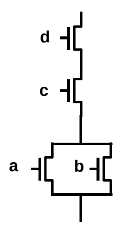
Signal Probabilities in AOI gates (2)



$P_{off}(\text{NOR}) = \prod P_{off}(\text{block } i)$

$P_{off} = P_{off}(\text{block 1}) \times P_{off}(\text{block 2})$

$= P_0(a) \times P_0(b) \times (1 - P_1(c) \times P_1(d))$



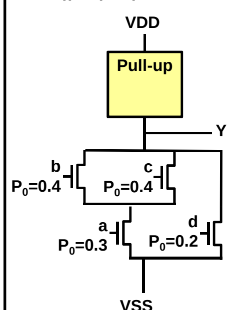
$P_{on}(\text{NAND}) = \prod P_{on}(\text{block } i)$

$P_{on} = (1 - P_0(a) \times P_0(b)) \times P_1(c) \times P_1(d))$

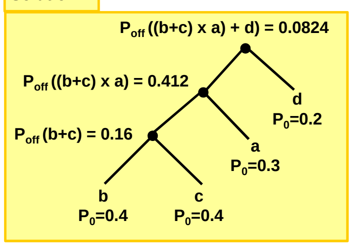
Signal Probabilities in AOI gates Example

$Y = \overline{((b+c) \times a) + d}$

(See Q6 of Exam April 2011)



Solution



P_{off} (pulldown) = 0.0824 ⇒ $P_0(Y)$=0.9176

From Signal Probability to Transition Probability

Example: Static 2-input NAND gate

A	*B*	*Out*
0	0	1
0	1	1
1	0	1
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

$p_{0\rightarrow 1} = p_{Out=0} \times p_{Out=1}$

$= 1/4 \times 3/4 = 3/16$

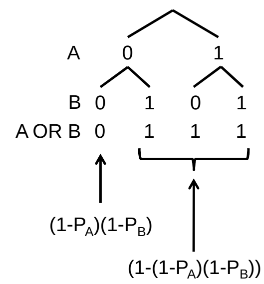
If inputs switch every cycle

$\alpha_{NAND} = 3/16$ $\quad \alpha_{NAND} = p_A p_B (1 - p_A p_B)$

NOR gate yields similar result

Transition Probabilities

Activity for static CMOS gates: $\alpha = p_0 p_1$



Transition Probabilities for Basic Gates

As a function of the input probabilities

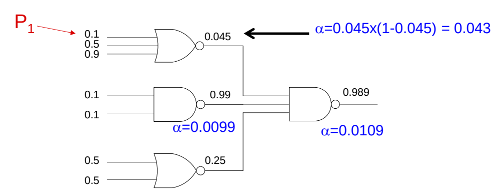
	$p_{0\rightarrow 1}$
AND	$(1 - p_A p_B) p_A p_B$
OR	$(1 - p_A)(1 - p_B)(1 - (1 - p_A)(1 - p_B))$
XOR	$(1 - (p_A + p_B - 2p_A p_B))(p_A + p_B - 2p_A p_B)$

Activity for static CMOS gates: $\alpha = p_0 p_1$

Because of symmetry: AND ⇔ NAND, OR ⇔NOR

Activity Factors

Transition probabilities from signal probabilities



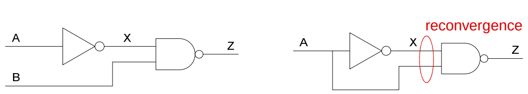
However, calculation becomes far more involved upon:

Reconvergent fanout

Feedback and temporal/spatial correlations

Reconvergent Fanout (Spatial Correlation)

Inputs to gate can be interdependent (correlated)



no reconvergence

$P_Z = 1-(1-P_A)P_B$

P_Z: probability that Z=1

reconvergent

$P_Z = 1-(1-P_A)P_A$?

NO!

$P_Z = 1$

Must use conditional probabilities

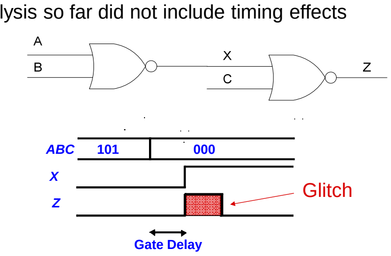
$\mathbf{P_Z = 1 - P_A \cdot P(X|A) = 1}$

probability that X=1 given that A=1

Becomes complex and intractable real fast

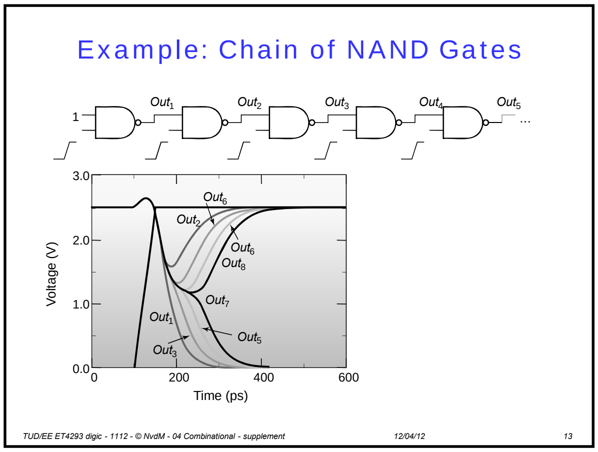
Glitching in Static CMOS

Analysis so far did not include timing effects



The result is correct,
but extra power is dissipated

Also known as dynamic hazards:
"A single input change causing multiple changes in the output"



Example: Chain of NAND Gates
Out1
Out2
Out3
Out4
Out5
Voltage (V)
Time (ps)
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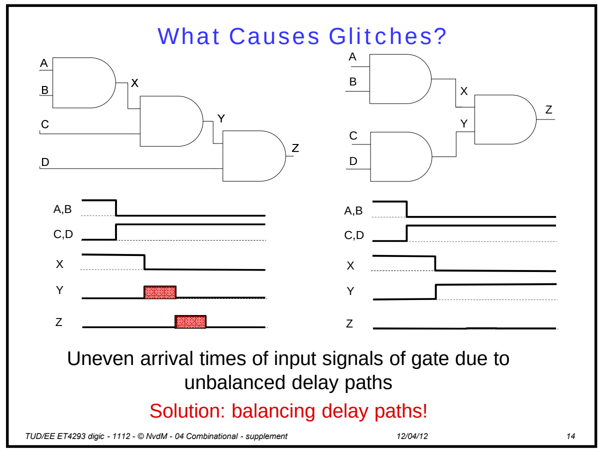

What Causes Glitches?
A,B
C,D
X
Y
Z
Uneven arrival times of input signals of gate due to unbalanced delay paths
Solution: balancing delay paths!
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