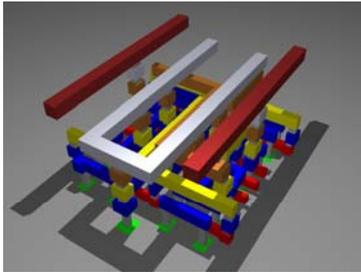


**MODULE 5**  
**Chapter 7**



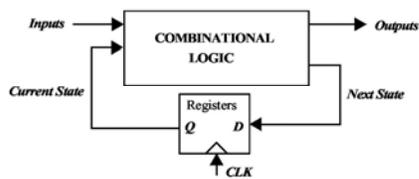
**Clocked Storage Elements**

**Clocked Storage Elements**

**Outline**

- **Background**
  - Timing, terminology, classification
- **Static CSEs**
  - Latches
  - Registers
- **Dynamic CSEs**
  - Latches
  - Registers

**FSM with Positive Edge Triggered Registers**



- CSEs/Flip-flops provide **memory/state**
- VLSI uses predominantly **D-type flip-flops**

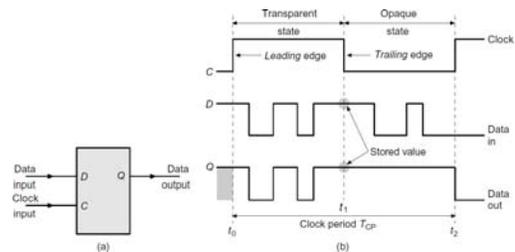
**Memory elements**

- Store a **temporary value**, remember a **state**
- Separate the **past, current, future**
- Typically controlled by **clock**.
- May have load signal, etc.
- In CMOS, memory is created by:
  - **capacitance** (dynamic);
  - **feedback** (static).
- Also see [http://en.wikipedia.org/wiki/Flip-flop\\_\(electronics\)](http://en.wikipedia.org/wiki/Flip-flop_(electronics))

**Variations in memory elements**

- **Form of required clock signal.**
- **How behavior of data input around clock affects the stored value.**
- **When the stored value is presented to the output.**
- **Whether there is ever a combinational path from input to output.**
- **Noise sensitivity on input and output**
- ...

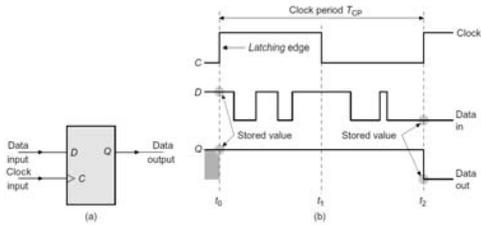
**D-Latch**



[Taskin, Kourtev & Friedman, The VLSI Handbook]

## D-Register

(more commonly known as D-Flip-Flop)



[Taskin, Kourtev & Friedman, The VLSI Handbook]

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7

## Latches vs. Registers

Terminology of book

### Latch

Level-sensitive

Transparent when clock is active

Clock active high: positive latch

Clock active low: negative latch

Faster, smaller

### Register

Edge-triggered

Input and output isolated

Sampling on 0 → 1 clock: positive edge triggered

Sampling on 1 → 0 clock: negative edge triggered

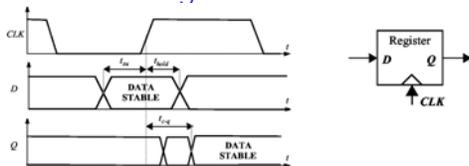
Safer

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8

## Timing Metrics Reminder



$t_{c-q}$  : delay from clock (edge) to Q

$t_{su}$  : setup time

$t_{hold}$  : hold time

$t_{plogic}$  : worst case propagation delay of logic

$t_{cd}$  : best case propagation delay (contamination delay)

T : clock period

$$T \geq t_{c-q} + t_{plogic} + t_{su}$$

$$t_{cdregister} + t_{cdlogic} \geq t_{hold}$$

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9

## Static vs. Dynamic Memory Elements

### Static

Operate through positive feedback

Preserve state as long as power is on

Can work when clock is off

More robust

### Dynamic

Store charge on (parasitic) capacitor

Charge leaks away (in milliseconds)

Clock must be kept running (for periodic refresh)

Faster, smaller

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10

## Static CSEs / Flipflops

### ■ Latches

### ■ Registers

Large part of literature talks about

**Clocked Storage Elements**

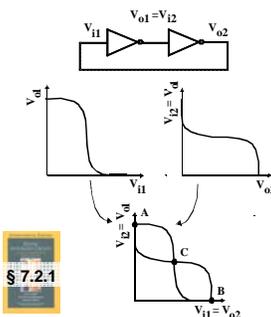
Are called **Flip-Flops** in book

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11

## Positive Feedback: Bi-Stability



■ Loop-gain in A,B  $\ll 1$

■ A,B: stable points

■ Loop-gain in C  $\gg 1$

■ C: meta-stable point

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12

### Meta-Stability

**Gain should be larger than 1 in the transition region**  
**Smaller than 1 in stable region**

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### SR-Latch

S	R	Q	Q̄
0	0	Q	Q̄
1	0	1	0
0	1	0	1
1	1	0	0

← forbidden

S	R	Q	Q̄
1	1	Q	Q̄
0	1	1	0
1	0	0	1
0	0	1	1

← forbidden

§ 7.2.5

- Construction of D-latch
- D-latch most common in VLSI

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### Clocked SR-Latch

- Naive implementation
- 16 transistors
- D latch requires 9xN, 9xP
- Master-slave D-register needs 18xN, 18xP
- Larger area, cost, power

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### CMOS Clocked SR-Latch

$\phi = CK$

- Save 6 PMOS, 2 NMOS transistors
- D-latch requires 7 x N, 3 x P (instead of 9xN, 9xP)

(TPS): Is this a ratioed design or not?

Does it consume static power?

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### Sizing for 'Set' Action

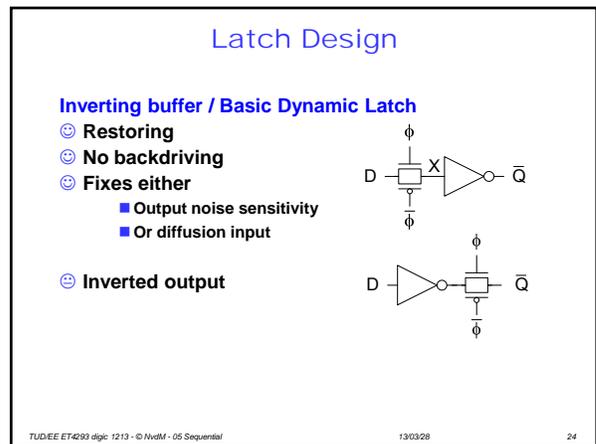
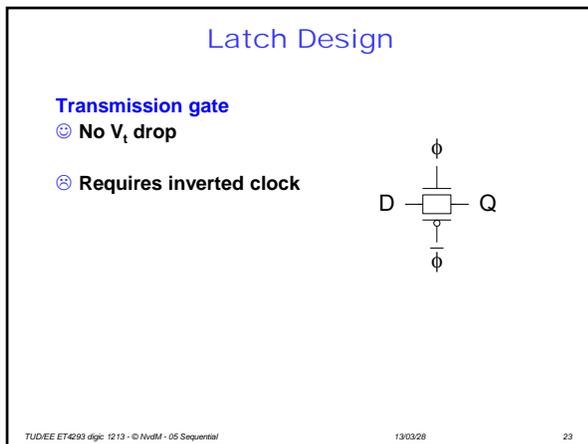
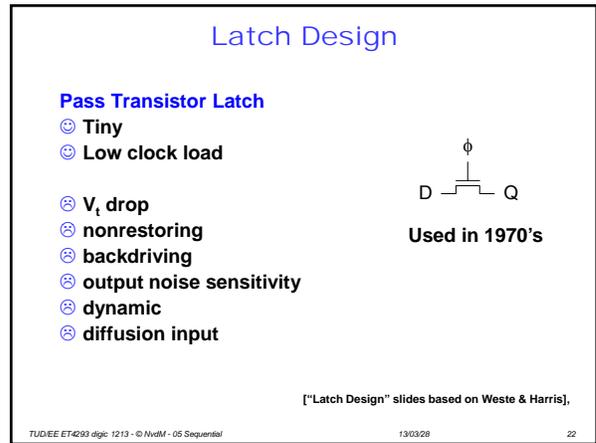
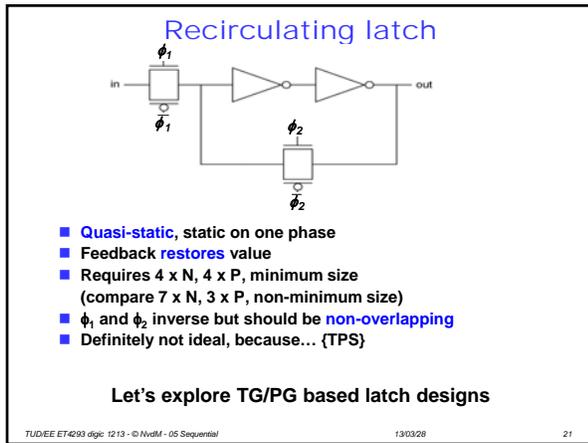
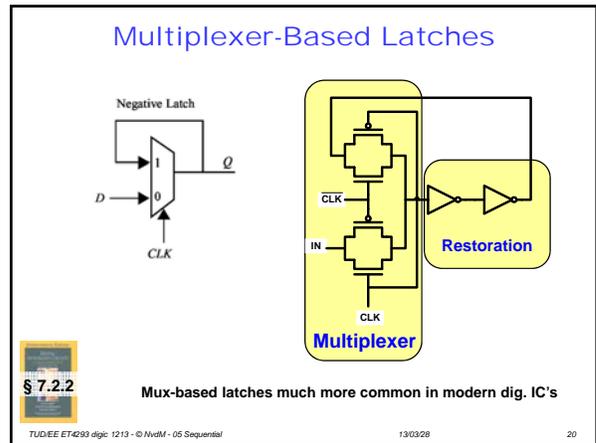
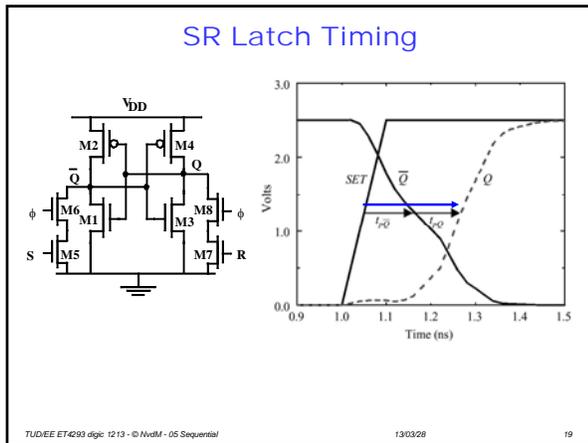
- M<sub>3</sub>-M<sub>4</sub> form conventional inverter
- Model M<sub>5</sub>-M<sub>6</sub> as one equivalent (double length) transistor M<sub>56</sub>
- Assume Q = 0 → M<sub>1</sub> is off, M<sub>2</sub> is on
- M<sub>2</sub>-M<sub>56</sub> operate like ratioed pseudo NMOS inverter
- Latch switches when M<sub>56</sub> pulls input of M<sub>3</sub>-M<sub>4</sub> below their switching threshold (assume V<sub>DD</sub>/2)
- Positive feedback amplifies switching
- M<sub>2</sub> and M<sub>56</sub> both in velocity saturation around V<sub>Q</sub> = V<sub>DD</sub>/2

$$k'_n \left(\frac{W}{L}\right)_{5-6} \left( (V_{DD} - V_{Tn}) V_{DSATn} - \frac{V_{DSATn}^2}{2} \right) = k'_p \left(\frac{W}{L}\right)_2 \left( -V_{DD} - V_{Tp} \right) V_{DSATp} - \frac{V_{DSATp}^2}{2}$$

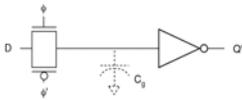
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### Sizing for 'Set' Action

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## Dynamic Latch



- Storage capacitance comes primarily from inverter gate capacitance.
- Setup and hold times determined by transmission gate—must ensure that value stored on transmission gate is solid.
- Stored charge leaks away
  - Duration of stored value being good depends on technology
  - Worst conditions during burn-in (High VDD, high Temp).
- Modern technologies (almost) mandate static latches.

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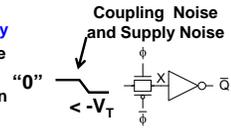
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25

## Noise Sensitivity

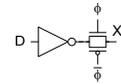
### Diffusion Input Noise Sensitivity

- Noise on input can drop node below  $V_T$
- TG NMOS turns on, and X can discharge if it was a "1"
- Similar problems for  $V_{in} > V_{DD}$



### Output Noise Sensitivity

- State node X is exposed
- Noise spike on output can corrupt the state



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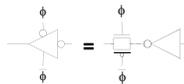
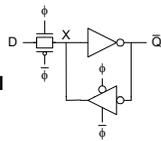
26

## Latch Design

### Tristate feedback

- ☺ Static
- ☹ Backdriving risk

- Static latches are now essential because of leakage
  - If only during burn-in (@ high VDD, T)



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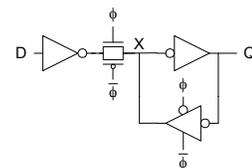
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27

## Latch Design

### Buffered input

- ☺ Fixes diffusion input
- ☺ Noninverting



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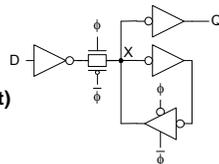
28

## Latch Design

### Buffered output

Widely used in standard cells

- ☺ No backdriving
- ☺ Very robust (most important)
- ☹ Rather large
- ☹ Rather slow (1.5 – 2 FO4 delays)
- ☹ High clock loading



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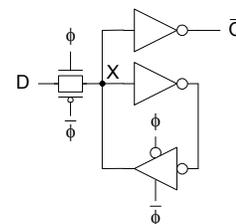
29

## Latch Design

### Datapath latch

(only use in noise-controlled environments)

- ☺ Smaller
- ☺ Faster
- ☹ Unbuffered input

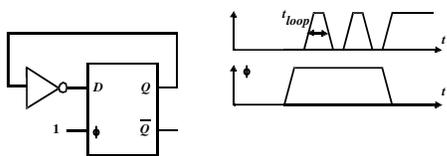


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30

## Latch Designs can Suffer from Race Problems



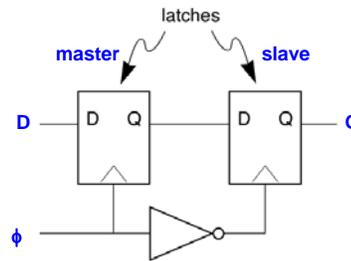
Signal can race around during  $\phi = 1$



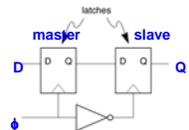
§ 7.2.3

## Registers

- Not transparent—use multiple storage elements to isolate output from input.
- Master-slave, edge triggered principle

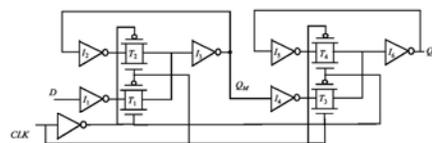


## Master-slave operation



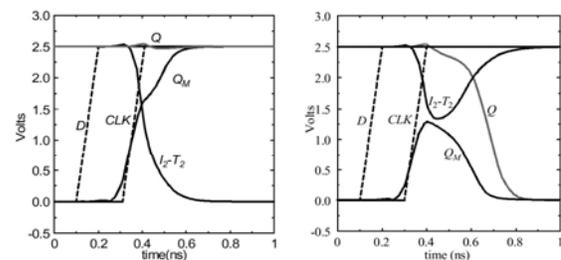
- $\phi = 0$ :
  - master latch is disabled;
  - slave latch is enabled,
  - but master latch output is stable,
  - so output does not change.
- $\phi = 1$ :
  - master latch is enabled,
  - loading value from input;
  - slave latch is disabled,
  - maintaining old output value.
- $\phi = 1 \rightarrow 0$ :
  - Slave latch copies current value of master, and master stops changing

## Transistor Level Master Slave Positive Edge Triggered Register



- Robust Design
- Can eliminate  $I_1$  and  $I_4$ , however, they make design more robust (avoid charge sharing, robust input) (see next)
- High Clock Load (8 x)

## Set-up Time Simulation



Slightly smaller delay between D and CLK

### Ratioed Reduced Register Clock Load Register

- $I_2$  and  $I_4$  are small, even long
- Lower clock load
- Increased design complexity
- Reduced robustness (reverse conduction / backdriving)

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### Simple Master-Slave Register

Clock phase overlap is important design problem

- Similar problem for 0-0 overlap

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### Dynamic Edge Triggered Register

§ 7.3.1

$t_{su}$   
 $t_{hold}$   
 $t_{cq}$   
 $t_{overlap\ 0-0}$   
 $t_{hold}$

$t_{T1}$   
 approximately zero  
 $t_{T1} + t_{T2} + t_{I3}$   
 $< t_{T1} + t_{I1} + t_{T2}$  Prevent race through  $T_1, I_1, T_2$   
 $> t_{overlap\ 1-1}$  Enforce hold-time constraint

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### Clocking and CSE problems

- Clock overlap with multiple phases great problem in view of clock skew
- Power – in some cases, around 50% of total power
- Delay – setup time, clk-to-Q, ..
- Robustness
- Noise-sensitivity of element, specifically for dynamic elements

Next: advanced CSEs to combat some of the above

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### Other Latches/Registers: C<sup>2</sup>MOS

#### Clocked CMOS Register – insensitive to overlap

“Keepers” can be added to make circuit pseudo-static

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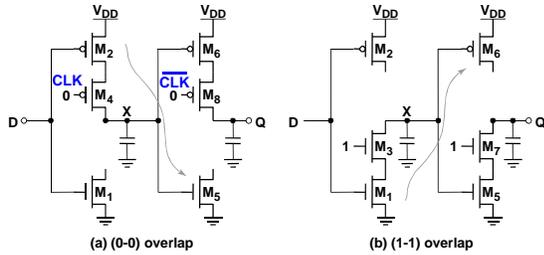
### C<sup>2</sup>MOS Latch

#### Clocked CMOS Latch

Slightly ... Slower  
Slightly ... Smaller

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## Insensitive to Clock-Overlap



Output always decoupled from input, even with overlap

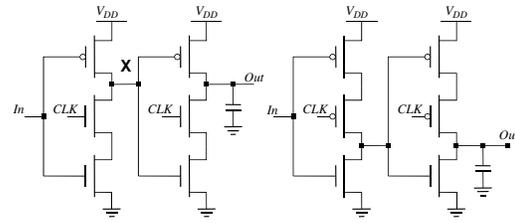
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43

## Other Latches/Registers: TSPC

### True Single Phase Clocking



Positive latch  
(transparent when CLK= 1)

Negative latch  
(transparent when CLK= 0)

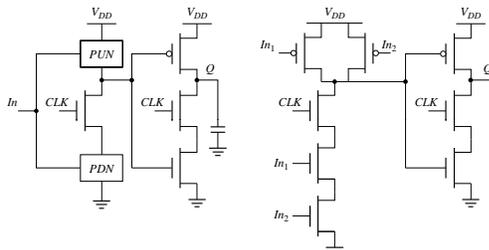
TSPC register: positive and negative latch in cascade

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44

## Including Logic in TSPC



Example: logic inside the latch

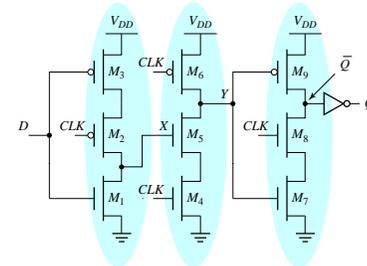
AND latch

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45

## Alternative TSPC Register



Clk = 0	D sampled on X	Precharge Y to VDD	Y ↑ doesn't make Q ↓
Clk ↑		Evaluate based on X	
Clk = 1	Falling X can't charge Y	Y is stable	Y sampled on Q

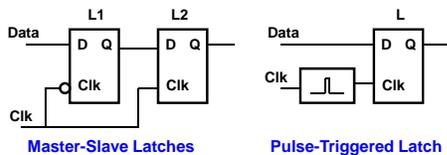
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46

## Pulse-Triggered Latches An Alternative Approach

Remember: Use registers to avoid race-around problem.  
Two latches in cascade: master-slave  
Alternative: Pulse triggered latches



Master-Slave Latches

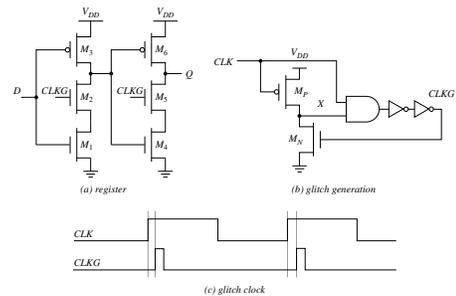
Pulse-Triggered Latch

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47

## Pulsed Latches



(a) register

(b) glitch generation

(c) glitch clock

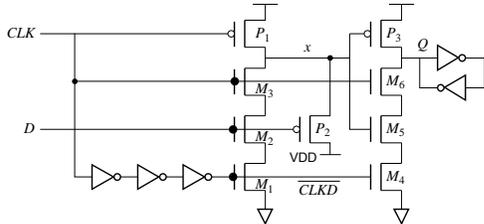
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48

## Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :

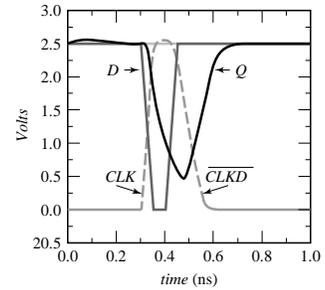


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49

## Hybrid Latch-FF Timing



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50

## More Topics

- Reset and enable inputs
- Scan-enabled CSEs
- Sense-amplifier based CSEs
- Double-edge triggered
- Low-leakage sleep mode
- (Ultra) Low voltage
- Soft-error / SEU tolerance
  
- Timing of CSEs

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51

## Summary

- Background
  - Timing, terminology, classification
- Static CSEs
  - Latches
  - Registers
- Dynamic CSEs
  - Latches
  - Registers

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52