

Write your name and student number
on all pages that you submit

Exam Digital IC Design (ET4293)

Date: Thursday, March 3, 2008 Time: 09.00 am – 12.00 am

Name:	Student number:	Mark:
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Read first:

- Write your name and student number in the boxes above and on the odd numbered pages.
- This is an open-book exam, you can use the Rabaey book and a printed copy of the lecture slides.
- You are allowed to use a calculator.
- Circle or cross the right answer of multiple-choice.
- Write your answers on this paper in the reserved spaces. Optionally, you can hand in extra pages. Write your name and student number on these extra pages, and show on the answer sheets that more details are in the separate sheets.
- Logical inverses (Boolean negation) is identified with primes ('). (Sometimes with an overbar.)
- When you need to give an explanation or calculation, be concise but precise. In graphs, always identify and draw/write the relevant values and quantities. Pay attention to the units, and scale factors.

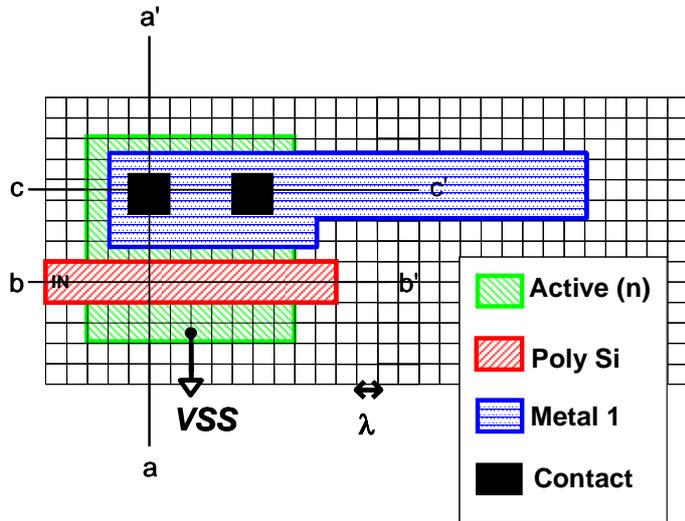
Question 1.

See the layout of a NMOS transistor at the right.

a. What are the length and width of the transistor (in λ)?

W =

L =

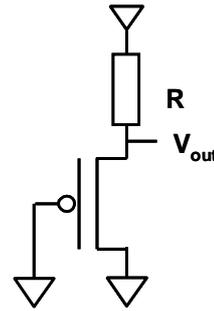


b. Draw the cross-sections a-a', b-b' and c-c'.

a-a'	b-b'	c-c'
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Question 2.

a. Consider the figure on the right. Assume that R is very large. What is the best approximation of V_{out} ?



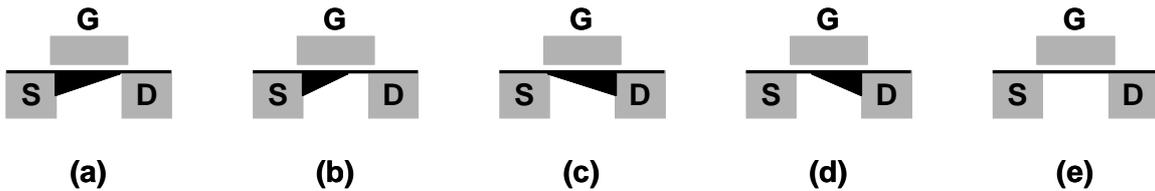
(a) $-V_{Tp}$	(b) V_{Tp}	(c) $VDD-V_{Tp}$	(d) 0	(e) VDD
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b. In the preceding circuit, the body effect makes the voltage V_{out} :

(a) Higher	(b) Lower	(c) No effect	(d) Can not be determined
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Question 3.

De figures below represent a side-view of a MOSFET with its channel under different operating conditions. Use the figures for the following questions. The transistors are 'typical' digital MOS transistors, like from the book of Rabaey.



a. Which of the figures above is the best representation of the channel in the schematic on the right (Choose one of (a) – (e)).



Figure:

b. Which of the figures above is the best representation of the channel in the schematic on the right (Choose one of (a) – (e)).

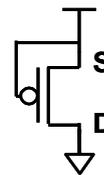


Figure:

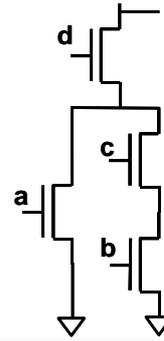
c. Which of the figures above is the best representation of the channel of an NMOS transistor with $V_{GS}=2.5V$, $V_{DS}=2.3V$, $V_T = 0.7V$ en $V_{SB}=0V$ (Choose one of (a) – (e)).

Figure:

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Question 4.

The VDD (supply voltage) of the circuit on the right is 2.0V. The transistors are those from the Rabaey book and all have the same W/L ratio, which is 8.



a. Give the input values (logical values, either 0 or 1) for the best-case and worst-case pull-down resistance.

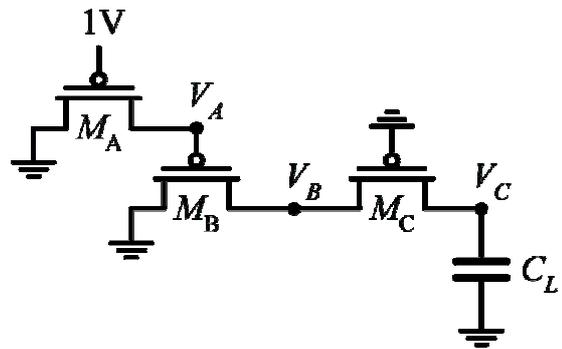
Best-case abcd =	Worst-case abcd =
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b. Consider the case with input a and d being high (equal to VDD) and input b and c being low (0V). Determine the effective on-resistance R_{on} of the pull-down network.

$R_{on} =$
Calculation:

Question 5.

For the circuit at the right, determine the final value of V_A , V_B , V_C , assuming the initial condition at each of the nodes is 3V and $V_{TP} = -0.5V$ (ignore the body effect).

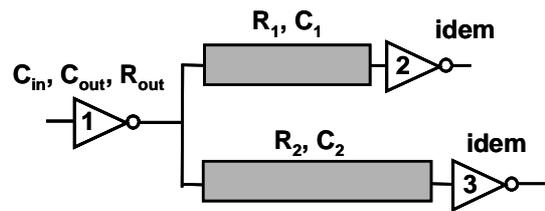


$V_A =$	$V_B =$	$V_C =$
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Explanation:

Question 6.

Consider the circuit on the right with 3 identical invertors and 2 different interconnects. The total resistance and capacitance of these interconnects, R_i and C_i ($i = 1, 2$) is shown in the figure (only symbolic value, not numerical). These 3 identical invertors have an input capacitance of C_{in} , an output capacitance of C_{out} and an equivalent output resistance of R_{out} .



Note: 'idem' means 'identical'

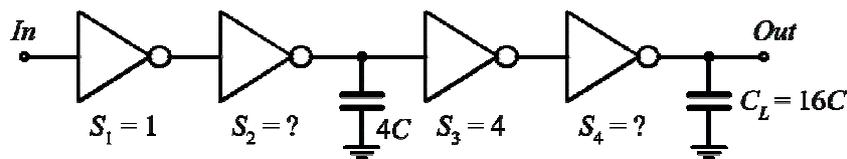
a. Draw the equivalent schematic, consisting of one voltage source and the minimum number of R's and C's (no distributed R/C elements!) to determine the Elmore delay from the input of invertor 1 to the input of invertor 2. For each R and C in the schematic, present its value in terms of the parameters ($R_i, C_i, C_{in}, C_{out}, R_{out}$) in the schematic above.

Equivalent schematic:

b. Determine the Elmore delay from the input of invertor 1 to the input of invertor 2 in terms of the parameters ($R_i, C_i, C_{in}, C_{out}, R_{out}$) in the schematic above. Only an answer, no calculation.

$T_{ed} =$

Question 7.



a. Consider the circuit above. You need to determine the sizes S_2 and S_4 such that the delay is minimal. What is the delay, expressed in terms of t_{p0} (intrinsic delay)? Give calculation.

$S_1 =$

$S_2 =$

$t_p =$

Calculation:

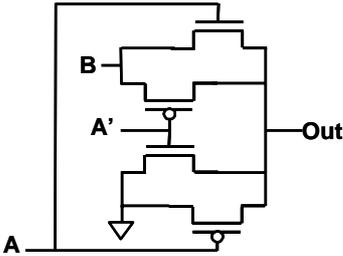
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(continued)

Question 8.

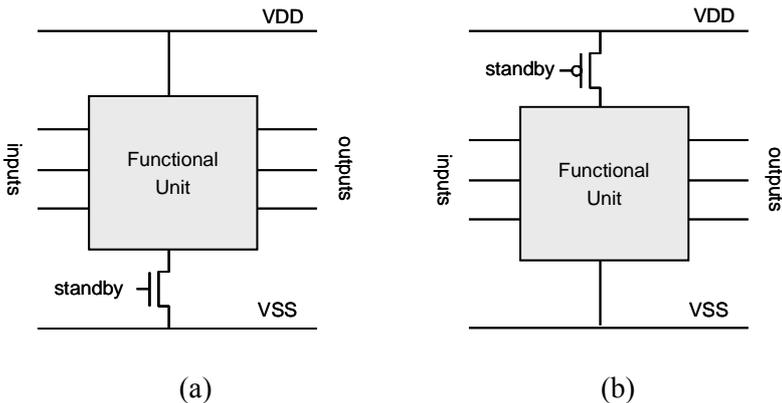
Give the Boolean formula for the circuit at the right.

Out =



Question 9.

Consider the 2 circuits on the right. The large blocks, of which the function is not important now, require to be switched into stand-by mode by disconnecting them from the supply. This can be done with either an NMOS in the VSS line or a PMOS in the supply line.



The standby transistor, in both cases, must be able to deliver enough current for the functional unit without too large a voltage drop. The standby transistors are in the 0.25mm process technology from the 2nd edition Rabaey book.

a. Which of the circuit alternative, (a) or (b) would be your choice, and why?

Answer:

Explanation:

Now consider circuit (b), with the PMOS transistor.

b. What is the operating region if the circuit is in standby mode with $|V_{ds}| < 0.1 \text{ V}$

Operating region:

Explanation/Calculation:

c. Determine the minimum width of the PMOS transistor (when $L = 0.25 \mu\text{m}$), such that $|V_{ds}| < 0.1 \text{ V}$ when $|I_{ds}| = 10\text{mA}$.

$W_{\text{min}} =$

Calculation:
