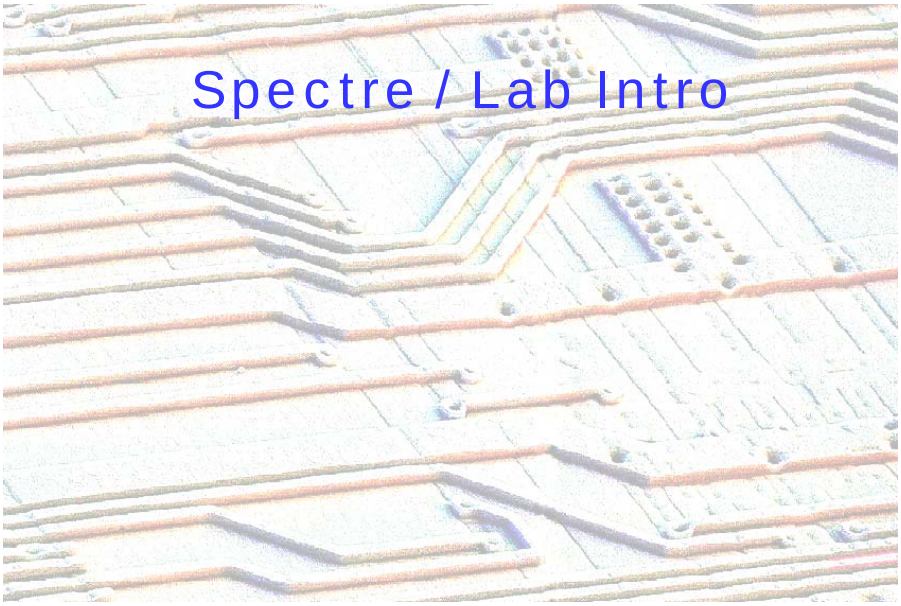
Spectre / Lab Intro



Lab / Project

- **Prepare yourself, form pairs**
- **Become (more) familiar with linux, cadence**
- **Can use computers in MSc lab (16th floor)**
- **Instructions are posted on web, being augmented through the course**
- **Use net-id for login**

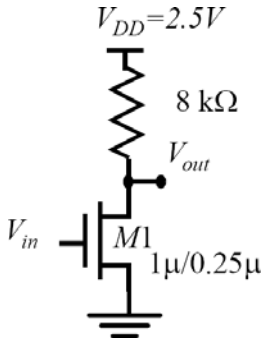
This Week's Plan
homework and labwork

1. **Become (more) familiar with linux**
   - **Tutorial: http://www.ee.surrey.ac.uk/Teaching/Unix/**
   - **In general, resources on class website**
   - **Use (!) BB forum to ask questions and share knowledge**

2. **Become familiar with Spectre (ckt sim)**
   - **Next slides show how to solve Rabaey Exercise 3.11**

3. **Solve Rabaey Exercises 3.4, 3.5 and 3.11**
   - **Use Spectre simulator**
   - **Spectre instructions follow**
   - **Hand-in 1 A4 with 4 annotated graphs on Mon 16/2 before class**
   - **Write your names (as a team) on it**
   - **Will not be graded, get feedback as necessary**

Exercise 3.11



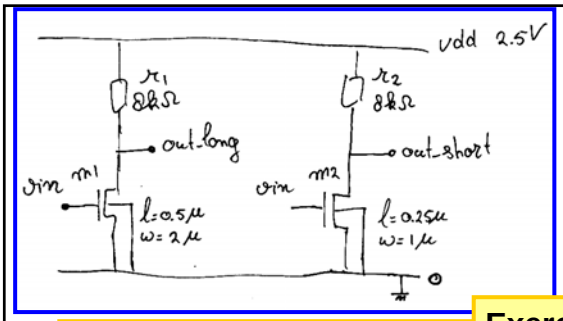
11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). V_{DD} = 2.5 V.

b. Repeat *a* using SPICE.

c. Repeat *a* and *b* using a MOS transistor with (W/L) = 4 / 1. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

http://cobalt.et.tudelft.nl/~nick/courses/digic/SpectreIntro.html



Simulation Example

- Make sketch
- Assign node names
- Write file
- Add control statements
- Or use schematic entry

Exercise 3.11

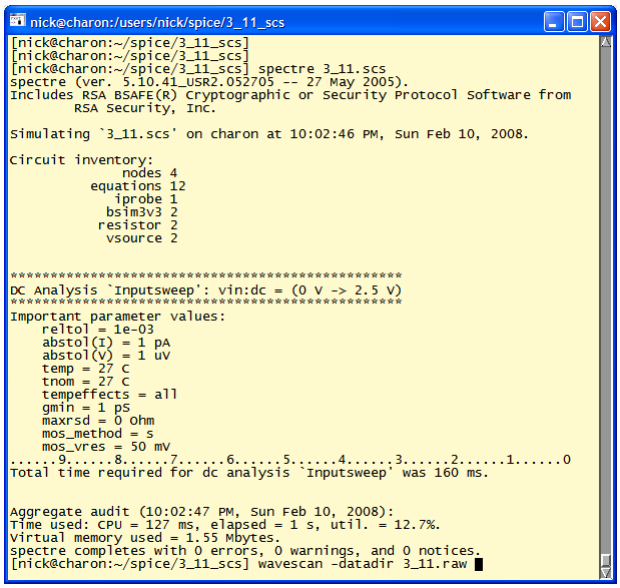
```
simulator lang=spectre
include "g25_scs.lib"     ← see course website
vdd (vdd 0) vsource dc=2.5
vin (in 0) vsource dc=2.5
r1 (vdd out_long) resistor r=8K
r2 (vdd out_short) resistor r=8k
m1 (out_long in 0 0) nmos l=0.5u w=2u
m2 (out_short in 0 0) nmos l=0.25u w=1u
Inputsweep dc param=dc dev=vin start=0 stop=2.5 step=0.1
save vin out_long out_short
```


250nm Spectre BSIM3 MOS Models

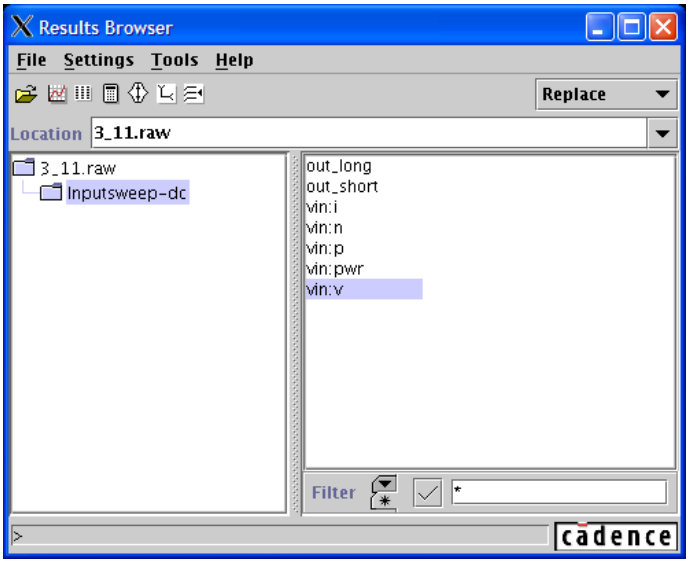
```
simulator lang=spectre
model nmos bsim3v3
+version=3.1
+type=n
+tnom    = 25            xl      = 3e-8
+xw      = 0             tox     = 5.8e-9
+xj      = 1e-07         nch     = 2.354946e+17   lln     = 1
+vth0    = 0.4321336     lvth1   = 2.081814e-08   wvth0   = -5.470342e-11
+pvth0   = -6.721795e-16 k1      = 0.3281252      lk1     = 9.238362e-08
... 60 lines deleted ...
+tlev    = 1             tlevc   = 1              js      = 1e-06
+jsw     = 5e-11
```

- Similar for **pmos** device

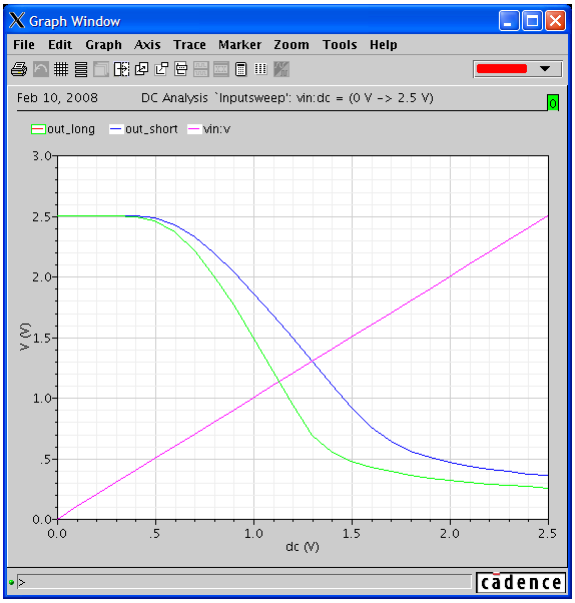
Spectre Terminal Interface



WaveScan Results Browser



WaveScan Graph Window



Exercise 4+5

4. [E, SPICE, 3.3.2] Using SPICE plot the *I-V* characteristics for the following devices.

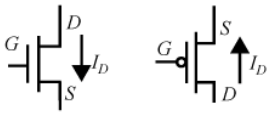


Figure 0.3 NMOS and PMOS devices.

a. NMOS $W = 1.2\mu m$, $L = 0.25\mu m$
b. NMOS $W = 4.8\mu m$, $L = 0.5\mu m$
c. PMOS $W = 1.2\ \mu m$, $L = 0.25\ \mu m$
d. PMOS $W = 4.8\ \mu m$, $L = 0.5\ \mu m$

5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.
a. the regions of operation.
b. the effects of channel length modulation.
c. Which of the devices are in velocity saturation? Explain how this can be observed on the *I-V* plots.

Tips

- Make 4 circuits, 1 for each of the cases 4a-4b
- Each circuit will have 6 transistors
  - All drains are connected, drain voltage to be swept from 0 to 2.5 V
  - All gates unconnected, different gate voltages: 0, 0.5, 1.0, 1.5, 2.0, 2.5 V
- Plot each circuit in a separate graph, combine them on 1 page (word or latex)
  - Wavescan can export png files, looks better compared to screen dumps
  - DON't underestimate importance of good quality graphics in reports

TA Help

TA Qin Tang (HB 17.140)
Q.Tang at tudelft.nl
available: 15:30-17:30 Tuesday and Friday

- **BB Forum** – me and TA's will answer questions