



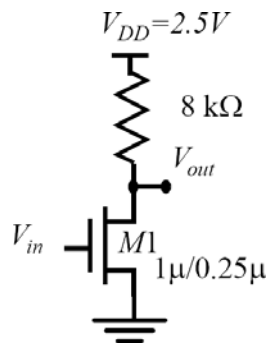
Spectre / Lab Intro

Lab / Project

- Prepare yourself, form **pairs**
- Become (more) familiar with linux, cadence
- Can use computers in MSc lab (16th floor)
- Instructions are posted on web, being augmented through the course
- Use net-id for **login**

This Week's Plan homework and labwork

1. Become (more) familiar with linux
 - Tutorial: <http://www.ee.surrey.ac.uk/Teaching/Unix/>
 - In general, resources on class website
 - Use (!) **BB forum** to ask questions and share knowledge
2. Become familiar with Spectre (ckt sim)
 - Next slides show how to solve Rabaey Exercise 3.11
3. Solve Rabaey Exercises 3.4, 3.5 and 3.11
 - Use Spectre simulator
 - Spectre instructions follow
 - Hand-in 1 A4 with 4 annotated graphs on Mon 16/2 before class
 - Write your names (as a team) on it
 - Will not be graded, get feedback as necessary



Exercise 3.11

11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.
- a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.
 - b. Repeat *a* using SPICE.
 - c. Repeat *a* and *b* using a MOS transistor with $(W/L) = 4/1$. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

<http://cobalt.et.tudelft.nl/~nick/courses/digic/SpectreIntro.html>

Simulation Example

- Make sketch
- Assign node names
- Write file
- Add control statements
- Or use schematic entry

Exercise 3.11

```

simulator lang=spectre
include "g25_scs.lib" ← see course website
vdd (vdd 0) vsource dc=2.5
vin (in 0) vsource dc=2.5
r1 (vdd out_long) resistor r=8K
r2 (vdd out_short) resistor r=8k
m1 (out_long in 0 0) nmos l=0.5u w=2u
m2 (out_short in 0 0) nmos l=0.25u w=1u
Inputsweep dc param=dc dev=vin start=0 stop=2.5 step=0.1
save vin out_long out_short

```

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250nm Spectre BSIM3 MOS Models

```

simulator lang=spectre
model nmos bsim3v3
+version=3.1
+type=n
+tnom = 25          xl = 3e-8
+xw = 0            tox = 5.8e-9
+xj = 1e-07        nch = 2.354946e+17  lln = 1
+vt0 = 0.4321336  lvth1 = 2.081814e-08  wvth0 = -5.470342e-11
+pvth0 = -6.721795e-16  k1 = 0.3281252  lk1 = 9.238362e-08
... 60 lines deleted ...
+tlev = 1          tlevc = 1          js = 1e-06
+jsw = 5e-11

```

- Similar for pmos device

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Spectre Terminal Interface

```
nick@charon:/users/nick/spice/3_11_scs
[nick@charon:~/spice/3_11_scs]
[nick@charon:~/spice/3_11_scs]
[nick@charon:~/spice/3_11_scs] spectre 3_11_scs
spectre (ver. 5.10.41_USR2.052705 -- 27 May 2005).
Includes RSA BSAFE(R) Cryptographic or Security Protocol Software from
RSA Security, Inc.

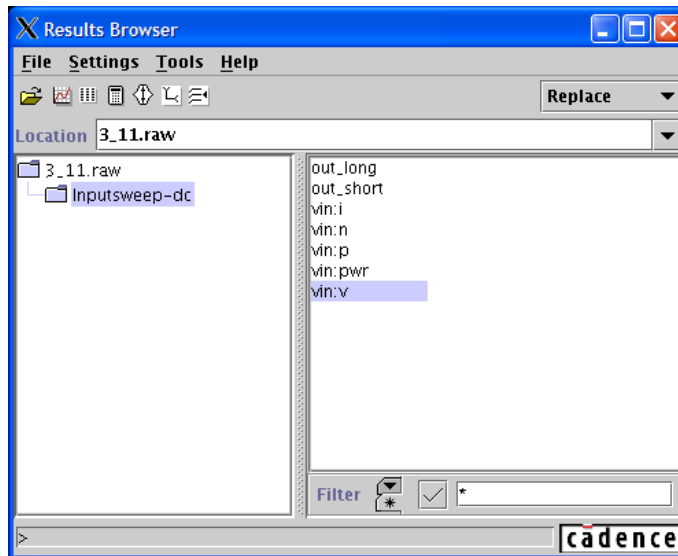
Simulating `3_11.scs' on charon at 10:02:46 PM, Sun Feb 10, 2008.

Circuit inventory:
  nodes 4
  equations 12
  iprobe 1
  bsim3v3 2
  resistor 2
  vsource 2

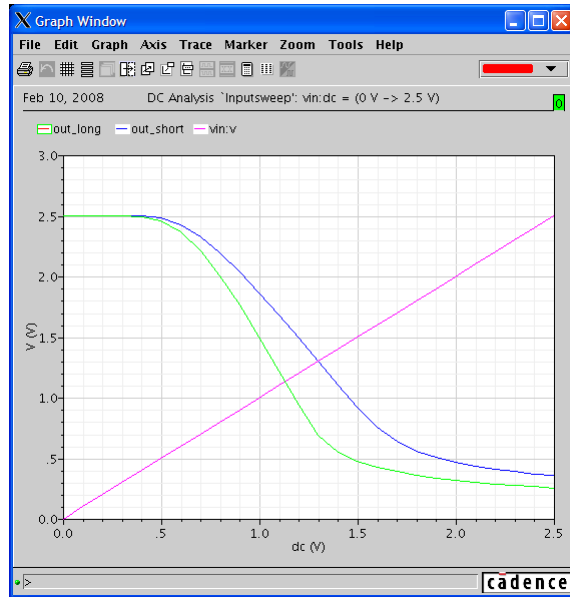
*****
DC Analysis `inputsweep': vin:dc = (0 V -> 2.5 V)
*****
Important parameter values:
  reit01 = 1e-03
  abstol(I) = 1 pA
  abstol(V) = 1 uV
  temp = 27 C
  tnom = 27 C
  tempeffects = all
  gmin = 1 pS
  maxrsd = 0 Ohm
  mos_method = s
  mos_vres = 50 mV
  .....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
Total time required for dc analysis `inputsweep' was 160 ms.

Aggregate audit (10:02:47 PM, Sun Feb 10, 2008):
Time used: CPU = 127 ms, elapsed = 1 s, util. = 12.7%.
Virtual memory used = 1.55 Mbytes.
spectre completes with 0 errors, 0 warnings, and 0 notices.
[nick@charon:~/spice/3_11_scs] wavescan -datadir 3_11.raw █
```

WaveScan Results Browser



WaveScan Graph Window



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Exercise 4+5

4. [E, SPICE, 3.3.2] Using SPICE plot the I - V characteristics for the following devices.

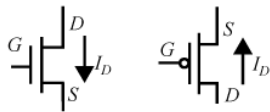


Figure 0.3 NMOS and PMOS devices.

- NMOS $W = 1.2\mu\text{m}$, $L = 0.25\mu\text{m}$
 - NMOS $W = 4.8\mu\text{m}$, $L = 0.5\mu\text{m}$
 - PMOS $W = 1.2\mu\text{m}$, $L = 0.25\mu\text{m}$
 - PMOS $W = 4.8\mu\text{m}$, $L = 0.5\mu\text{m}$
5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.
- the regions of operation.
 - the effects of channel length modulation.
 - Which of the devices are in velocity saturation? Explain how this can be observed on the I - V plots.

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Tips

- Make 4 circuits, 1 for each of the cases 4a-4b
- Each circuit will have 6 transistors
 - All drains are connected, drain voltage to be swept from 0 to 2.5 V
 - All gates unconnected, different gate voltages: 0, 0.5, 1.0, 1.5, 2.0, 2.5 V
- Plot each circuit in a separate graph, combine them on 1 page (word or latex)
 - Wavescan can export png files, looks better compared to screen dumps
 - DON't underestimate importance of good quality graphics in reports

TA Help

TA Qin Tang (HB 17.140)
[Q.Tang at tudelft.nl](mailto:Q.Tang@tudelft.nl)
available: 15:30-17:30 Tuesday and Friday

- **BB Forum** – me and TA's will answer questions