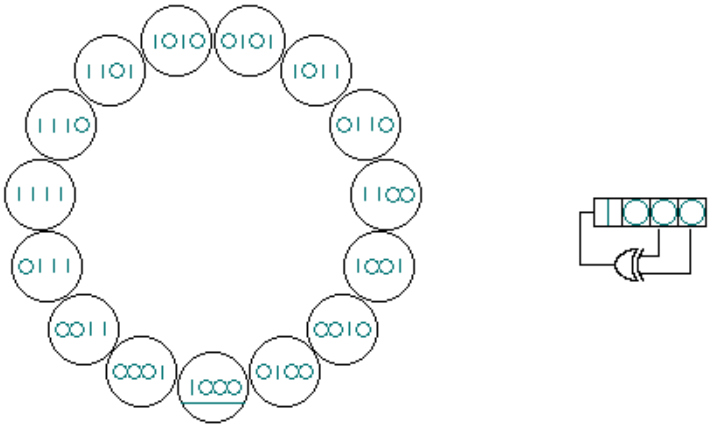
Project

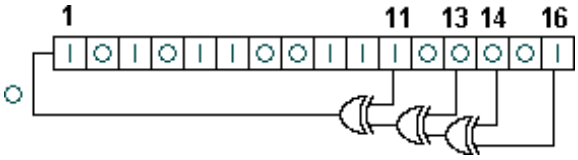
- **Pseudo Random Number Generator (PRNG)**
- **A 'counter' producing an output sequence that approximates the properties of random numbers**
- **Pseudo random sequences have many applications**
  - **Spread spectrum communication**
  - **Whitening**
  - **Monte-Carlo simulation**
  - **Stream ciphers**
  - **Test pattern generation**
  - **…**

4-bit Fibonacci LFSR



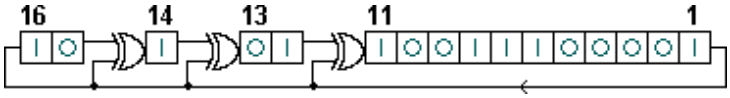
http://en.wikipedia.org/wiki/Linear_feedback_shift_register

Fibonacci vs. Galois Style



- Fibonacci

Can expect differences in speed/power tradeoff



- Galois

Project Requirements

- **8 bit PRNG**
- **Tap positions at 8, 6, 5, 4 for Fibonacci type**
- **Choose between Fibonacci or Galois (adapt 'taps' for Galois)**
- **Clock frequency to be specified (must use clock)**
- **Ideal non-overlapping 2-phase clock is made available**
- **90nm UMC CMOS technology**
- **10 fF load at each output**
- **Clock frequency 800 Mhz, 50ps slopes**
- **Circuit – Simulation – Spectre Simulation (No Layout)**

Design Goal and Deliverables

- **Design Goal: lowest power requirements**
  - **All will use same test bench**
  - **VDD is variable (design specific)**
  - **Projected area of design (i.e. sum of transistor sizes) is not of concern**

- **Deliverables (electronically):**
  - **Design database (for checking performance)**
  - **Presentation**
  - **Design report**

Grading

- **Final grade 50/50% project/exam**

50%	**Exam**	**Written exam (example will be made available)**
30%	**Design**	**Correctness, creativity, elegance, robustness A correct design gives at least a 6.**
10%	**Presentation**	**Relevance, information, (presentation skills)**
10%	**Report**	**Relevance, information, documentation (design decisions) (brief, factual, clarity and easy of reading (!), documentation, not essay or paper)**

Contest

Bonus points for top-n

- **2 points for winner team**
- **1.5 points for 2nd place, 1 for 3rd, 0.5 for 4th, 5th place**
- **Bonus to be added to overall mark**

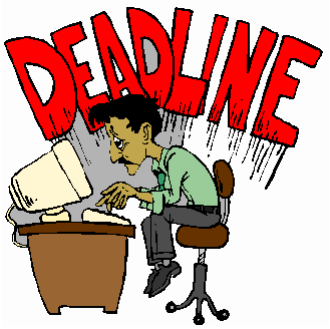
Presentations

- **Why is your design good**
- **What is special about it**
- **Present design decisions, trade-offs, …**
- **Include important schematics, waveforms, …**
- **Everything needed for demonstrating functionality and performance**
- **Try to avoid mostly-black screendumps for graphics, schematics**
- **References/citations (!)**

- **PPT presentation, ~ 10 minutes including Q&A**

Project Schedule

- **Due date: Thu Apr 16**
  (2nd week of next lecture period) Agree?
- **Presentations: 15:30 - finished**



Feel free to

- **Use any circuit style (Chapter 6)**
  - complementary CMOS, ratioed logic, DCVSL, pass-transistor logic, CPL, dynamic logic, …
    (No need to stick to style from book)
- **Any clocking scheme / Flip Flop type (Chapter 7)**
  - single phase, two phase, four phase, ...
  - Avoid Races
- **Consider any known (or unknown ☺) technique to improve power**
  - ckt level: body bias, sub-threshold logic, …,
  - design: automatic sizing, …

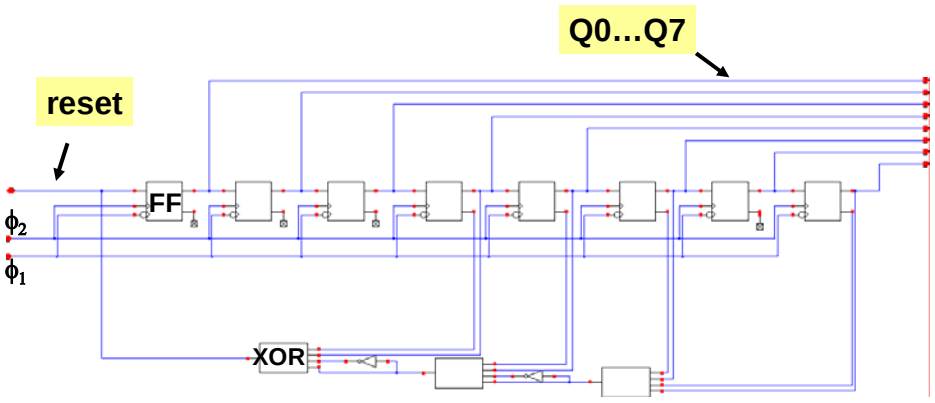
2-phase Clock

- 2-phase clock is made available, can use 1 phase if you want
- More advanced clock has to be derived from it
- Only circuit design, no layout needed for clock generation
- Report (poster) should show schematic, design rationale, resulting waveforms

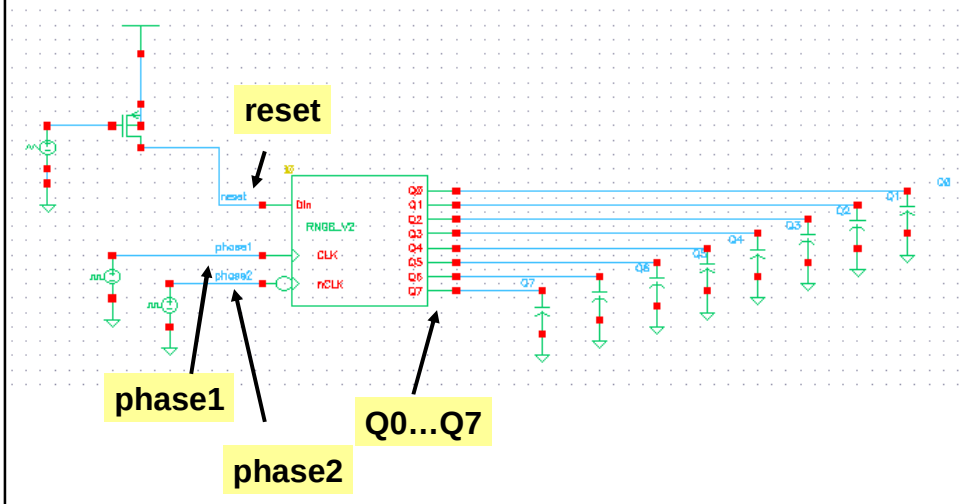
Reference Schematic

- Reference netlist is made available
- This netlist is not tuned, transistors are minimum size, topology not necessarily optimal

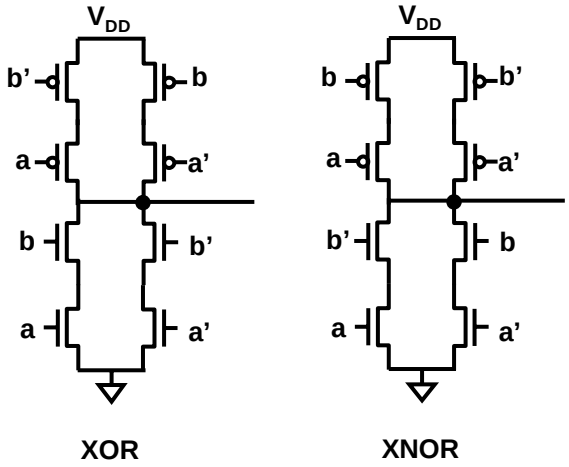
LFSR8



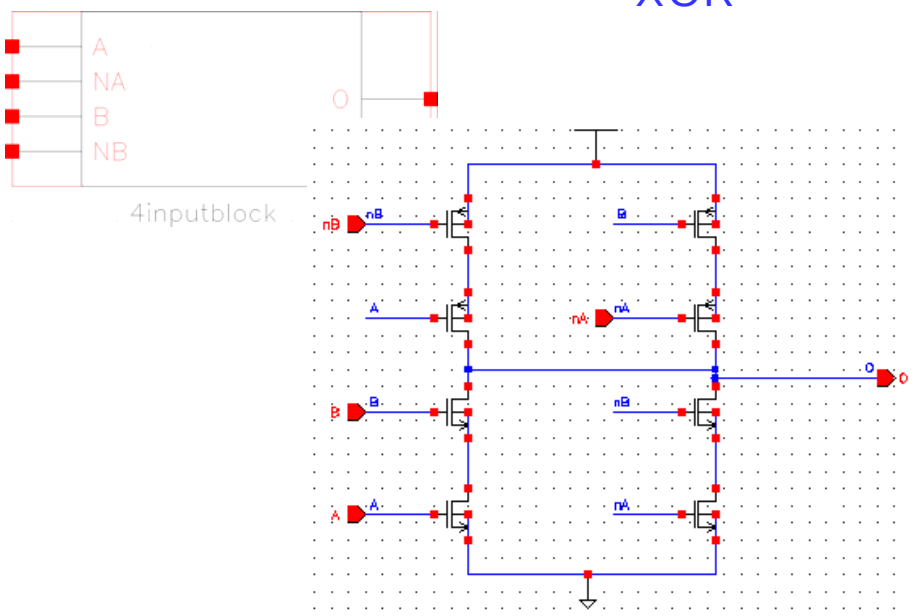
Test Bench



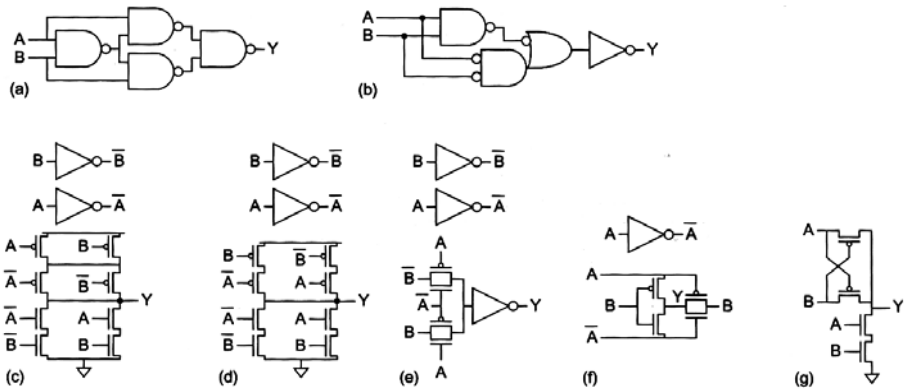
XOR – XNOR



XOR



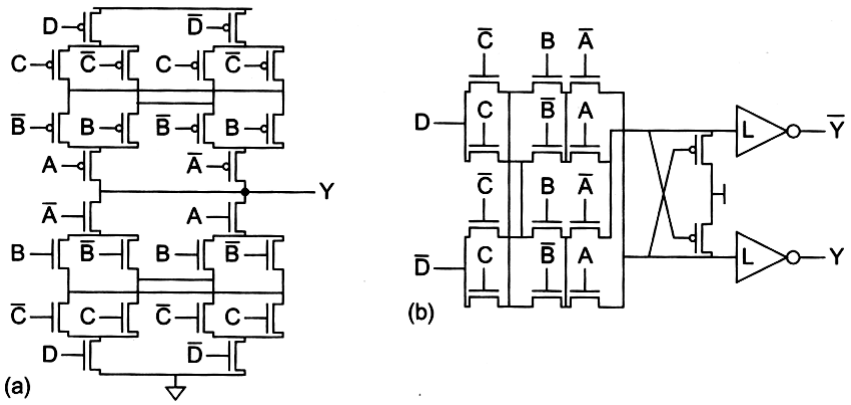
XOR-2 alternatives



[Weste/Harris]

AB=00→$V_{out} = |V_{TP}|$

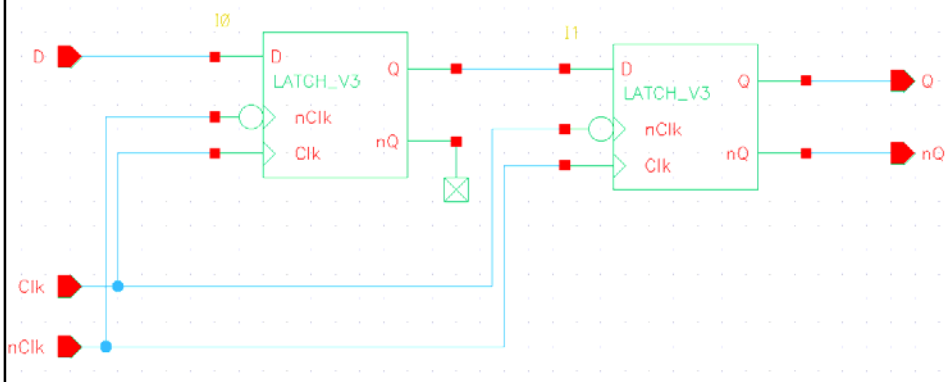
XOR-4 alternatives



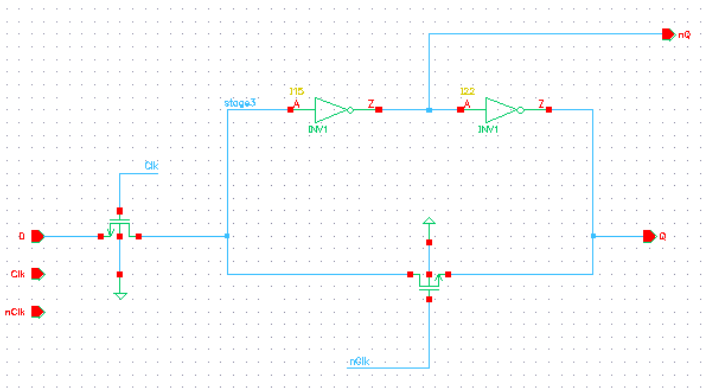
[Weste/Harris]

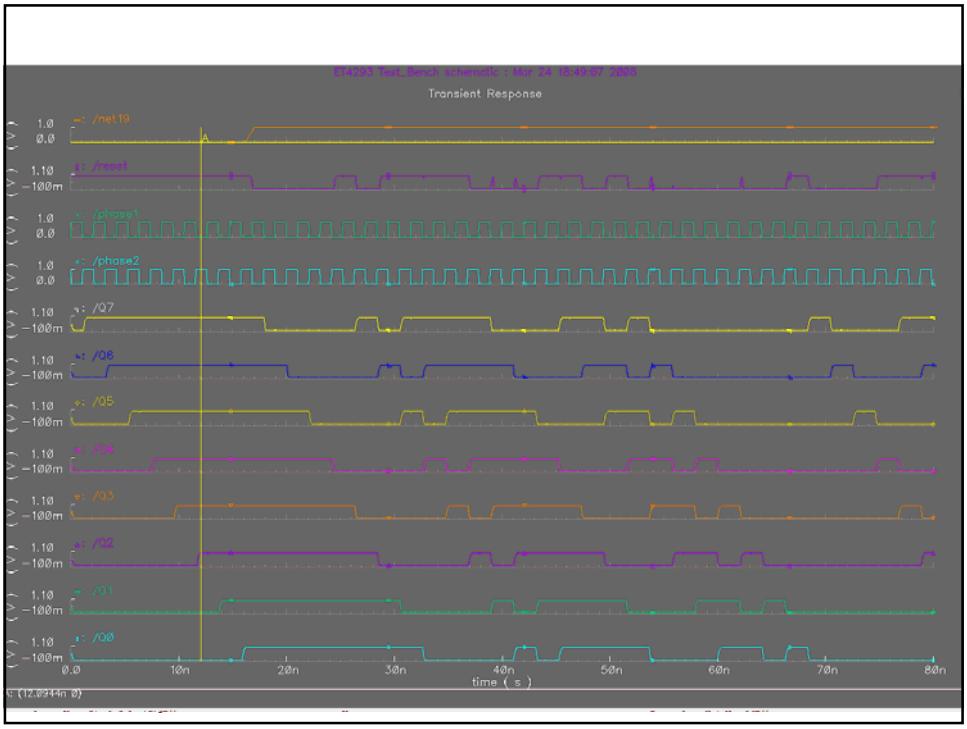
- Can be more compact, not necessarily faster than xor2

DFF


I0
I1
D
LATCH_V3
nClk
Clk
Q
nQ
D
LATCH_V3
nClk
Clk
Q
nQ
Q
nQ
Clk
nClk

Latch


nQ
stage3
I15
A
Z
INV1
I22
A
Z
INV1
Clk
Q
Clk
nClk
Q
nClk


Transient Response
/net19
/reset
/phase1
/phase2
/Q7
/Q6
/Q5
/Q4
/Q3
/Q2
/Q1
/Q0
1.1Ø
−1ØØm
1.Ø
Ø.Ø
Ø.Ø
1Øn
2Øn
3Øn
4Øn
5Øn
6Øn
7Øn
8Øn
time (s)

?