Assignment due Wednesday Feb. 25

Virtuoso Layout Design

- Draw a PMOS transistor using Virtuoso
- Make sure it is DRC correct using Calibre
- Hand-out will be posted on web, printed copy to be made available from secretariat (Laura Bruns, 17.100)

Assignment due Monday Mar. 4

Schematic Driven Layout

- Design a symmetrical inverter using Schematic Composer and Spectre Simulation
- Design Layout using Virtuoso Analog Design Environment (Schematic Driven Layout)
- Hand-out will be posted on web, printed copy to be made available from secretariat (Laura Bruns, 17.100)

Assignments need to be Checked

- You need to complete the assignments
- No grading – just pass/fail
- Pass/fail will be easy decision
  - a serious attempt counts as pass,
    not needed to have everything exactly correct
    and optimal (but it can give you satisfaction)
  - We will try to give feedback, so that you know
    what is OK and what needs improvement
- See TA when you are done ☺
  - Or when you are stuck ☹