

Module 2: Process

Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

Outline

- CMOS Processing
 - Wafer Production
 - CMOS Process Outline
 - Photolithography
 - Material Deposition & Removal
 - Oxide Growth & Removal
- Layout Design
 - Layer map
 - Layout examples
 - Stick diagrams
- Design Rules
 - Only very briefly

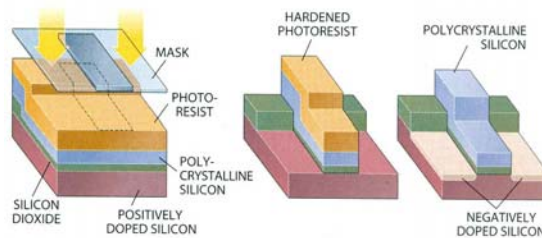
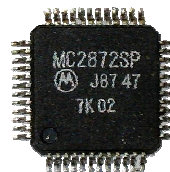
CMOS Processing

- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

IC Technology

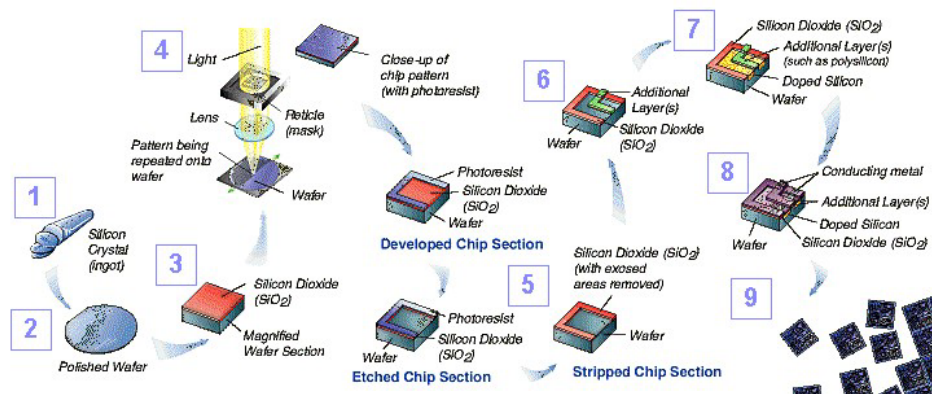


- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist



Multiple cycles, 100's STEPS in total

Another Overview of Semiconductor Processing



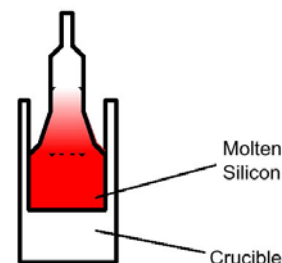
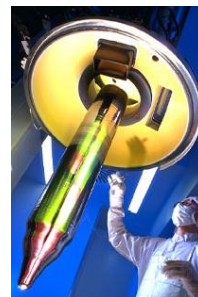
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Wafer Processing – Czochralski Method

- Start with crucible of molten silicon ($\approx 1425^\circ\text{C}$)
- Insert crystal **seed** in melt
- Slowly rotate/raise seed to form single crystal **boule**
- After cooling, slice boule into **wafers** & polish

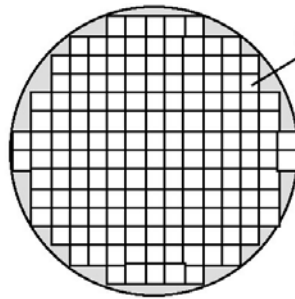
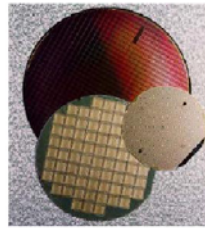


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Wafer Structure



Die - Single IC chip



**300 mm
wafer
(sematech)**

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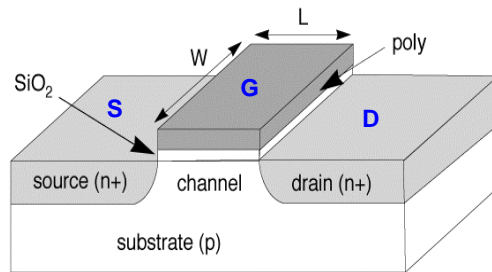
CMOS Process Outline

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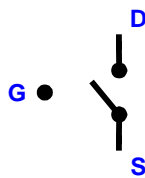
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MOS Transistor



Position of switch depends on gate to source voltage



V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

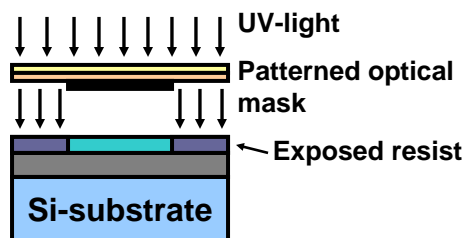
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How Patterns on a Chip are Created

- Basic Principle: **Photolithography**
 - Like **projecting an image** through a photographic negative (or positive)
- Coat wafer with **Photoresist**
- **Shine UV light** through glass mask
- **Develop**: dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")

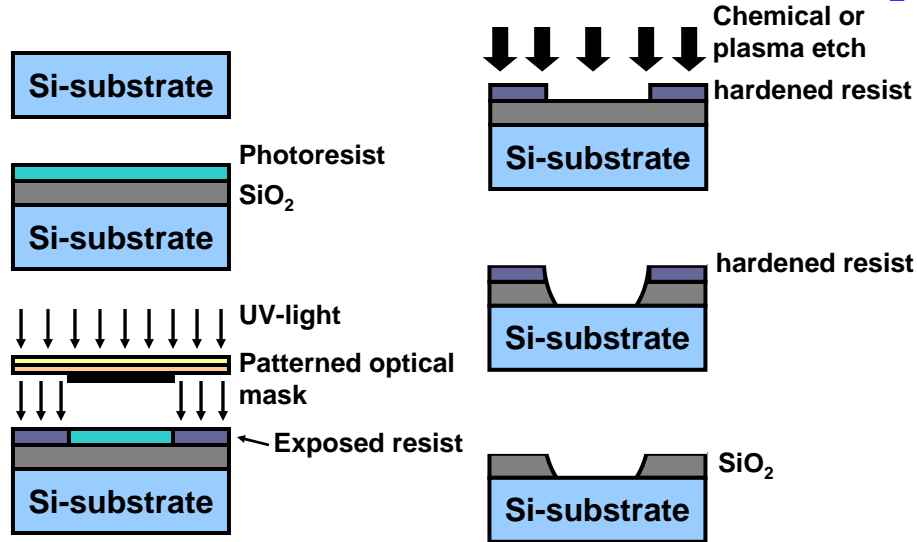


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Example: Etching Step, opening of SiO_2



Etching is for removal of material, similar masking principles for deposition (adding of material)

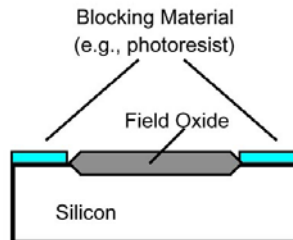
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Oxidation

- SiO_2 formed by oxidation
 - Wet oxidation: heat with water (900°C - 1200 °C)
 - Dry oxidation: heat with pure oxygen (1200 °C)
- Oxide occupies more volume
- Alternative: deposition



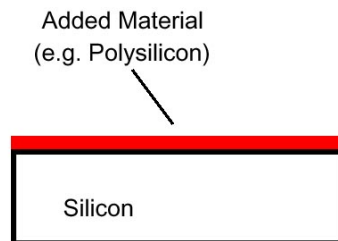
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Adding Materials

- Add materials on top of silicon
 - Polysilicon
 - Metal
 - SiO_2
- Methods
 - Vapor deposition
 - Sputtering (Metal ions)



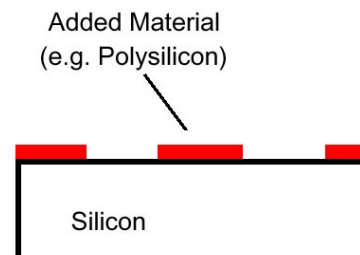
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Patterning Added Materials

- Add material to wafer
- Coat with photoresist
- Selectively remove photo resist (PR), after exposure through mask
- Remove unprotected (by PR) material
- Remove remaining PR



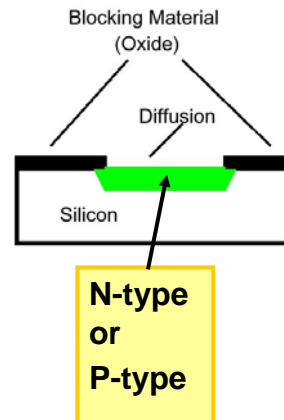
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Diffusion

- Modify electrical properties of Si:
 - **N-type** (extra electrons)
 - or **p-type** (fewer electrons \Leftrightarrow extra holes)
- Introduce **dopant** via epitaxy or ion implant e.g. Arsenic (N), Boron (P)
- Allow dopants to **diffuse**
- Block diffusion in selective areas using oxide or PR (photo-resist)
- Diffusion spreads both vertically, horizontally



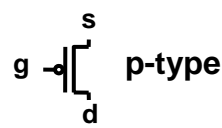
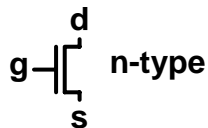
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CMOS – Complementary Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



- | | |
|--|--------------------------------------|
| ■ “on” when V_g is high | ■ “on” when V_g is low |
| ■ With n-type s/d | ■ With p-type s/d |
| ■ Electrons (n) as carrier | ■ Holes (p) as carrier |
| ■ Built in p-type Si | ■ Built in n-type Si |



n-well (for PMOS) in p-type substrate (for NMOS)

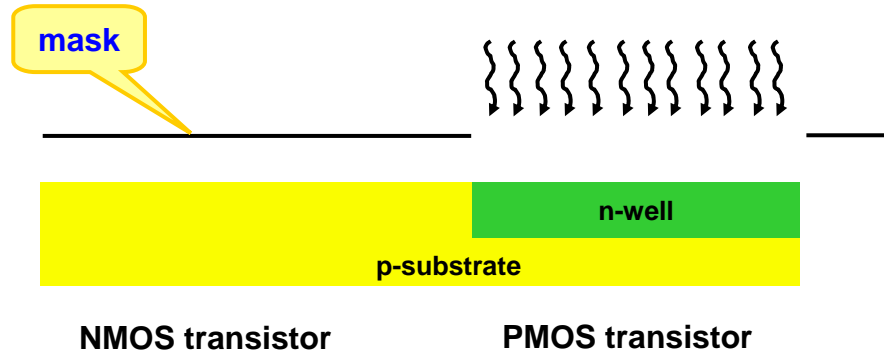
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Outline of Process Flow

First place **n-well** to provide properly-doped substrate for n-type, p-type transistors :

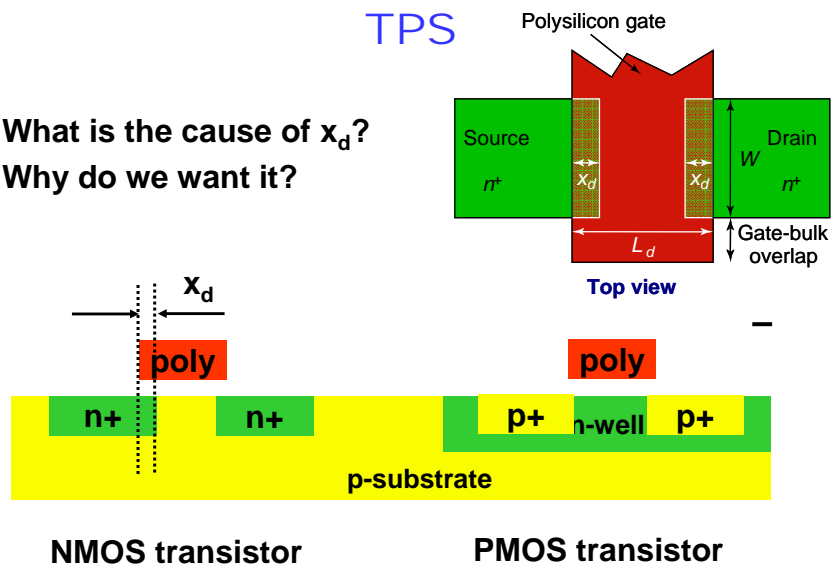


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- What is the cause of x_d ?
- Why do we want it?



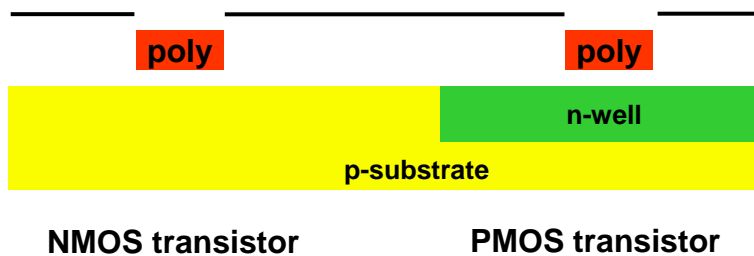
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Outline of Process Flow, cont'd

Pattern **gate** next, to later act as a mask for source and drain diffusions:



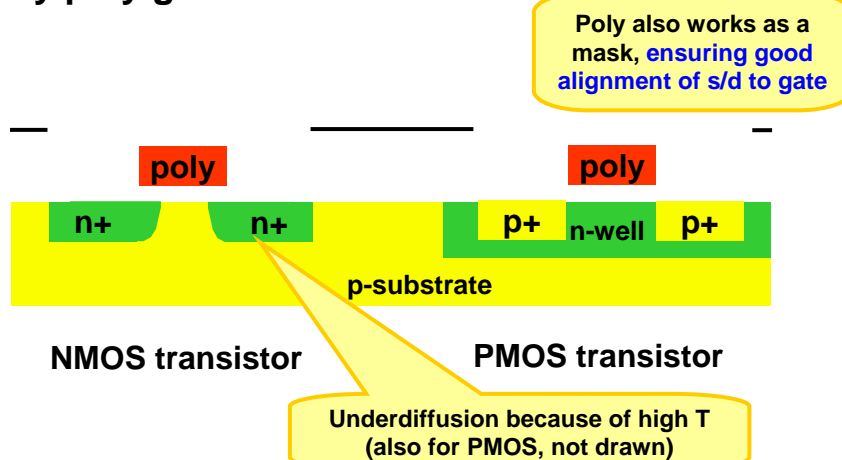
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Outline of Process Flow, cont'd

Add **s/d diffusions**, performing self-masking by poly gate:



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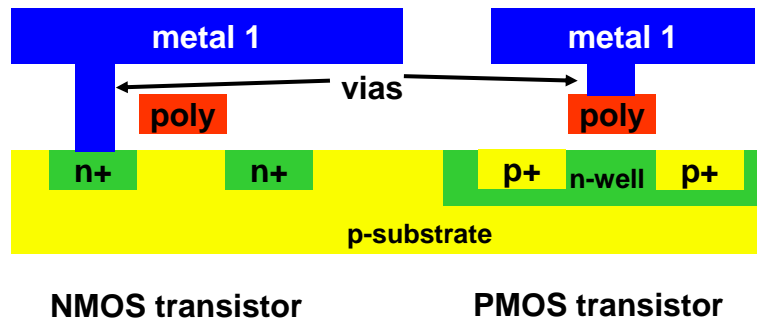
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Outline of Process Flow, cont'd

Start adding **metal layers**:

Via: contact hole between metal layers



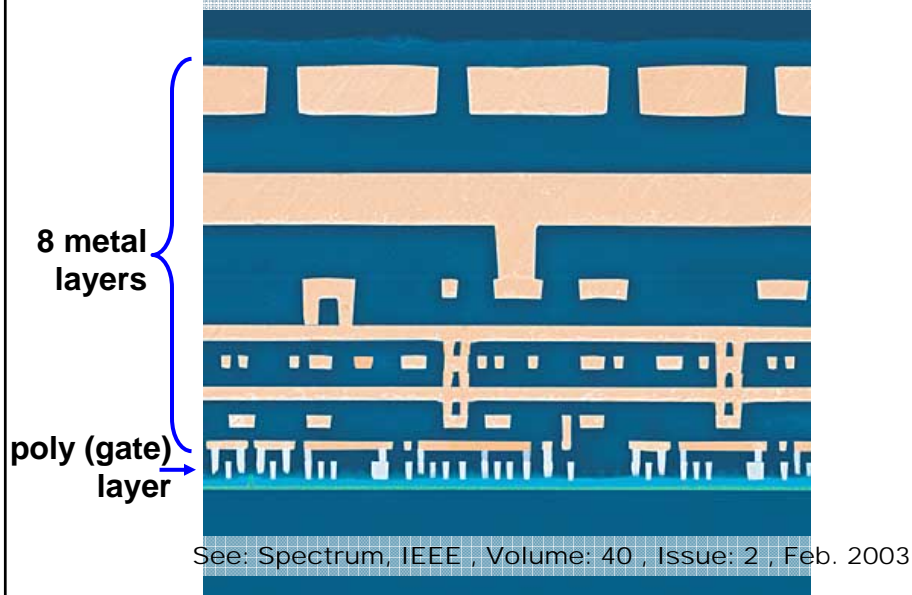
Similar for subsequent metal layers

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Cross-section of IBM CU process



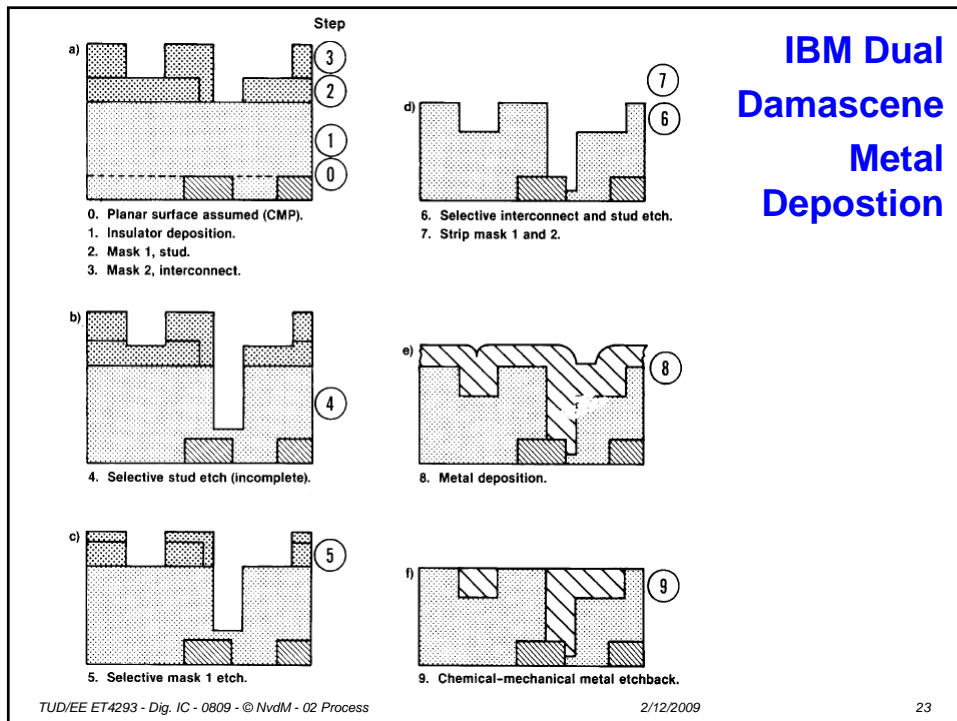
See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

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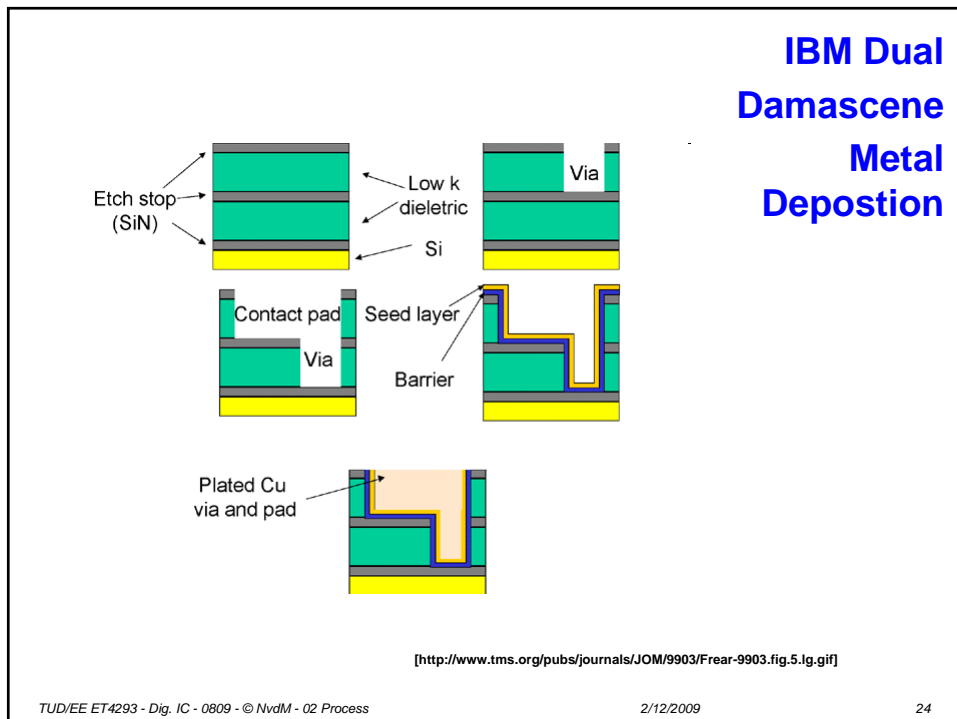
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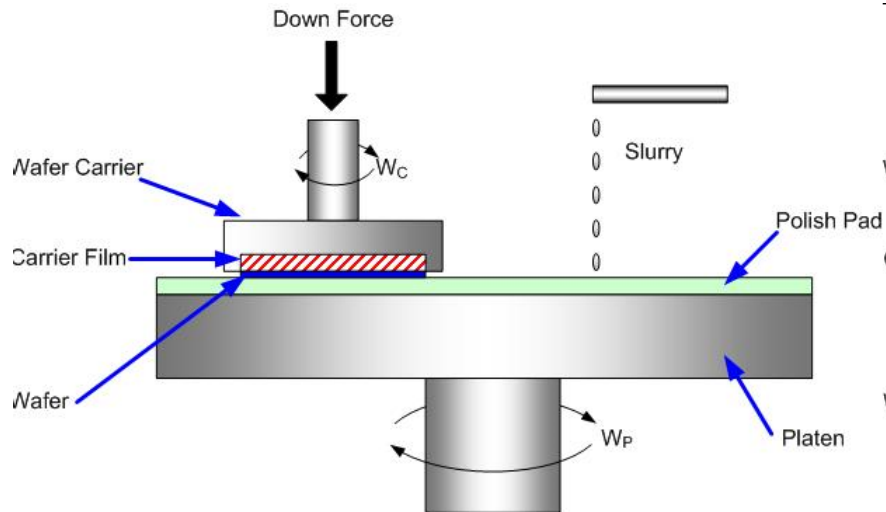
IBM Dual Damascene Metal Deposition



IBM Dual Damascene Metal Deposition



CMP – Chemical Mechanical Polishing



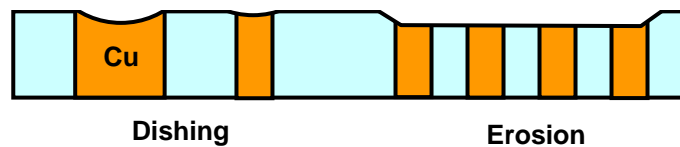
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Metal CMP Variability Effects

- Systematic, layout-process interaction
- Die-level
- Effect can be modeled with 'local layout density' concept
- (Effective) metal height
- Density function from selectivity of chemical polishing combined with mechanical/chemical 'protection' from dielectric
 - Wide metal sensitive to thinning
 - Narrow dielectric sensitive to erosion

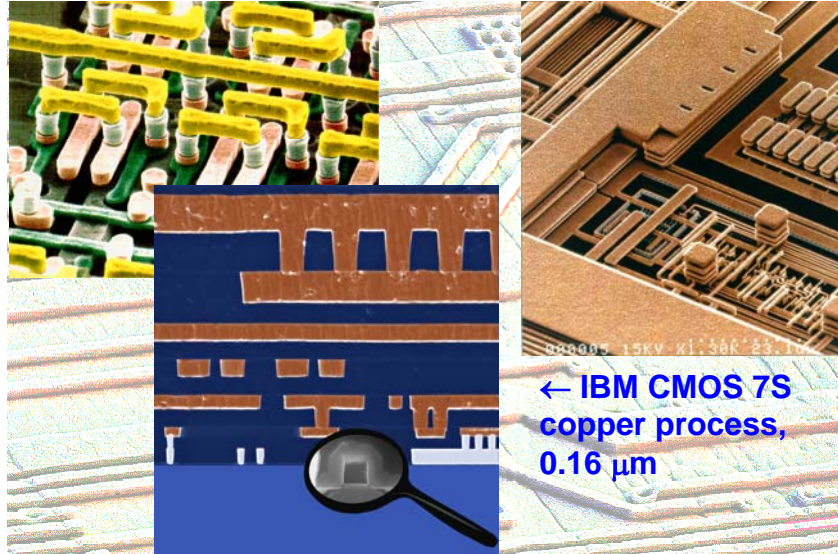


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Interconnect Examples (motorola, ibm)



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IC Recipe Precisely Fixed

- Process conditions (temperature, time, concentration, ...) **very critical**
- Many **strong compatibility** issues of materials and processes
- Very expensive and **difficult to tune**
- Very expensive **equipment** and facilities
- Need **Billions** of turnover for break-even

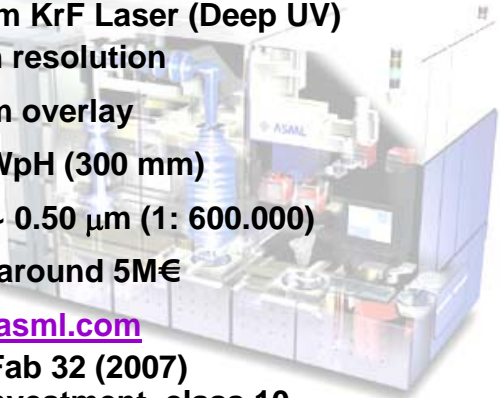
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Complex Lithographic Process

- Example: ASML TWINSKAN™ XT:1250
- Sub wave length Lithography
193 nm KrF Laser (Deep UV)
- 65 nm resolution
- < 8 nm overlay
- > 85 WpH (300 mm)
- DOF ~ 0.50 μm (1: 600.000)
- price around 5M€
- www.asml.com
- Intel Fab 32 (2007)
3B\$ investment, class 10



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Compare Stepper Wafer Size and Resolution to NL scale

- Wafer size: \varnothing 300mm
- Resolution: 65nm
- Netherlands: 40.000 km² ~ 200km x 200km

300mm	1	65nm
200km	667x10 ³	4.3cm

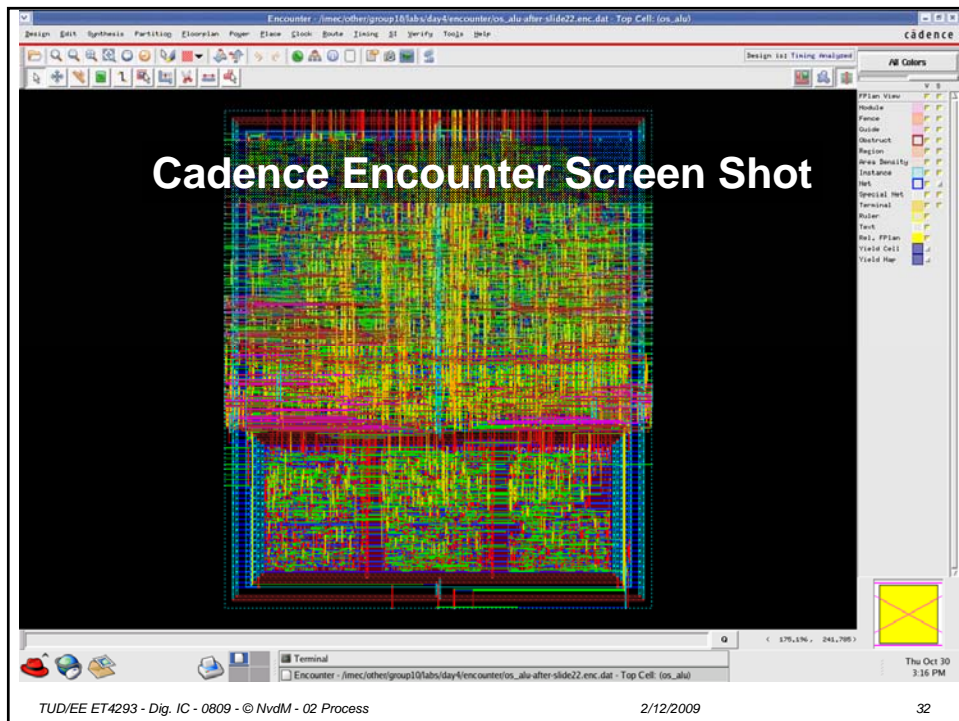
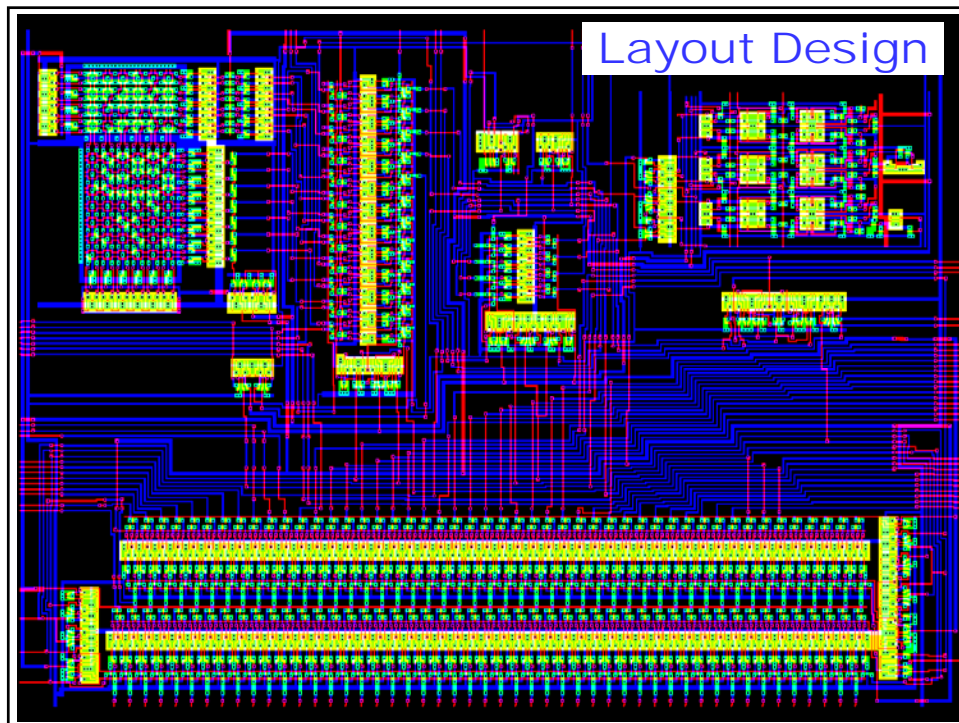
A 'magnified' waferstepper could 'print' the Netherlands with a resolution of 4.3 cm in 42 sec.

Better than a 52.5 terabit camera
~ 10 Million 5 megapixel cameras (B/W)

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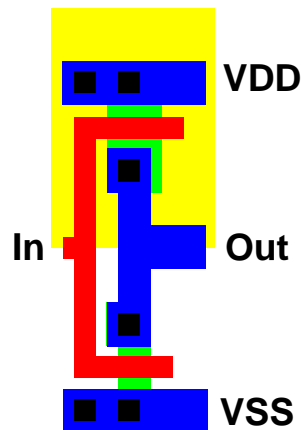
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Layout Design

Layout Design Concepts

- Layer map
- Layout examples
- Stick diagrams



You should be able to understand such a drawing as well as simpler drawings called 'stick diagram'

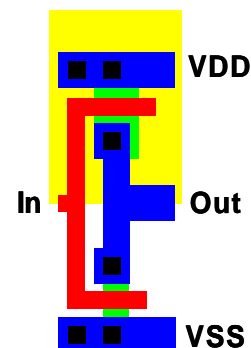
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Layout Design

- Layout is design of **fabrication masks**
- Each mask is drawn in **different color**
- Layout is not a free-form drawing
 - Most often: **Manhattan Layout** (rectangular)
 - Sometimes 45-degree angles
 - Curved geometry only for special applications
- Layout should obey **Design Rules**



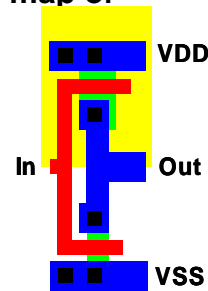
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Layer Map

- **Layers** are assigned **colors** and/or **patterns**, not always 1 to 1
- Is a matter of **convention**
- Site-dependent, process dependent, tool dependent
- Be prepared to **reverse-engineer** layer map of **unknown layouts**



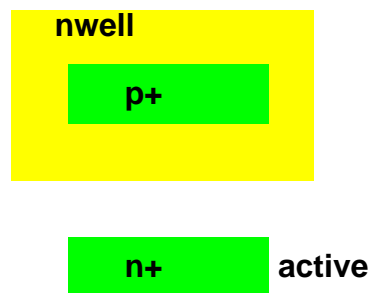
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Polarity of Active Area

- **Active layer** or active area is the source/drain implant layer (area). Usually abbreviated as '**active**' only.
- Normally, a so-called **select** mask determines polarity of **active**
- See color plate 5
- Many simplified drawings only show subset of the masks
- Rest should be clear from context

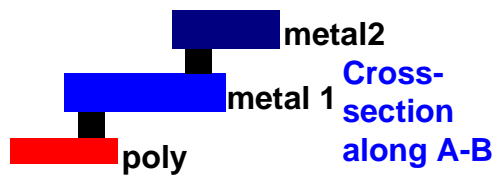
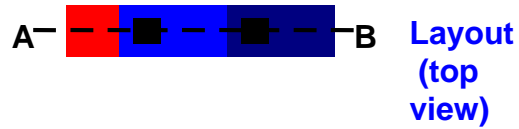
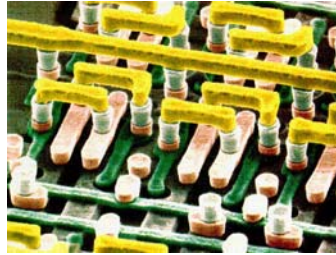


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Contact Holes and Vias



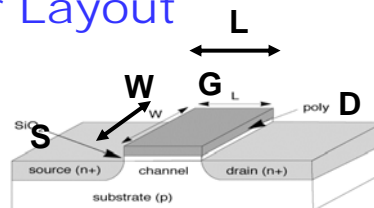
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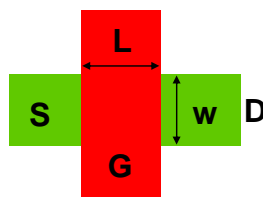
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Transistor Layout

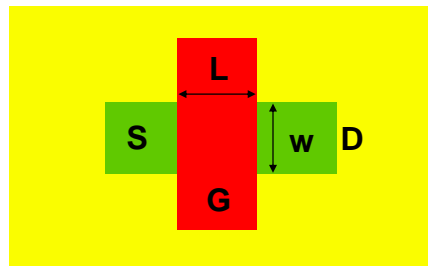
n-well (p-sub)



n-type



p-type











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Simplified CMOS Layer Map






■ Compare to / instead of colorplate 1.

yellow		nwell – place for P-transistors
pink		select – invert polarity of active
green		active – source and drain regions
red		polysilicon – gate material
blue		metal 1 – first interconnect metal
dark blue		metal 2 – second interconnect metal
magenta		metal 3 – third interconnect metal
black		contact, via – hole in interlayer oxide

■ **Note:** active = active area = diff = diffusion, well \approx tub

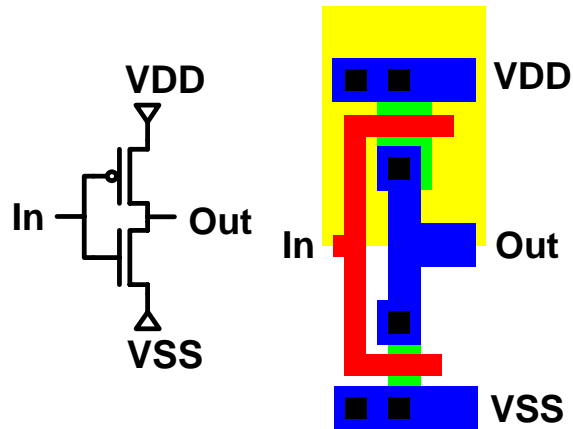
Further Simplified CMOS Layer Map

■ Compare to / instead of colorplate 1.

yellow		nwell – place for P-transistors
green		active – source and drain regions
red		polysilicon – gate material
		metal 1 – first interconnect metal
black		contact, via – hole in interlayer oxide

■ Or equivalent B/W patterns

Inverter Layout



Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

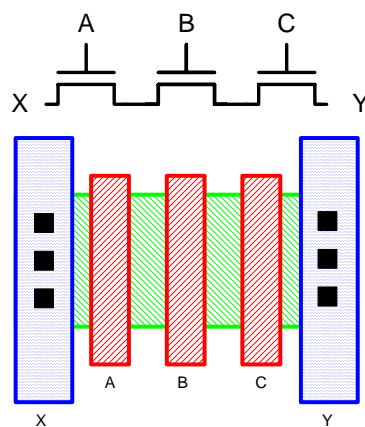
Be able to draw such layouts (but more complex) (coming weeks) and reverse engineer (decode) them

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From Schematic to Layout



Transistor schematic

Layout

- Active
- Poly Si
- Metal 1
- Contact

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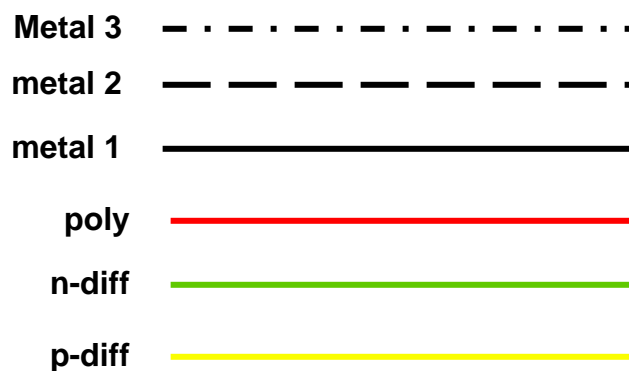
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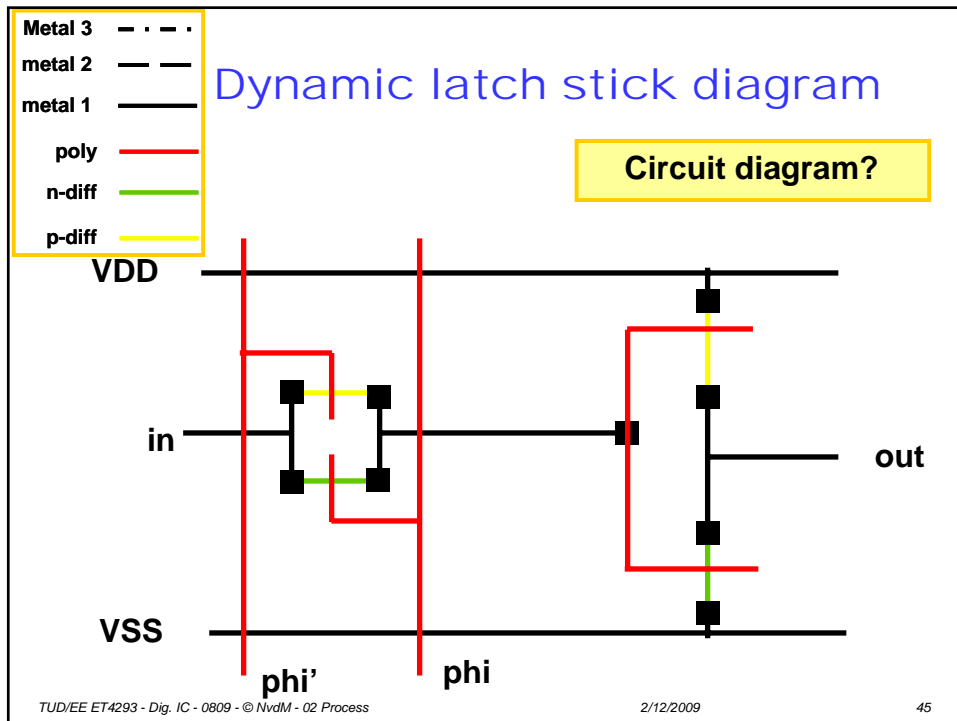
Stick diagrams

- A stick diagram is a **cartoon** of a layout.
- Does show components/vias but only **relative placement**.
- Does **not** show **exact placement**, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.

Stick layers



- **Caution:** stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff



Exercise

See transistor layout below.
 Determine for each of gate, source, drain which regions A-E (see the layout) form this terminal.

G:
 S:
 D:

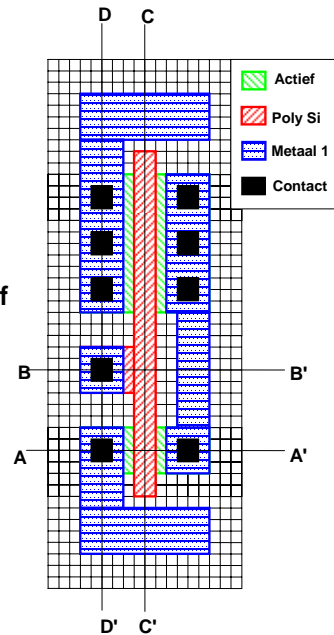
Draw a cross-section through a-a' en b-b'

Legend:
 Actief (n): - - - (green)
 Poly Si: - - - (red)
 Metaal 1: - - - (blue)
 Contact: - - - (black)

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See the CMOS inverter layout on the right

- Draw cross-sections A-A', B-B' and C-C'
- Which of the 2 transistors must be the P-transistor? Why?
- Draw the corresponding N-well.
- Annotate in the layout the location of the VDD and VSS terminals.
- Draw the schematic, including L and W ratios.



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Design Rules



















- The fabrication process will suffer from **tolerances**
- Chip features will have a practical **minimum size** to allow them to be fabricated reliably enough (with high enough **yield**)
- This is captured into a set of precise **Design Rules**
- Modern processes have terribly complex set of design rules as a compromise between **flexibility** and **manufacturability**
- Need to work with those rules during cell layout.

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Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal					
	m1	m2	m3	m4	m5
well					
	nw				
polysilicon					
	poly				
contacts & vias					
	ct	v12,v23,v34,v45	mwc	pwc	
active area and FETs					
	ndif	pdif	nfet	pfet	
select					
	nplus	pplus	prb		

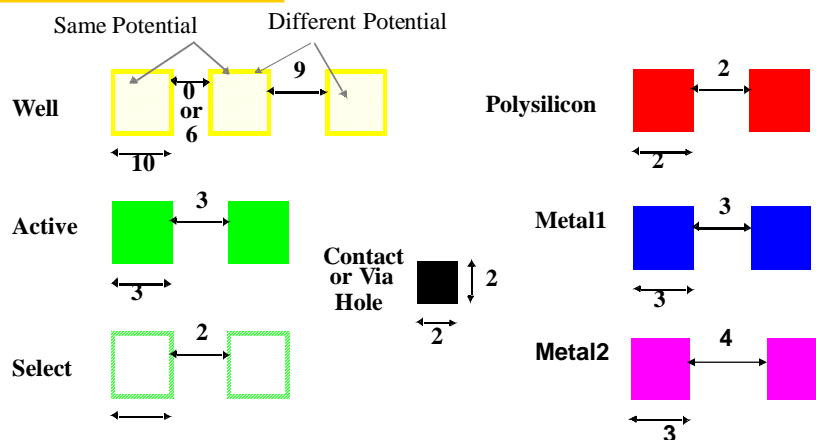
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Intra-Layer Design Rules

Example Rules

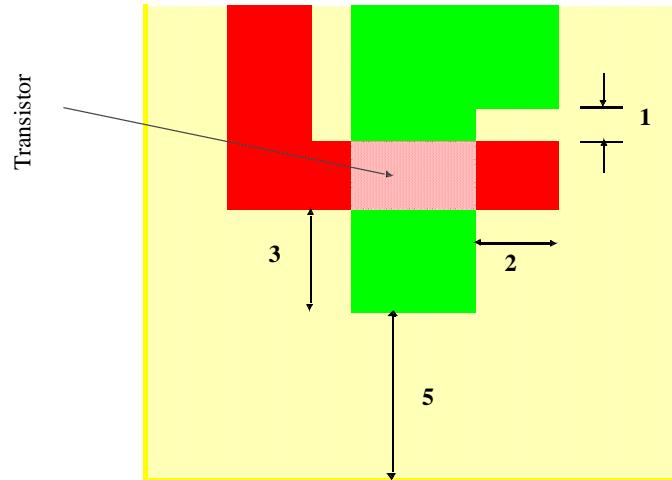


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Transistor Layout

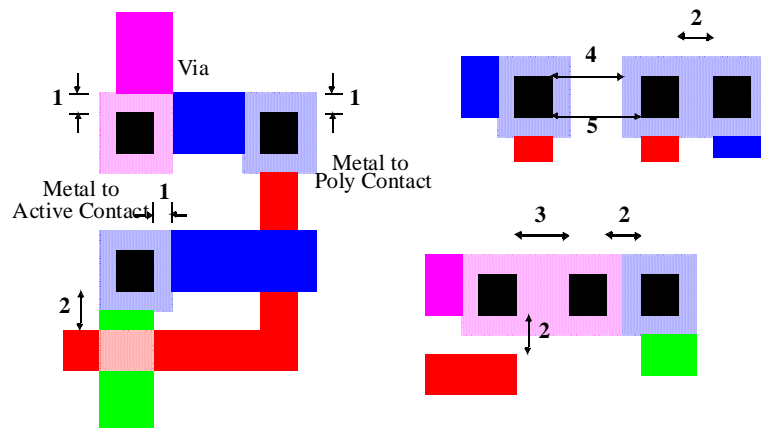


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Vias and Contacts

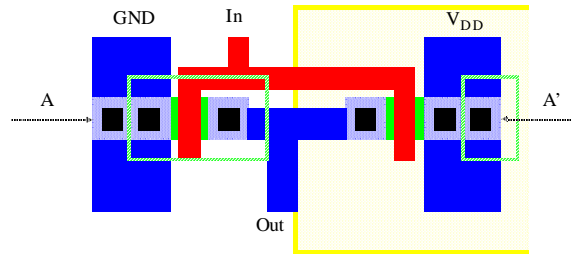


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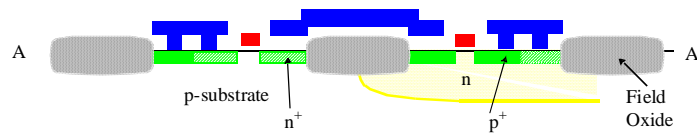
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Inverter Layout and Cross-Section



(a) Layout



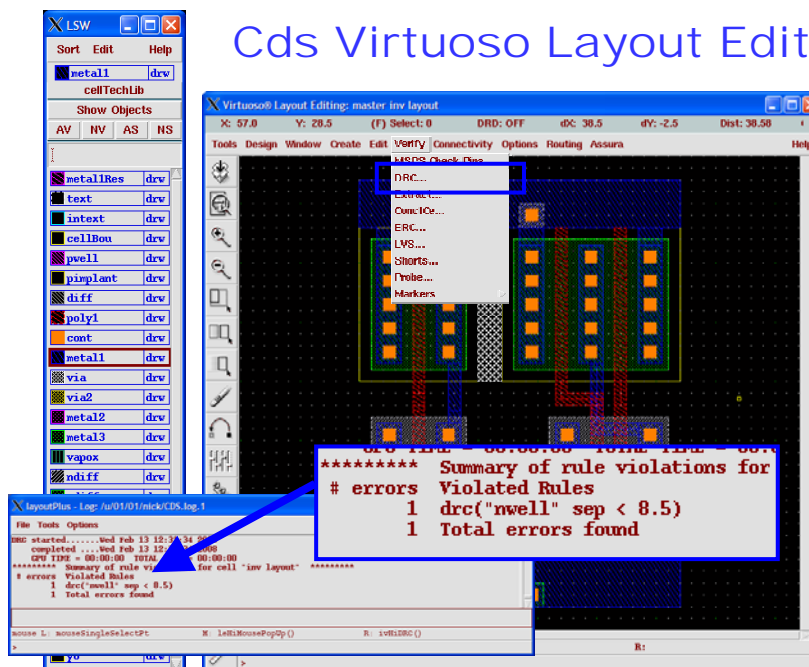
(b) Cross-Section along A-A'

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Cds Virtuoso Layout Editor



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Summary

- CMOS Processing
 - Photolithography
 - Material Deposition & Removal
 - Oxide Growth & Removal
- CMOS Process Outline
- Layout Design
 - Layer map
 - Layout examples
 - Stick diagrams
- Design Rules
 - Why we need design rules