Virtuoso Layout Design

The basic steps of using the Cadence layout editor called Virtuoso will be covered. Some excises are beneficial to gain a deeper insight into fabrication process. This document is supposed to be a general overview of tool for beginners who didn't design any layout before. The fundamental steps to design a PMOS device are used as an example.

1. Set up the design environment

Before starting, you should add the library named "**UMC090**" to your cds.lib file in your working directory and copy the display.drf file to your working directory, and then create your library in your working directory. Preparing work is listed below:

1. create your working directory and copy some files
   >cd /users/username
   //go to the directory (you can select it, it's up to you!) where you want to create your working directory
   >cp –a /opt/cad/cadence/5.1.41/sun4v/IC5.1.41/tools.sun4v/dfII/samples/tutorials/le/cell_design .
   //copy cell_design to the current directory and then use it as your working directory. Do not forget the "." at the end of command line.
   >cd ./cell_design
   Note: Following steps will be operated in this directory
   >cp –a /opt/cad/cadence//5.1.41/sourceme .
   >cp –a /opt/cad/DesignKits/UMC090/designkit/display.drf .
   >vi cds.lib
   //cds.lib is an important file which specifies library information. At beginning, we are going to add library 'UMC090'. After vi cds.lib *(you can use* emacs *if you like)* you will read the cds.lib, press 'i' key to edit it, add the sentence:
   'include /opt/cad/DesignKits/UMC090/designkit/cds.lib'.
   After that, press "Esc" to quit edit mode and then type :wq

2. open ICFB
   >source sourceme //you have copied sourceme file to your working directory, so you can source it in your working directory.
   >icfb & //Now cadence is activated by command 'icfb &' and a **CDS.log** window (Fig 1) pops up.

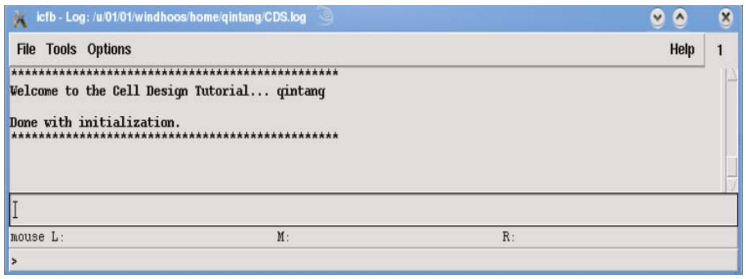

Fig 1 CDS.log window of icfb

3. create your library
   Start "library manager" (**Tools->Library Manager**), then create your own library by clicking **File->New->Library.**
   Note: your library should be attached to the existing library UMC090.

4. start layout design
   Click your new library, follow these steps: **File->New->cell view**, a window like Fig 2 will pop up:

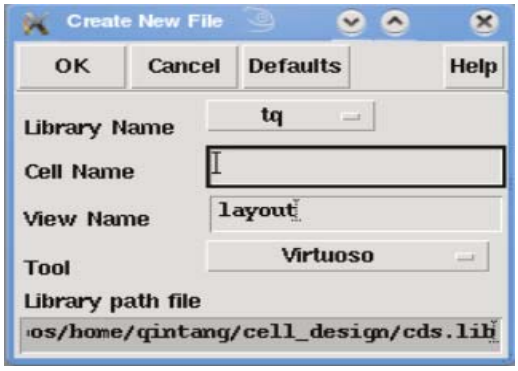

Fig 2 Create New File

Write down the cell name, and choose '**Virtuoso**' as Tool. Click **OK** and then the Virtuoso Layout Editing window will pop up along with a **LSW window**, shown in Fig 3. Description of various mask layers can be found at:

/opt/cad/DesignKits/UMC090/designkit/stream.map

Now you can start your layout design!

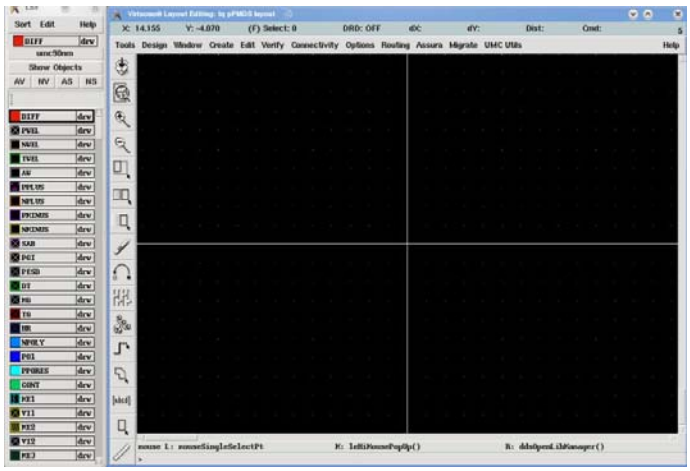

Fig 3 Layout Editing and LSW window

2. Layout Design

The first thing you should do to start the layout is fix the grid sizing. Go to **Options->Display** or **press e key** which is the shortcut for that, the options window (Fig 4) will pop up. The **X/Y Snap Spacing** parameter is a foundry limitation resulted from the ability to place masks on the wafer, if you make a smaller grid, probably when you check DRC of the layout you will find lots of errors about 'offgrid', if you don't correct this errors the foundry will refuse your fabrication order. The default value 0.005 is fine. Click **OK** to save your modification or just keep the defaults.

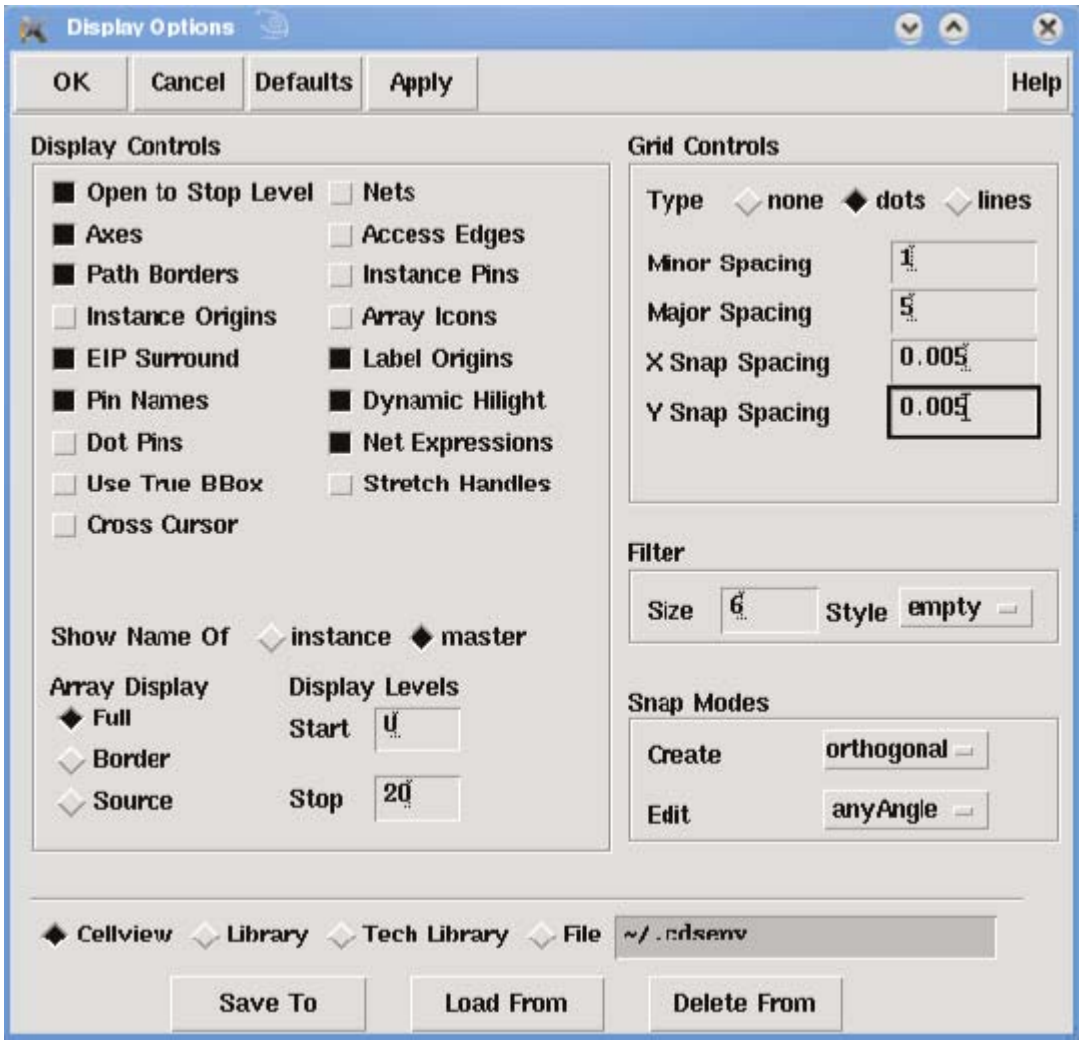

Fig 4 set options for layout design

Then we go back to the Virtuoso Layout Editing window (Fig 3). In the left column window, you can see the icons for **Save, Fit Edit, Zoom in, Zoom out, Stretch, Copy, Move, Delete, Undo, Properties, Instance, Path, Polygon, Label, Rectangle and Ruler**. You will use them frequently during designing. The short-cut keys listed below will help you work faster. Take **r** as a case, before you draw any layer, you should select corresponding layer from the **LSW** palette window, click it then move the cursor to **Virtuoso Layout Editing** window to left-click so as to activate it. Press **r** on the keyboard or click the icon for **Rectangle**, sequentially left-click and drag the mouse

pointer to define the range. After drawing, ***do remember to press Esc to exit this mode***. Detailed explanations for these commands are listed after shortcut-key Tips.

Tips:

- **r** to Create Rectangle
- **m** to Move
- **s** to Stretch
- **p** to Create Path
- **u** to Undo
- **c** to Copy
- **k** to ruler
- **Q** to show property
- **i** to add instance
- To zoom in on the schematic, hold **right-button** mouse to create zooming area and release to zoom in.
- To zoom out, press **Shift+z**
- To fit whole schematic on screen, press **f** (the shortcut key for **Fit Edit** icon)

Edit Menu

- **Rectangle**: creates a rectangle of the layer selected in the LSW.
- **Move**: click on any object and move it around in the layout.
- **Stretch**: Click on the edge of a rectangle and size it. Be careful during using it. Before pressing **s**, make sure no object is selected; otherwise the selected object in your previous step will be moved unexpectedly.
- **Path**: Creates a path of the layer selected in the LSW. ***Double click to end the path.***
- **Undo**: undo the previous commands.
- **Copy**: Create a copy of any object in the layout.
- **Properties**: Change the properties of objects in the layout. Change the layer definitions and the changes are immediately reflected in the layout.
- **Instance**: used to import another existing cell view into this cell view.

Let's design a PMOS transistor at first. PMOS is built in Nwell, which is put in the P-type substrate. The black background in **Virtuoso Layout Editing** window can be considered as the P-substrate so NMOS device can be put directly in it while PMOS devices need Nwell. Fig 5 shows the different layers required to build a PMOS transistor. The detailed explanation of PMOS layout design is in the **Appendix** section.

PMOS device is composed of these layers listed below (names are from LSW window):
-----Nwell
-----SDSYM

-----P01 (poly)
-----DIFF (S/D diffusion, active region)
-----PPLUS (S/D P+ implant)
-----DEVICE
-----CONT (S/D contacts)
-----ME1 (Metal 1)

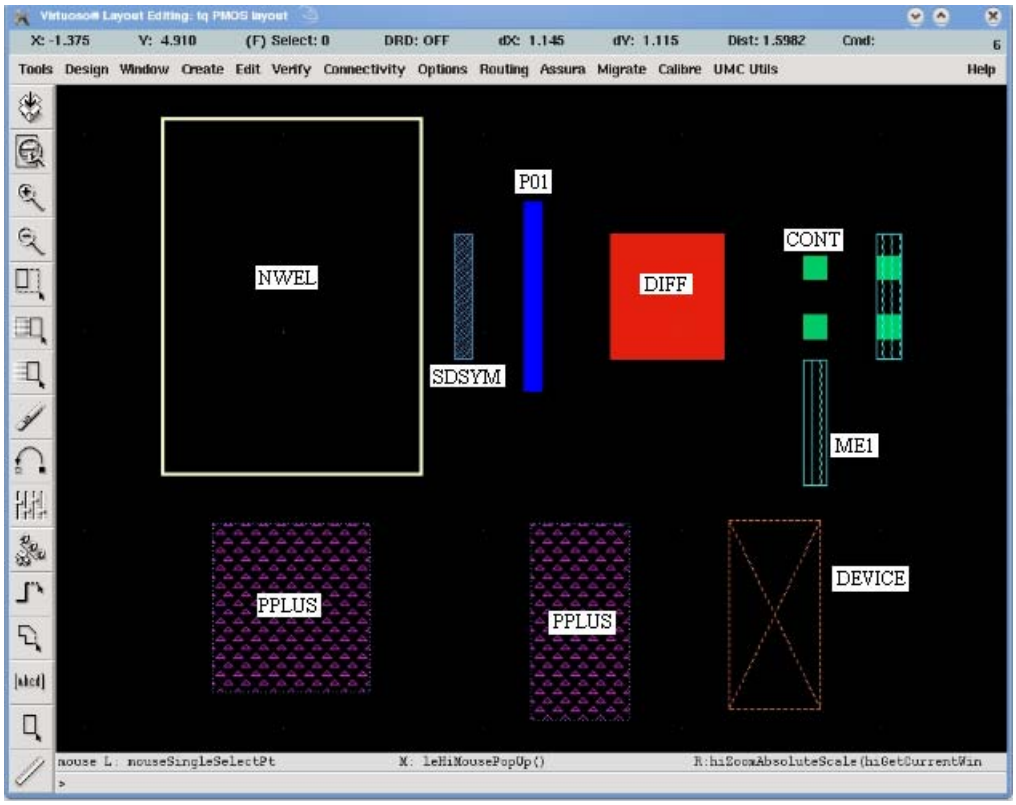

Fig 5 layers for buliding PMOS

The complete layout is shown in Fig 6.

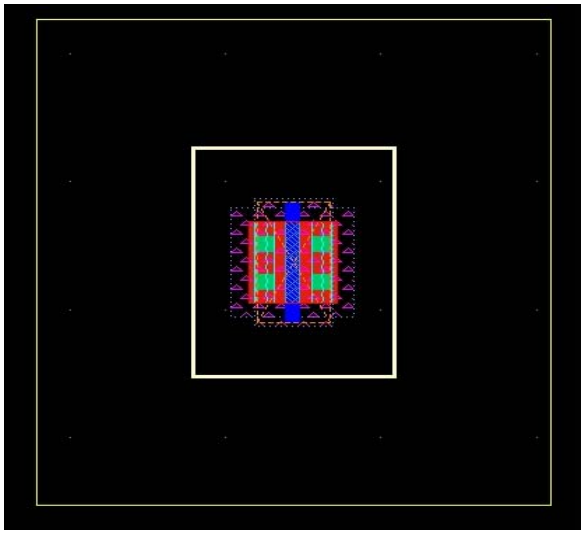

Fig 6 PMOS layout

When you're designing layout, the most important thing you should keep in your mind is the DRC rule. The design rules are specific for particular manufacturing processes,

which set certain geometric and connectivity restrictions to ensure that most of design works correctly. If you don't comply with it, you will face numerous errors and warnings after DRC. That's terrible!

The most frequently used rules are illustrated in **Layout_rules.ppt**. Please read them and refer to them during designing.

Maybe you will ask: there is no N-plus layer to connect Nwell to high voltage, why? Generally designers will design the M1-NWEL and M1-Psub contact models to connect Nwell and substrate to metal respectively. As a result, the PMOS and NMOS models are simplified and compact.

3. DRC<Design Rule Checking>

DRC is available with Cadence distribution which checks most of the rules. The next step following with completing layout design is to run DRC to ensure the designed layout meets rules. There are two methods to run DRC, one is Assura and the other is Calibre. Calibre will be introduced here.

Now you would ask why I cannot find Calibre menu in Virtuoso Layout Editing window?

Yes, you need to edit .cdsinit and sourceme file, then cadence loads those changes and add Calibre. Exit icfb, download these two files from
http://cobalt.et.tudelft.nl/~nick/courses/digic/CadenceLocalGuide.html
to your working directory to overwrite the old ones. And then copy the directory Calibre to your working directory. The last step is not compulsory but it will make simulation more convenient.

```
>cp –a /opt/cad/DesignKits/UMC090/designkits/RulesDecks/Calibre .
// make sure now operation is in your working directory
```

Source sourceme again and restart icfb, you will see **Calibre** menu in your layout if you follow these steps correctly.
Note: .cdsinit is a hidden file; you can read it by command 'cat' in x-term or set up your computer not to hide files.

1. Open your layout, in the Layout Editing window, select **Calibre->Run DRC** to invoke the **Calibre Interactive – nmDRC** window (Fig 7). If this is the first time for you to run DRC, click **Cancel** for Load Runset File. If you saved a runset file before and you want to load it, specify the runset file here. Specify DRC Rule File and DRC Run Directory (set it to your working directory) like Fig 8. DRC Rule File can be found in the directory **Calibre->DRC**.
2. Specify the 'Top Cell' in the **Calibre Interactive – nmDRC** window (Fig 9). If you need to change some DRC switches, you have to edit the Calibre DRC file.

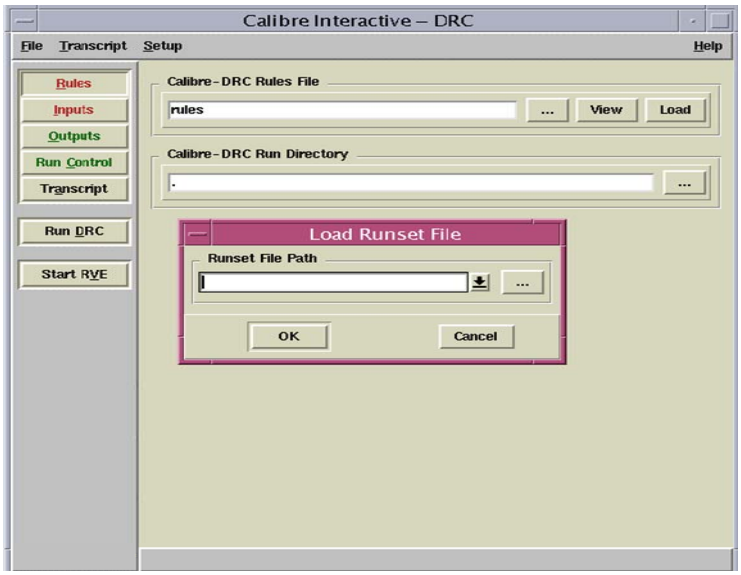

Fig 7 Calibre Interactive – nmDRC window

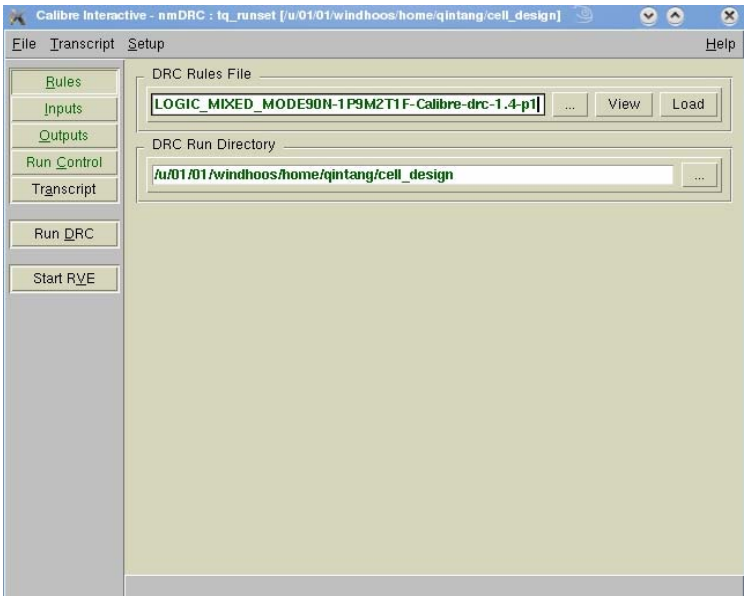

Fig 8 specify DRC rule file and run directory

3. Click **Run DRC** icon on the left of **Calibre Interactive – nmDRC** window. Finally you will have **Calibre – DRC RVE** and **DRC Summary Report** windows with violations as indicated in Fig 10 and Fig 11 respectively.
4. Correct layout according to the errors and warnings in **Calibre – DRC RVE** window (Fig 10). Click errors so as to read errors in the bottom of **Calibre – DRC RVE** window (Fig 10). At the same time, the location of error will be highlighted in the layout. It's easy for you to realize where should be modified.
5. Repeat correcting layout and running DRC until there is no error shown in **Calibre – DRC RVE** window (Fig 10). However, if there are errors like 'Minimum DIFF density over 150m*150um area step 50 is 25%' and 'Maximum P+ diffusion to nearest N+ pick-up spacing is 20um' for your PMOS layout, they could be neglected. The layout checking is finished. The first error arises because it's just a small model. After designing the layout for a whole system, this requirement will

be met. The last error is resulted from NWELL contact. If the

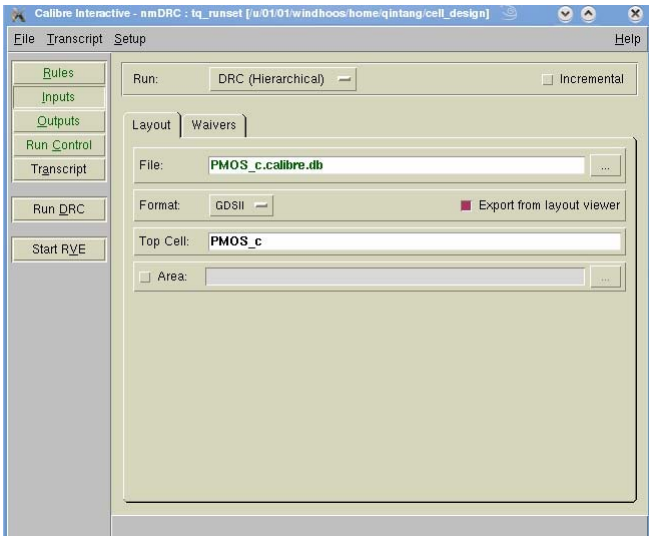

Fig 9 specify the top cell

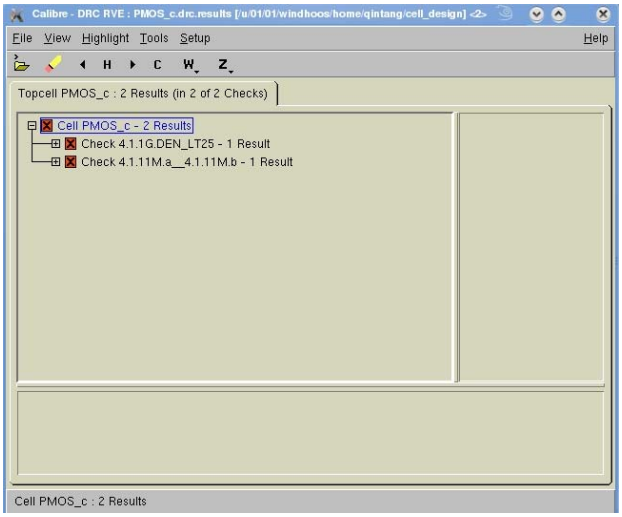

Fig 10 Calibre-DRC RVE window

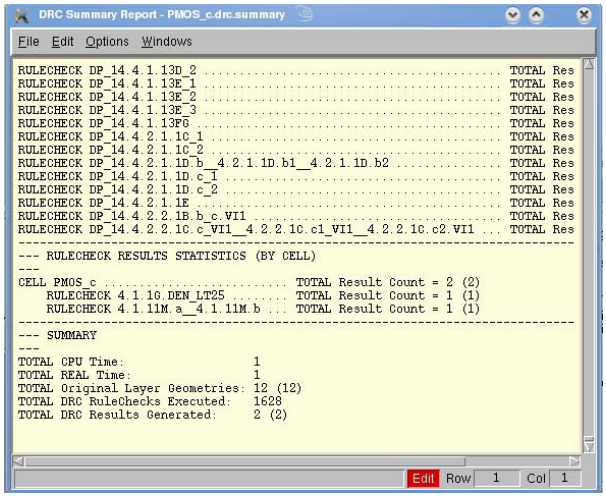

Fig 11 DRC Summary Report

PMOS model is used; there must be an Nwell-Metal contact to connect Nwell to supply voltage, so the last error can be neglected.

The next step is to run LVS (Layout Versus Schematic). Schematic must be matched to corresponding layout.

One example to correct layout according to DRC results

This is an example to indicate how to correct layout in order to make sure everything you place in the layout is compatible with the design rule. I modify the layout (Fig 12). The DRC results are listed in Fig 13. Click **Check 4.1.13C.a-2 Results** and then double-click **01**, you can see the error is highlighted and amplified in **Layout Editing window**. The bottom of **Calibre – DRC RVE** window is the information about the error: *Minimum spacing of DIFF CONT to P01 is 0.08um / P01 with width <= 0.13um*. that's mean the CONT in the left of Poly layer is placed too close to poly, the spacing between them must be at least 0.08um. So the two CONTs on the left are supposed to be moved towards the left.

Then edit the layout, and run DRC again, the result indicates that there are only two errors (Fig 14). As said previously, these two kinds of errors could be ignored.

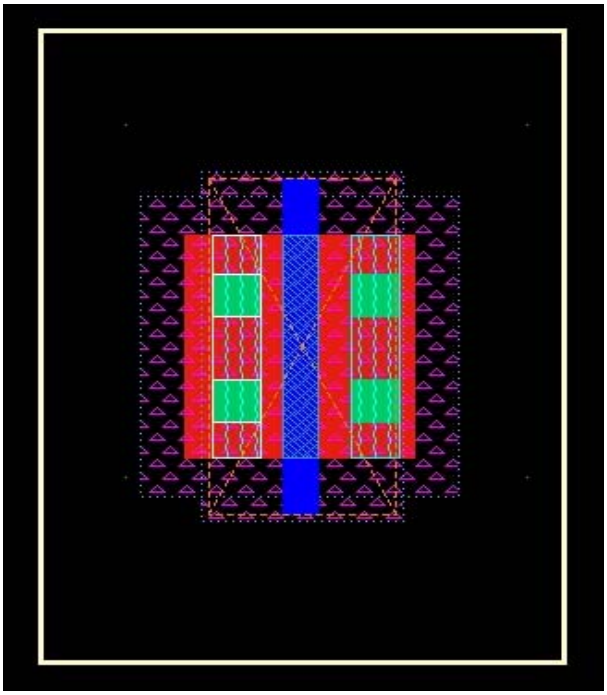

Fig 12 modified layout

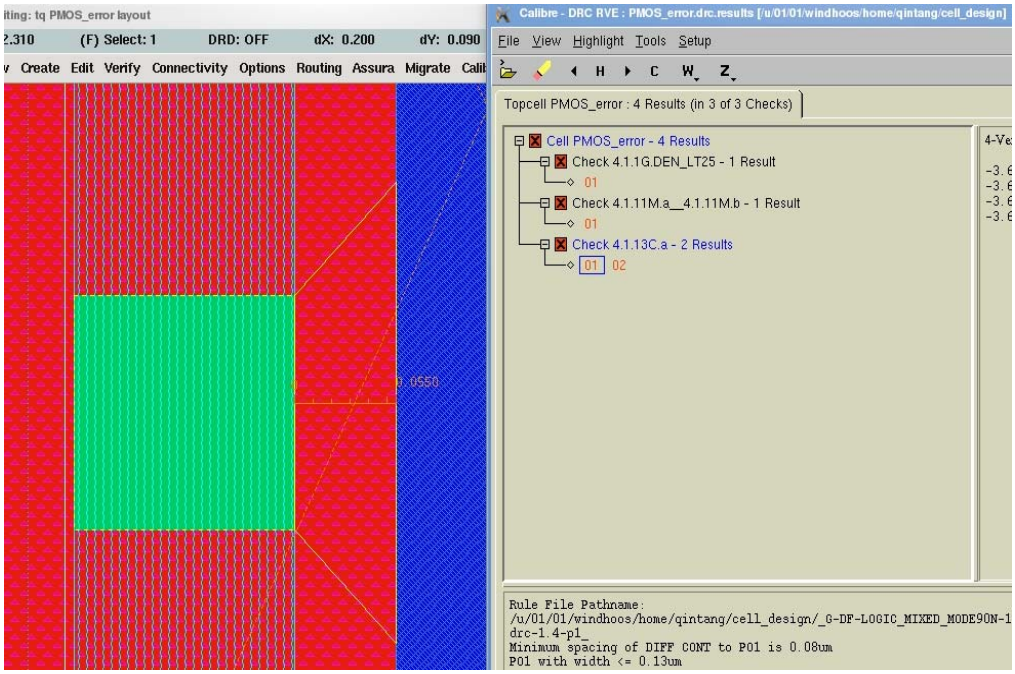

Fig 13 selected error is highlighted

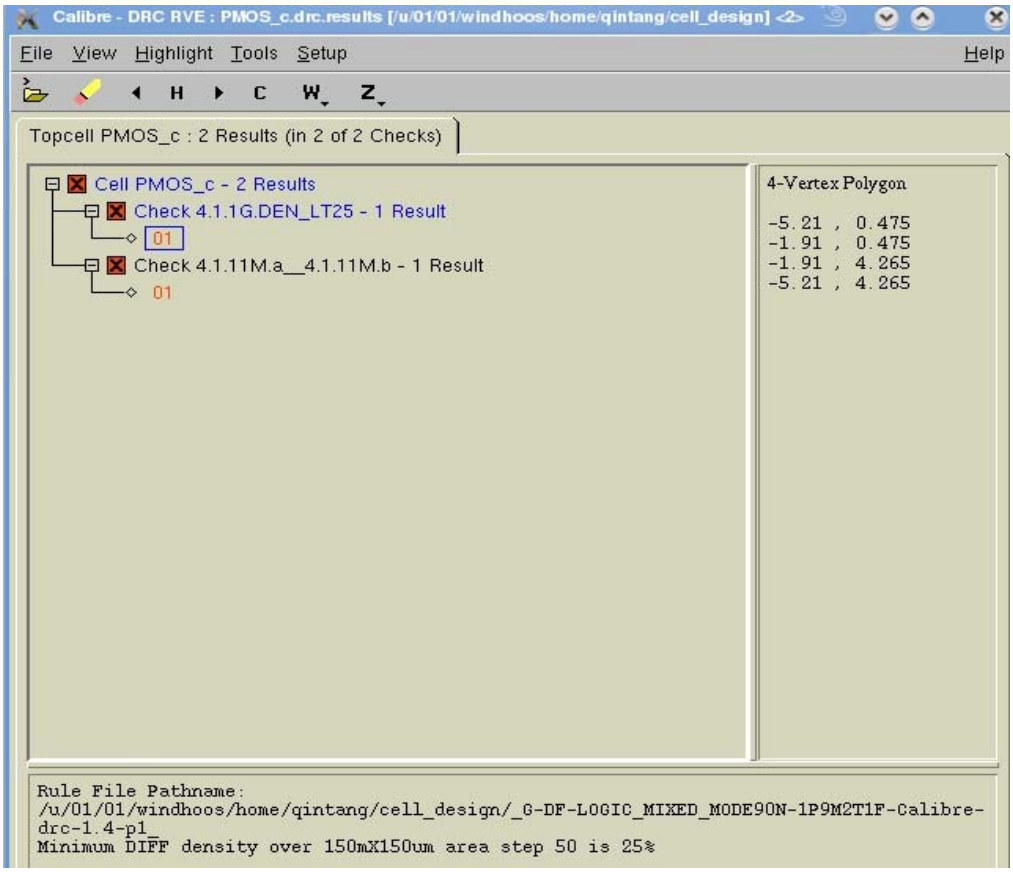

Fig 14 DRC results after correcting

4. The design flow

When you want to design circuits, no matter how large and complicated they are, you should follow this design flow:

1. design the schematic
2. simulate the schematic to make sure the function meets the requirements
3. design layout
4. Physical verification (DRC, LVS, PEX)
5. Post-Layout Simulation

This part will introduce the first 4 steps with a simple inverter as a case. But the introduction of the forth step will focus on DRC, which has been explained in detail.

1. Design the schematic *inverter*.
   In **CDS.log window** (Fig 1), open "library manager"(**Tools->Library Manager**). Click your library then follow these steps: **File->New->cell view**, the **Create New File** window will pop up (Fig 15), fill in cell name and select **composer-Schematic** as Tool.

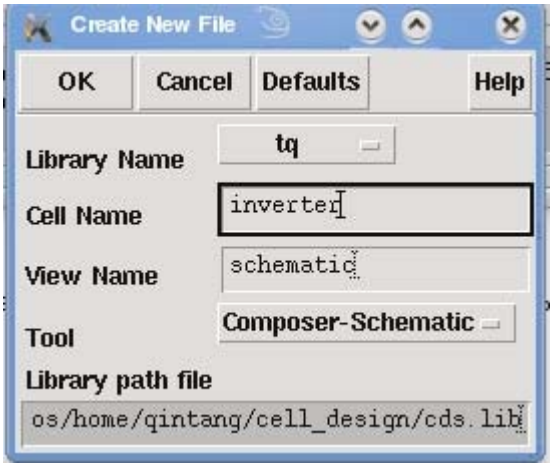

Fig 15 create new schematic

Click OK, then you will see **Virtuoso Schematic Editing** window showing up. Press '**i**' key to add instances to the schematic. Select NMOS and PMOS models from the Library UMC90 (Fig 16), the width and length depend on specific requirement. You should calculate them approximately then set these values manually. Then select Vdd and gnd model from **Library analogLib**. It's the time to connect them, press '**w**' to connect these four models. Finally, press '**p**' to add input Pin (**I** in this example) and output pin (**O** in this example). Click 'check and save' icon to save what you did.

Note: press Esc after finishing every mode, then using icons or keys to enter new mode. & Click 'save' frequently, just in case of some unexpected situations. It's a good habit for designers.

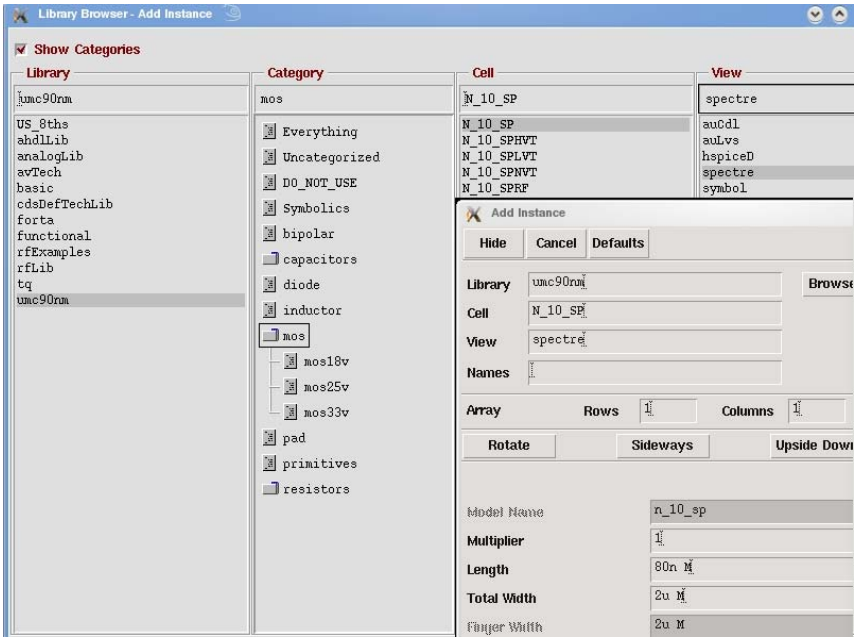

Fig 16 add NMOS spectre model

2. Simulate the schematic to make sure the function meets the requirements.
   In order to simulate the inverter, we usually create a symbol for the inverter, and then create a new schematic named ‘inverter_test’, where the symbol of inverter and input port and output load are added to simulate.

   Open the schematic inverter, click **Design->Creat Cellview->From Cellview**. Click **OK** in pop-up window (Fig 17), and also **OK** for next pop-up window. Finally **Virtuoso Symbol Editing** window pop-up, you can see the symbol of inverter with the same name for input and output ports. ***Remember to save the file by selecting Design->Check and Save in the Symbol Editing window.***

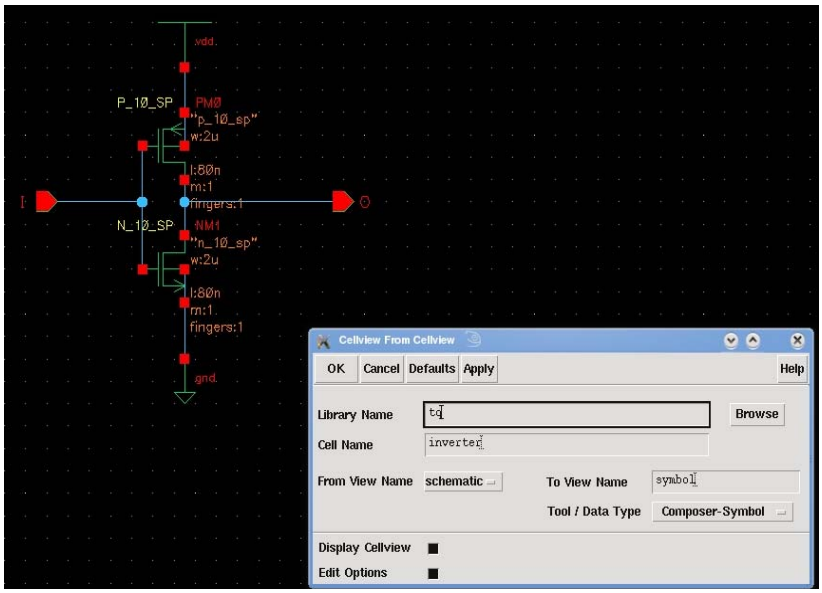

Fig 17 create symbol

Create new schematic named ‘inverter_test’, press ‘**i**’ to add inverter symbol from your library, put it to your schematic by clicking the place then press **Esc** to exit. Press ‘**i**’ to continue to add vpulse, vdc, capacitor, vdd and gnd models.

vpulse is selected from analogLib(Library)→Source-Independent(Category)→vpulse(Cell)---symbol(View)

Set up values like Fig 18:

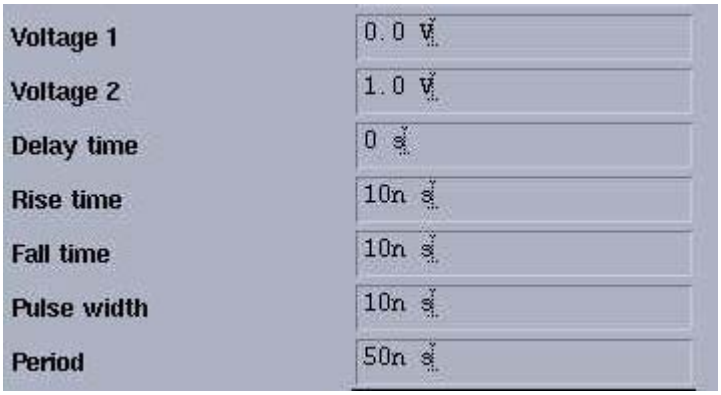

Fig 18 vpluse

vdc is selected from analogLib(Library)→Source-Independent(Category)→vdc(Cell)---symbol(View)

Set up value like Fig 19:

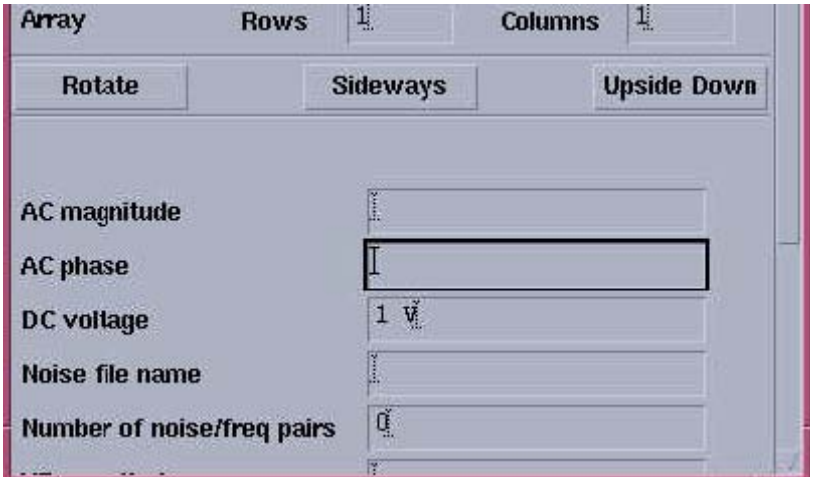

Fig 19 vdc

cap is selected from analogLib(Library)→ passive(Category)→cap(Cell)---symbol(View)

The final schematic for simulation is shown in Fig 20. Select symbol then press ‘**e**’, you can open the detailed circuits of this symbol, if you want to go back to the parent circuit, press **‘Ctrl’ plus ‘e’**. Any modification of *inverter* in *inerter_test* will be saved to *inverter*, so be careful.

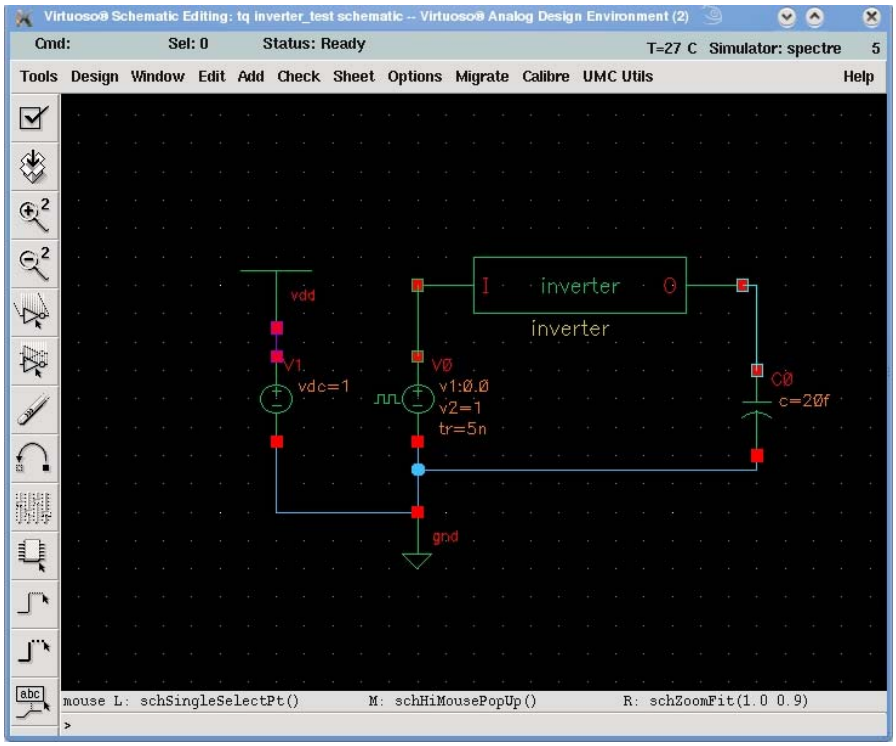

Fig 20 complete schematic inverter_test

After connecting everything for test, click **Tools->Analog Environment** in the **Schematic Editing** window, then **Virtuoso Analog Design Environment** window pops up (Fig 21).

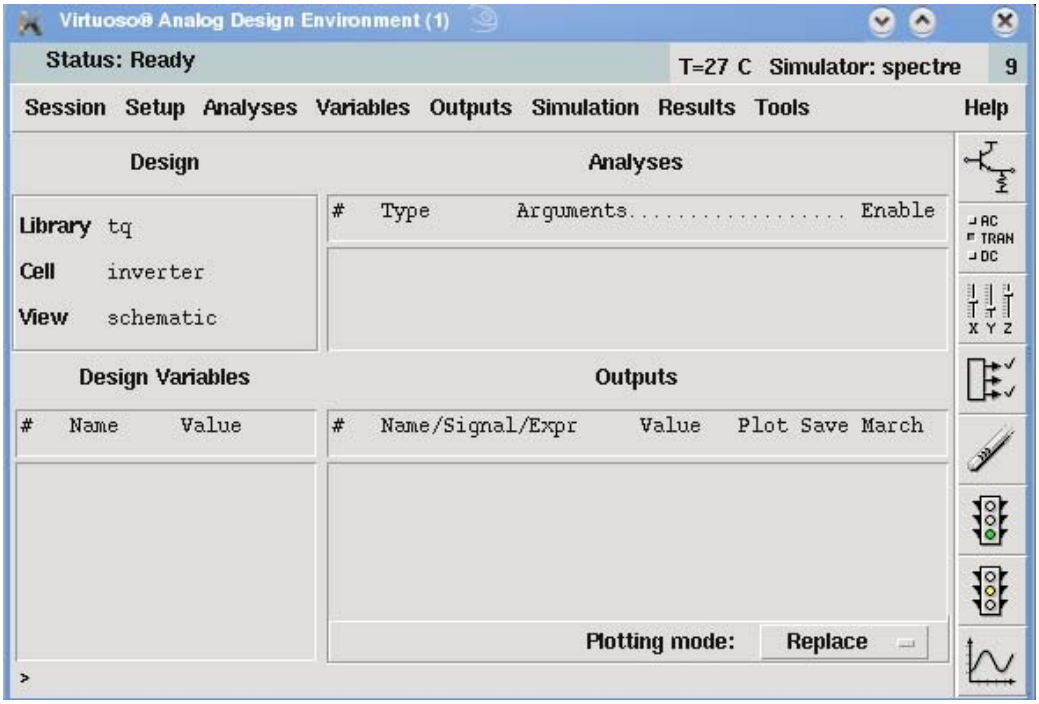

Fig 21 Analog Environment

In the **Virtuoso Analog Design Environment** window, select **Setup->Simulator/Directory/Host**.

The Choosing Simulator/Directory/Host window will appear (Fig 22). Ensure that the simulator is set to '**spectre**' and click on **OK**.

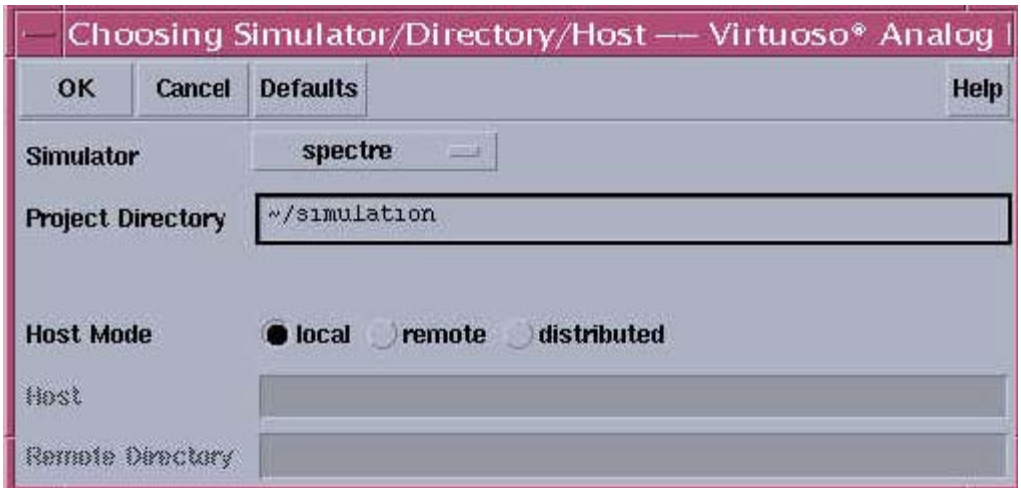

Fig 22 set up the simulator

In the **Virtuoso Analog Design Environment** window, select **Setup->Model Path**. The Setting Model Path window will appear. Check the model directories and you will have the same window as Fig 23.

Note: *select all those library files and click* ***Disable*** *on the right of* ***Model Library Setup*** *window, then select just one file named* ***'…/designkits/umc90nm/…Models/Spectre/L90_SP_V051.lib.scs tt', enable*** *it. Click* ***OK*** *to save changes.*

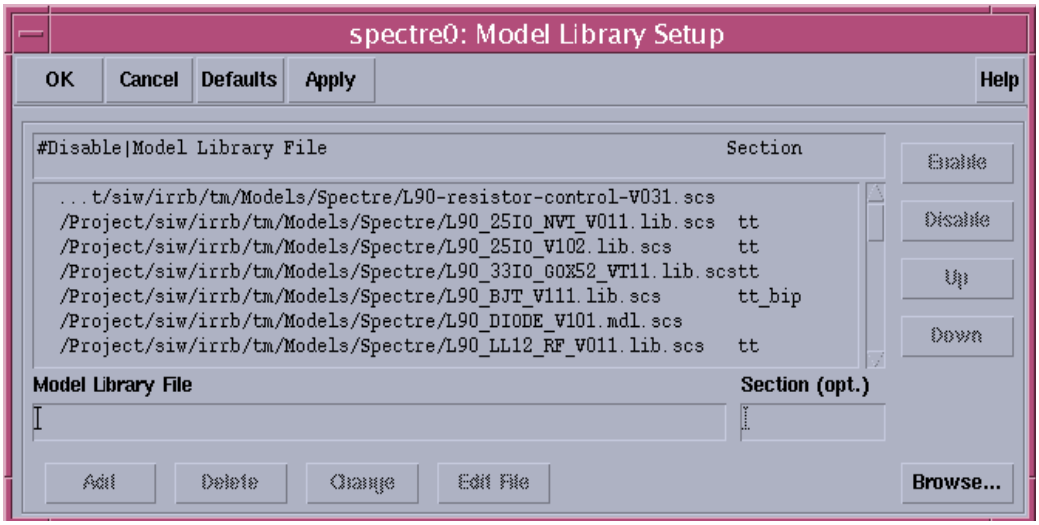

Fig 23 set up the model path

Please refer to http://www.ee.ucla.edu/~dejan/ee115c/ee115c_tut_2.htm to get more information about how to simulate schematic. Modify the W/L ratio of NMOS and PMOS devices to meet specification. The next step after completing the schematic design is to design layout.

3. layout design

   The basic steps for PMOS layout design have been introduced in detail at the beginning of this paper. Now another method to design layout will be explained.

Open *inverter* schematic. In the **schematic window**, select **Tools->Design Synthesis->Layout XL**, you will see a Startup Option window (Fig 24). Select **create new** then click **OK**.

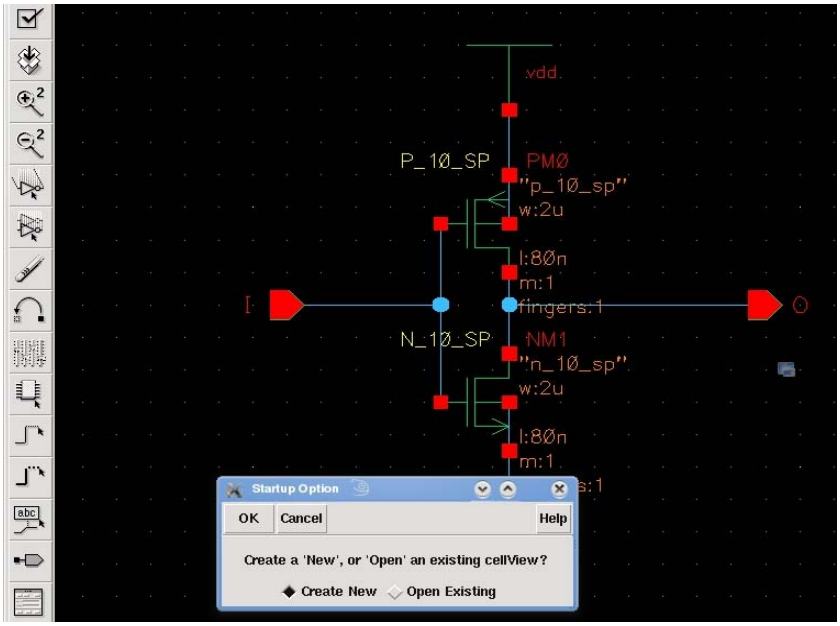

Fig 24 startup option window

A quite familiar window will pop up, which is **Create New File** window (Fig 25). Click **OK** to get an empty **Virtuoso Layout Editing** window of layout *inverter*.

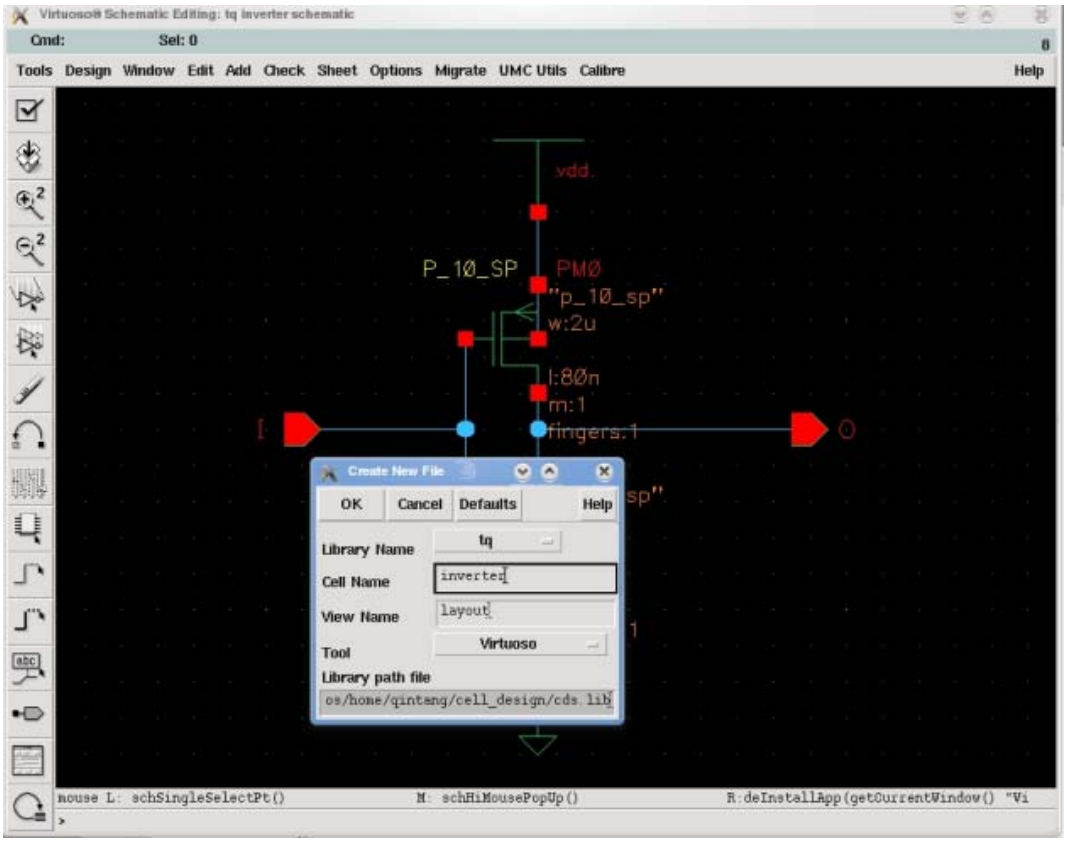

Fig 25 create new layout file

In the **Virtuoso XL Layout** window, select **Design->Gen from source**. The **Layout Generation Options window** will appear (Fig 26). Then, users need to set up the options in Layout Generation, I/O Pins, and Boundary.

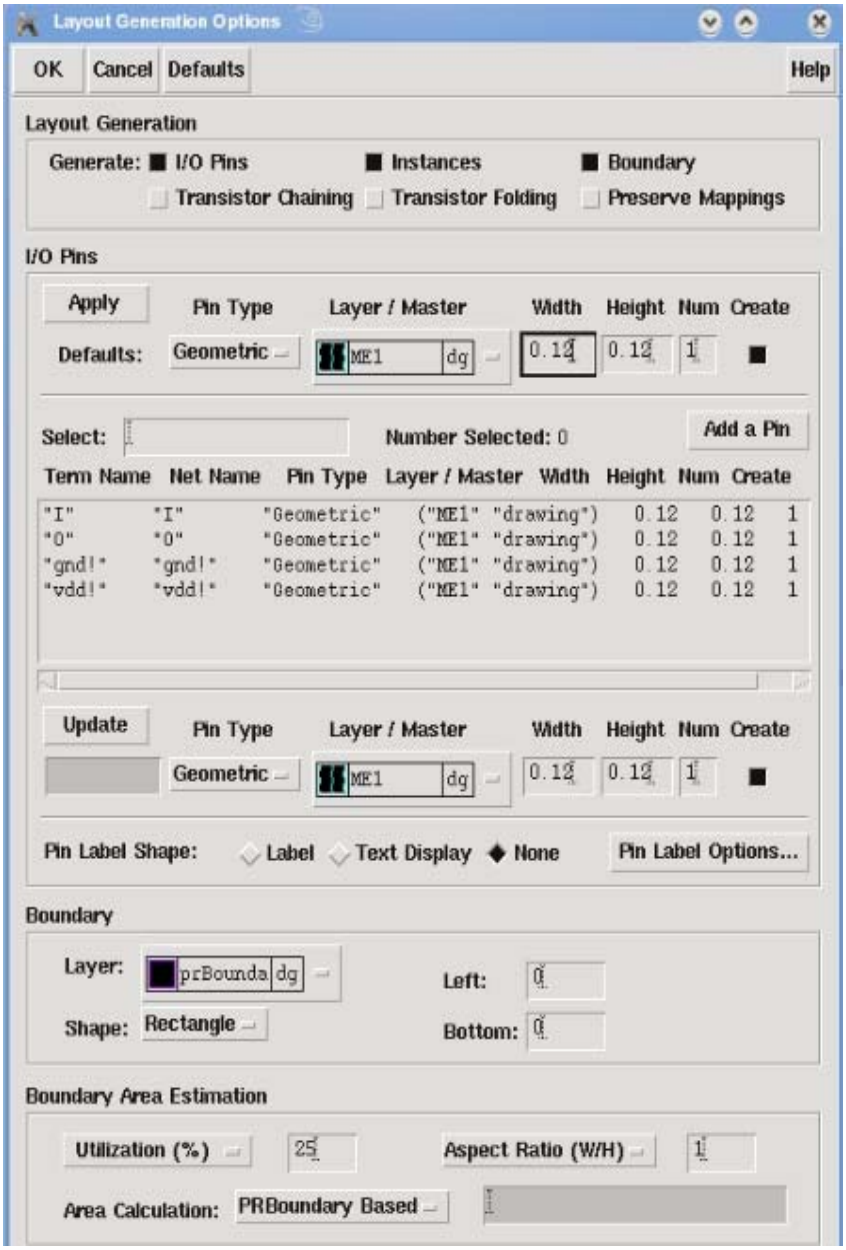

Fig 26 Layout Generation Options Window

Click **OK**. Transistors and I/O pins will appear in the layout view (Fig 27). Now when you move anyone of them, you will see the connecting line is moved along with it (Fig 28). It is beneficial for designers because the possibility of incorrect connection is reduced.

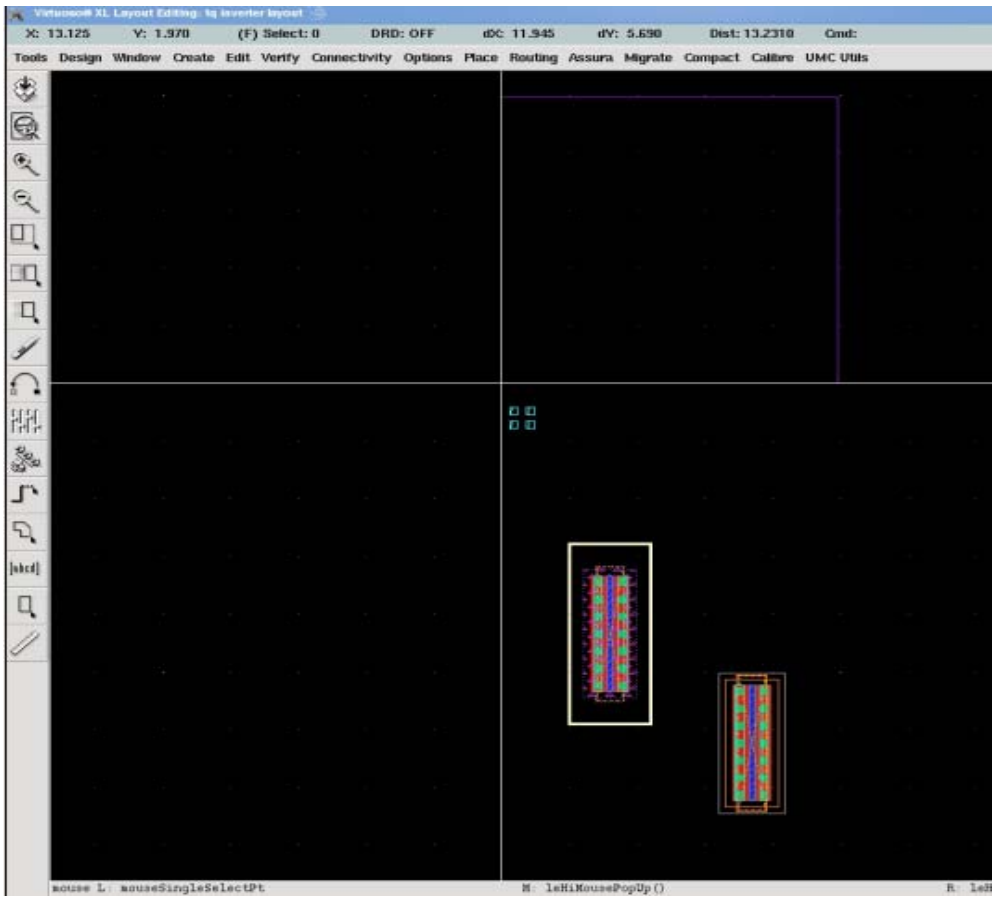

Fig 27 layout automatically generated

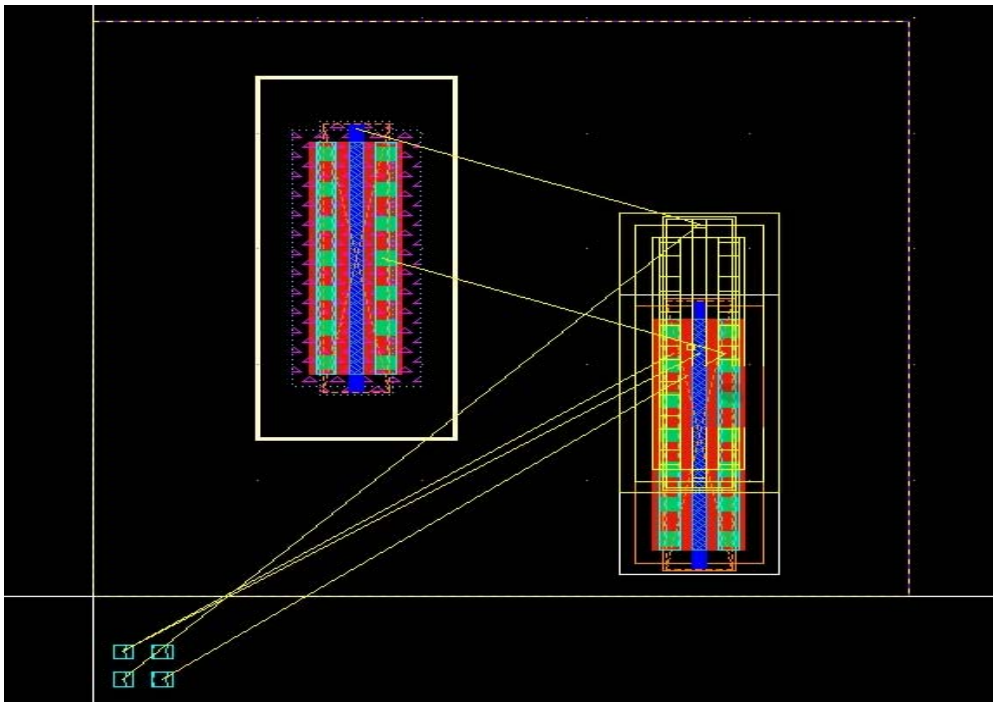

Fig 28 connection in the layout

The NMOS and PMOS models are placed here automatically but it doesn't mean layout design is completed. Supply voltage vdd and ground gnd, M1-NWEL and M1-Psub contacts need to be added and connected. Similarly, the source, drain,

gate and body pickups should be created and at last, labels need be added. The complete layout is shown in Fig 29.

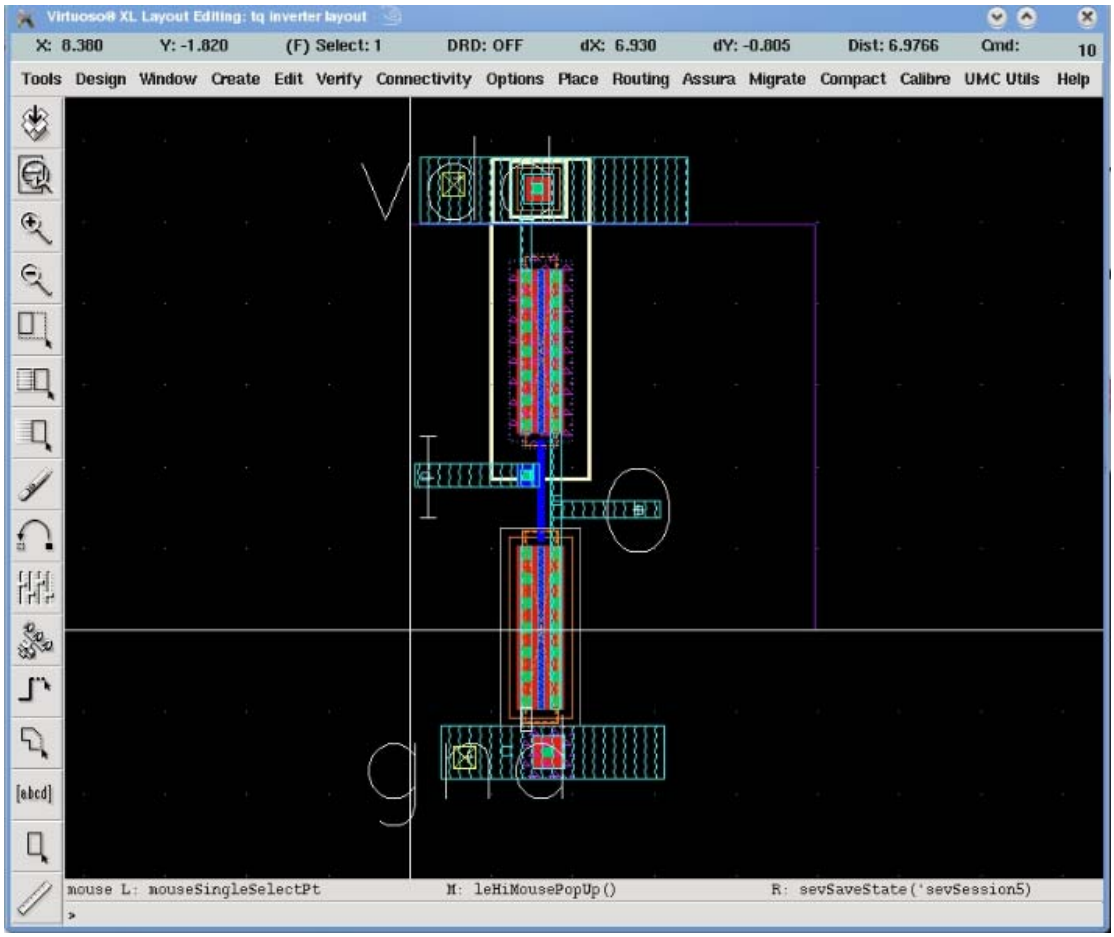

Fig 29 the complete layout

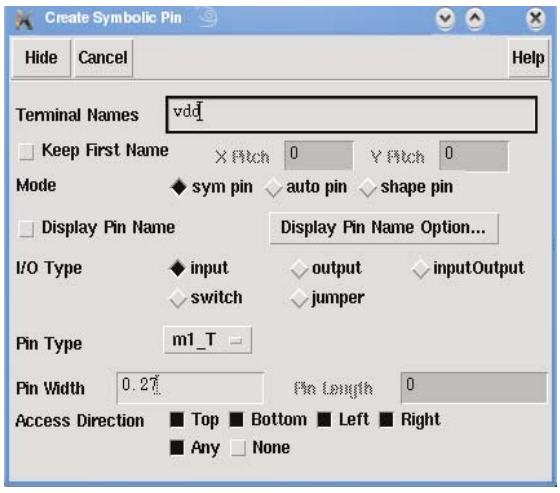

Fig 30 create symbol pin

Note:

The labels in layout must be constant with pin names in schematic. Select **Create->Pin** in **Layout Editing window**. **Create Symbol Pin** window will appear (Fig 30). Fill in Terminal Names and select I/O Type and Pin width for different pins. Pin Type should be **m1_T** because vdd, gnd, input I and output O are all connected by ME1 layer. Click **Hide** then put cursor to the right place and click, the pin name is added successfully.

If layout creation is completed, next step is to run physical verification, in which DRC is the first step. DRC is introduced in detail in previous part. For LVS and PEX, please refer to http://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2

Appendix

The PMOS transistor is made by using the layers as shown in Fig 5. The steps to design this layout are listed below. Considering PMOS layout design is an exercise for you, figures to illustrate each step are not put here, please do the homework by yourself.

1. Choose the **P01** layer, press r to draw a rectangle with the size you want. The minimum width of P01 is 0.08um. The width of P01 determines the channel length.
2. Choose layer **DIFF**, press r to draw active area on the layout. This step defines the active area of the PMOS.
3. Choose the layer **CONT**, Check the minimum distance between P01 and CONT and the minimum DIFF enclosure of the CONT from the Design_rules.ppt, Draw some CONT on the layout. CONT create some holes on the oxide layer for metal contact with the active area, of course all of CONT are in DIFF.
4. Check the minimum P01 overhang of DIFF, use k key to measure the distance. Then press s to stretch P01 layer to modify the poly-gate to fit the requirement. The minimum extension mainly overcomes the misalignment of masks to avoid failure of device
5. Choose **ME1** layer, check minimum width of ME1 and minimum enclosure of CONT from the design rules and then draw two metal1 strips on the layout. The ME1 strips here are used to connect active area of PMOS.
6. Choose the **PPLUS** layer. Check the minimum PPLUS overhang of DIFF, draw the PPLUS implantation mask. The area with PPLUS layer will be implanted to P+ region to ensure ohmic contact between the metal and the substrate.
7. Select **SDSYM** layer, and then draw a rectangle exactly overlapped with channel. I still have no idea about what is SDSYN layer, maybe it is oxide. I didn't find any useful information in data sheet, but in standard library, all kinds of PMOS and NMOS layout have this layer, perhaps it is special requirement of the process.
8. Select **DEVICE** layer to draw device area. Then select **PPLUS** to draw an overlapped area.
9. Select **NWEL** layer. PMOS must be built in Nwell. Check the minimum NWEL enclosure of P+ DIFF (the overlapping area of PPLUS and DIFF). Draw a rectangle in NWEL layer.

Now, click 'check and save' to save your design, and then run Calibre-DRC.

Actually when you design the inverter, you will utilize existing PMOS and NMOS models in the library. But learning how to design PMOS and NMOS transistors by yourself is useful for you to understand fabrication process.