A 0.1pJ Freeze Vernier Time-to-Digital Converter in 65nm CMOS

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***Abstract*—A Freeze Vernier delay line time-to-digital converter for very low power and high resolution is presented. The Freeze Vernier Delay Line is a Vernier-type TDC, where the state of the start line can be frozen by the stop line, omitting the power-hungry time capture elements like D-registers or arbiters that are usually employed in a Vernier TDC. The two main issues of the design, the charge kickback between the delay lines and the imperfect freezing are solved with additional circuitry. The TDC core consists of inverters and current-enabled inverters only. A proof-of-concept design has been implemented in 65nm CMOS with a typical resolution of 4.88ps, a dynamic energy consumption of 106.22fJ per conversion and a combined gate width of 96μm.**

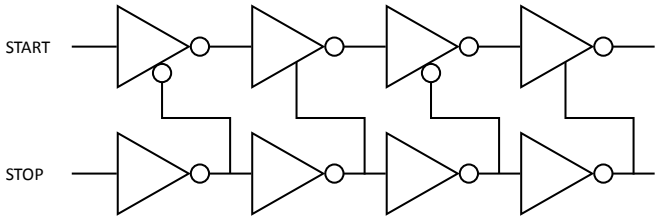


Fig. 1: Freeze Vernier Delay Line architecture

I. Introduction

With the ever-increasing integration of functionalities onto silicon chips, the so called time-to-digital converters (TDCs) [1] have been introduced which can be fabricated with standard CMOS processes. TDCs are stopwatches that measure the time difference between two signal edges and convert it to a digital code, with a resolution of picoseconds [2]. The downscaling of CMOS technology has brought more and more different architectures into the state-of-the-art [3].

The original counter-based solutions had proven to be limited by the clock period [4], so sub-clock period resolution TDCs were proposed. Taking the analogy from analog-to-digital converters, the flash-type TDCs [5] are based on delay line(s) with identical delay stages. To achieve sub-gate delay resolution, the Vernier delay line is used [6]. In the Vernier delay line the timing resolution is dependent on the delay difference of the start and stop line stages, thus it can in theory take an arbitrarily small value. Practical limits that arise when increasing resolution are typically due to the time capture elements, process spread and drive/load mismatch [7].

To achieve high resolution by separating the signal propagation and the sampling in the delay line, the Vernier Gated Ring Oscillator [8] architecture has been proposed, where the delay stages are frozen by the start and the stop signal. Wherever the signal is frozen in transition, the analog voltage value is preserved long enough to be read out by a counter. As a consequence, the design also consumes considerably less power. Similarly, the charge kickback from the time capture elements is no longer present.

The disadvantage of the Gated Vernier Ring Oscillator is that the external signal has to drive a large capacitive load consisting of all the delay elements in the loop. Furthermore, the start and the stop signal are led through extra circuitry to operate the TDC. Finally, the ring oscillator itself has a nonideal layout which introduces delay mismatch between the stages, thus the timing error increases linearly with time.

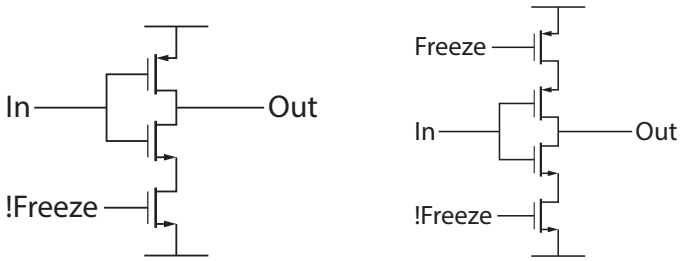
In this paper we propose the Freeze Vernier Delay Line as a low-power TDC which eliminates the loop error and the heavily loaded enable signal in the Vernier Ring Oscillator. It is a variant of the conventional Vernier delay line where, just like in the Vernier Gated Ring Oscillator, the delay line can be frozen with the current starving technique. Unlike in the Vernier GRO, however, the stop line acts as a disable input for the delay elements of the start line. This eliminates the extra circuitry in the Vernier GRO and the disable signal is no longer heavily loaded, because each delay stage is connected to one disable input only. Furthermore, the proposed architecture is not in a loop, thus the timing error does not increase with time and regular layout can be made.

II. Architecture

The conventional Vernier delay line TDC [6] makes use of one ‘fast’ and one ‘slow’ delay line. The start signal arrives first and propagates through the slow line, while the stop signal follows and enters the fast line. The time difference between the arrival of the start and stop signal can be determined with time capture circuitry by finding the delay stage where the stop signal takes over the start signal. The problem with the Vernier technique is the large load imposed by these time capture elements or early-late detectors (ELD, usually a D-register or an arbiter [1]). In the following we propose a way to eliminate these circuit elements.

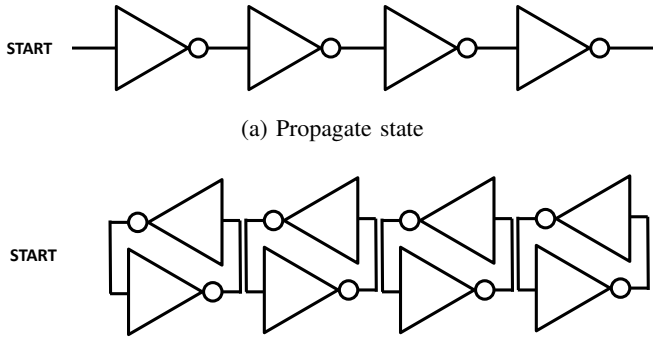
Our Freeze Vernier architecture fully benefits from the Vernier principle without the need of ELDs. This is done by freezing the node voltages of the start line exactly at the moment when it is supposed to be sampled by an ELD. As mentioned before, the method of freezing the delay stages is already known as in the Vernier-Gated-Ring-Oscillator [8]. In a gated-Vernier delay line, a ring oscillator is frozen [9] by

978-1-4799-3432-4/14/$31.00



(a) N-Freeze inverter (b) Feedback inverter

Fig. 2: Freeze inverters



(a) Propagate state

(b) Hold state

Fig. 3: Functional description of the Freeze Vernier Delay Line

disabling the delay elements. While conventionally this is done by an external signal for all delay elements synchronously, our Freeze Vernier architecture uses the stop signal to freeze the start line in a linear Vernier delay line. The start and the stop signals are directly fed into the slow and fast line, respectively. When the stop signal reaches a certain stage in the fast line, it freezes the corresponding stage in the slow line, as depicted in Figure 1.

In the Freeze Vernier architecture we implemented the delay stages with two inverters, forming a buffer which has considerable better DNL than an inverter-stage Vernier Delay architecture. For the stop line, normal CMOS inverters are used, while the start line has one inverter which has an NMOS footer device (Figure 2a), connected to the stop line node. Thus the stop line, instead of driving the clock input of a D register as in conventional Vernier delay line, is now connected to a current-enabled inverter [10] as an enable/disable input. At the end of the measurement, the start line is entirely frozen and the transition point indicates where the stop signal has caught up with the start signal. Usually at that point there are digitally invalid analog values, which need to be regenerated in order to provide the thermometer signal.

The advantage of proposed Freeze Vernier architecture is that the time capture blocks have been eliminated, thus it is possible to obtain high resolution in a power- and area-efficient way. The measurement rate is also better as the start and the stop lines are not loaded as heavily as they would be with an early-late detector. The core does not need any reset signal — it resets on the falling edge of the stop and the start signal. The drawback is that in the frozen state, there are invalid logic values which generate extra static power consumption and have to be regenerated with extra circuitry to provide valid logic values. Similarly, the stop line suffers from the charge injection by the start line, causing second-order INL. In the following, the solutions for the aforementioned problems are presented.

To eliminate the drawbacks, it is important to understand the operation of the Freeze Vernier Delay Line, which is depicted in the Figure 3a and 3b. While the stop signal has not caught up with the start signal, the start-line ideally behaves as a delay line with stages of identical delay. This phase of operation is the ‘propagate’ phase (Figure 3a), because the signal on the start-line is advancing uninterrupted. In a conventional Vernier architecture the TDC only operates in this ‘propagate’ phase since external time capture elements store the timing difference between the start and the stop line. However, our Freeze Vernier architecture has a second phase — the ‘hold’ phase (Figure 3b). The hold phase is when the stop line has caught up with the start line and the state of the start line must be preserved. In order to achieve this, there are two criteria:

1. Isolation: the individual nodes must be independent from each other, i.e. the logic value of one cell should not influence the other. As a consequence the start line stages must separate their input from the output, which is accomplished by using freeze inverters (Figure 2a). The NMOS footer transistor prevents a high-to-low transition in the start line if the stop line has switched it off. At the same time, if the stop signal has not yet arrived, the two NMOS transistors are both enabled and are able to pull down the next node. Since buffers are implemented as delay stages, there is only one type of transition occurring at the freeze inverter which makes a PMOS header unnecessary.

2. Regeneration: since the Freeze Vernier architecture makes use of current starved inverters which can be enabled/disabled, there are digitally invalid analog values at the stages where the stop signal catches up with the start signal. The invalid logic values are present due to the finite transition time of the freeze inverters; once the stop-line catches up with the start-line, the latter is frozen by the former. In some cases the start-line gets frozen during transition, which results in an invalid logic value. These invalid logic values are regenerated

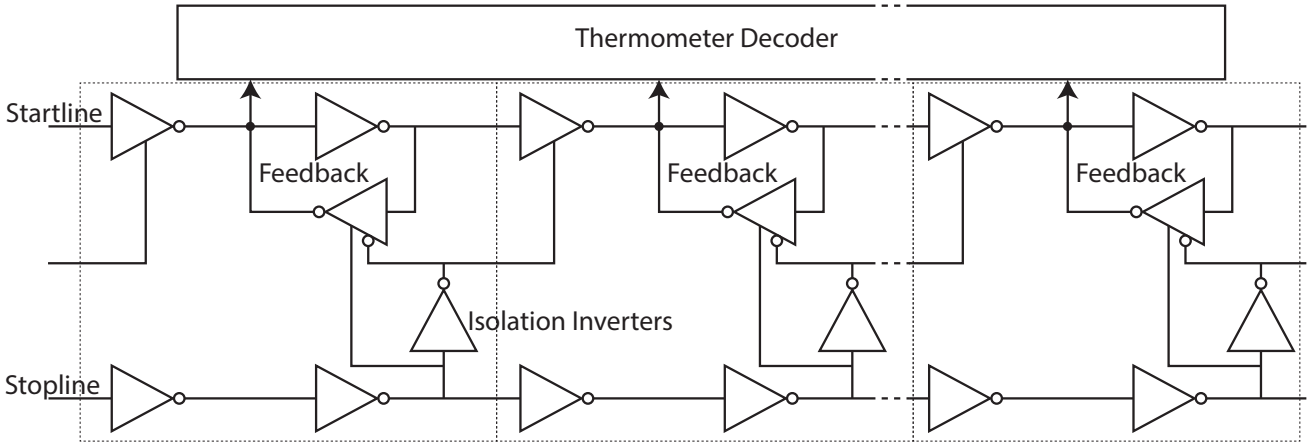


Fig. 4: Simplified overview of the buffer-stage Vernier Delay Architecture

TABLE I: Simulation results for the Freeze Vernier TDC

	SS	TT	FF	FNSP	SNFP
Resolution	5.77ps	4.69ps	3.99ps	3.87ps	5.43ps
Power	98.74fJ	104.30fJ	113.71fJ	105.41fJ	103.74fJ
INL	0.891	0.815	0.708	0.809	0.782
DNL	0.403	0.280	0.053	0.394	0.216
Offset	1.83ps	0.95ps	0.24ps	1.24ps	0.67ps

by adding a bi-stable circuit to the output nodes, which are composed of the second inverter of the start line buffer and a cross-connected feedback inverter with enable from the stop line, making a simple latch. In order to provide a fast and precise start-line delay and maintain low power consumption, the feedback inverter (Figure 2b) of the inverter pair is enabled by the stop line (Figure 4).

The start and the stop line are coupled through the enable/disable transistor in the freeze inverter. When the start signal propagates through the freeze inverter, a small amount of charge is dumped onto the freeze transistor. This charge kickback causes a shift in the delay of the stop line stages which are near the transition point. The result is a second order INL. In the present design it was decided to shield the stop line from part of the charge kickback by introducing an isolation inverter between the start and the stop line (see isolation inverters in Figure 4). This protects the stop line from most of the charge.

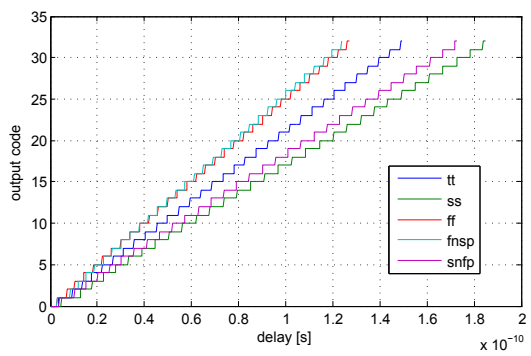
In order to optimize power consumption and resolution, devices with different threshold voltages (Vt) were implemented. We designed the freeze inverter in the start line to be all-low-Vt to compensate the large delay imposed by the footer NMOS. The two inverters in the stop line buffer and the second inverter of the start line buffer are identically implemented with normal Vt devices. We have 'skewed' the feedback inverter to favor pull-up for quick regeneration: the PMOS transistors are low-Vt, while the NMOS transistors are high-Vt. The shield inverter was designed to be high-Vt since it does not drive large load and its speed is not important.

III. Simulation

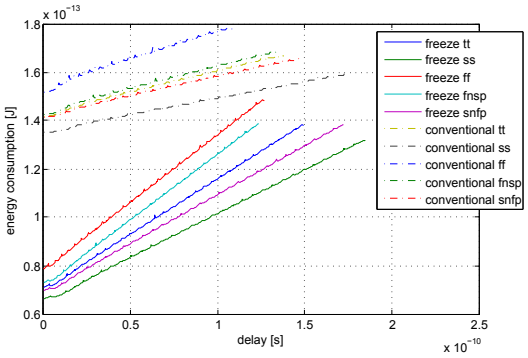
The Freeze Vernier TDC was simulated, along with a Vernier TDC as a reference design, in a 65nm CMOS process in the FF, SS, TT, FNSP and SNFP corners (FF – fast NMOS and PMOS; TT – typical NMOS and PMOS; SS – slow NMOS and PMOS transistors). In each of these corners we calculated the merits for different input delays. From the output code, the INL, DNL and resolution were extracted, as well as the supply current values were used to calculate the average energy consumption, as shown in the Table I. The process variations can be eliminated by two standard ways [11]. One is based on applying the current starving technique [10] for the second inverter in the buffers. The resolution can then be set with a delay-locked loop. Another way to solve the problem is to measure the period of a known signal, then interpolate the linear curve to get the resolution, which then can be used for digital correction.

In Figure 5a the output curve and hence the DNL and INL result of the simulation is presented. The results show low DNL due to matched capacitance and inverter drive strength. The power consumption of the Freeze Vernier TDC — unlike that of the conventional Vernier TDC reference design — depends heavily on the input delay, as shown in Figure 5b. Due to the freeze architecture, the propagation of the start line is discontinued once the stop signal has taken over, therefore the rest of the start line does not switch state. In average this operand isolation saves about 25% of the power for a uniformly distributed random input, compared to a full delay input.

As consequence of the simple architecture, prototype design fits very small area with 96μm combined transistor width, and 6 inverters per stage. The average DNL over the corners was 0.27LSB with a maximum of 0.4LSB, while the INL average value was 0.8LSB with maximum of 0.89LSB. The average resolution is 4.88ps with 1.1ps spread over different corners, while the average energy per conversion is 106.22fJ for a 1.2V supply. The power consumption of the core is 0.06 mW for a 250 MS/s sample rate. With these merits, the proposed Freeze Vernier Delay Line architecture is the most power-efficient high-resolution TDC, as shown in Table II.



(a) Output codes



(b) Energy consumption

Fig. 5: Simulation results

TABLE II: Comparison with reference design and other architectures (*simulation data)

	This Work*	[8]	[12]*	[13]	[11]	[14]	[15]
Scheme	Freeze Vernier (Vernier)	Vernier gated ring osc.	delay line	2 D Vernier	local passive interpolation	inverter-chain	two-step
Technology	65nm (65nm)	90nm	90nm	65nm	90nm	65nm	65nm
Supply	1.2V (1.2V)	1.2 V	1 V	1.2V	1.2V	1.33V	1.2V
Area	0.00062mm^2 (core, est.)	0.027mm^2	0.032mm^2	0.02mm^2	0.02mm^2	0.0063mm^2	0.002mm^2
Resolution	4.88ps (4.2ps)	3.2ps / 30ps	6.25ps	4.8ps	4.7ps	80ps	3.75ps
DNL	0.40LSB (0.1LSB)	NA	0.04LSB	1LSB	0.6LSB	0.01LSB	0.9LSB
INL	0.89LSB (1.18LSB)	NA	0.015LSB	3.3LSB	1.2LSB	NA	2.3LSB
Range	156ps (134ps)	NA / 40ns	37.5ps	614ps	601ps	4ns	480ps
Number of Bits (b)	5bit (5bit)	10bit	3bit	7bit	7bit	10bit	7bit
Sample Rate (f_S)	250MS/s (250MS/s)	100MS/s / 25MS/s	5GS/s	50MS/s	180MS/s	250MS/s	200MS/s
Power (P)	0.060mW (0.073mW)	3.6mW / 4.5mW	9mW	1.7mW	3.6mW	5.66mW	3.6mW
FoM$_P$ ($P/f_S 2^b$)	7.5fJ (9.1fJ)	35.1fJ / 175.7fJ	225.0fJ	265fJ	156.2fJ	22.1fJ	140.6fJ

IV. Conclusion

The proposed Freeze Vernier TDC is a high-speed, simple and robust architecture with very low power consumption and a low area. The overall TDC consists of inverters and current enabled inverters only, omitting the power-hungry time capture elements like D-registers or arbiters that are usually employed in a Vernier TDC. A proof-of-concept design has been implemented in a 65nm CMOS technology with a typical resolution of 4.88ps, dynamic energy consumption of 106.22fJ per conversion and a combined gate width of 96μm.

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