Efficient Sensitivity-Based Capacitance Modeling for Systematic and Random Geometric Variations

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Abstract— This paper presents a highly efficient sensitivity-based method for capacitance extraction, which models both systematic and random geometric variations. This method is applicable for BEM-based Layout Parasitic Extraction (LPE) tools. It is shown that, with only one system solve, the nominal parasitic capacitances as well as its relative standard deviations caused by both systematic and random geometric variations can be obtained. The additional calculation for both variations can be done at a very modest computational time, which is negligible compared to that of the standard capacitance extraction without considering any variation. Specifically, using the proposed method, experiments and a case study have been analyzed to show the impact of the random variation on the capacitance for a real design.

I. Introduction

Manufacturing variability can be categorized into systematic and random variations. Systematic variations are introduced by predictable design or process procedures, and are often highly layout-dependent. Contour variations, for instance, are induced during the lithography step, while thickness variations in metals and interlevel dielectrics (ILD) can be caused by chemical mechanical polishing (CMP). Although there are design rules and compensation techniques, e.g. OPC for the lithography, provided by the fab, small variations are still observed in the deep sub-micron era. The study of modeling systematic variations started with the worst-case corner method, which was acknowledged to be overly pessimistic. A statistical approach using empirical capacitance expressions was then proposed to overcome this problem [1]. An enhanced lookup method based on analytical capacitance models was presented in [2], to account for systematic variations by computing the derivatives of capacitances with respect to the thickness and the linewidth deviations. These derivatives were later referred to as *sensitivities* and have been computed for the floating random walk (FRW) method [3] and the boundary element method (BEM) [4] [5].

Random variations, on the other hand, are caused by various unpredictable fluctuations in the manufacturing environment. In most cases, random variations are not layout dependent, but often a spatial correlation can be observed. One of the most typical random geometric variations is the so-called line-edge roughness (LER), which has been intensively studied for the critical dimensions of MOSFETs since the technology nodes reached deep sub-micron dimensions [6]. With technology shrinking, the impact of LER on interconnects and some novel designs of passive components with high-precision requirements [7] demands to be understood and modeled.

Recently, several methods were proposed for modeling random geometric variations of on-chip interconnects. A perturbation based 3D BEM solver [8] and Hermite polynomial chaos technique based approaches [9], [10] and [11] have assessed the effects of variational surfaces on interconnect capacitances by generating quadratic models.

Unfortunately, examples demonstrated in these papers are general cases based on pure theoretical assumptions, which indeed is advantageous in indicating the robustness of the methods. The obtained results, however, are consequently with less guidance for real circuit designs. The variational surfaces of interconnects, for example, are modeled using spatially correlated Gaussian distribution in 3-dimensions, while the irregularity on different surfaces are usually considered independent based on the measurement data [6] [12]. Researches from the technology and the manufacturing part further indicate the nature of striations on the sidewalls [13] [14]. Thus it is appropriate to use the LER to model the sidewall variation of metal wires, as what will be done in this paper. Besides, since the impact of random variations, such as LER, inherently differs largely depending on various applications and technology aspects, parameters characterizing the process spreads need to be selected carefully.

In this paper, an extremely fast sensitivity-based statistical model is proposed to capture the effect of the LER. Although it is less accurate than the quadratic models, its high efficiency can be very useful for estimations and optimizations during early design stages. Experiments with process spreads based on measurement data, as well as a case study are demonstrated to indicate the impact of LER on a real design. This is one of the two main contributions of this work.

The other main contribution is that the nominal capacitance extraction and the statistical modeling of both the systematic and the random variations can be accomplished with only one system solve. This can be done because the method is based on *panel sensitivities*, which will be explained in the following sections. These panel sensitivities can be calculated by manipulating the intermediate data that is used for nominal capacitance extraction, using the algorithm proposed in [4] and [5]. Thus the additional time complexity for modeling the variations is very low and negligible compared to that of the standard capacitance extraction without considering any variation.

The rest of this paper is organized as follows: Section II

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first gives an overview of the BEM-based sensitivity computation and defines the *panel sensitivity*. Section III presents the modeling method for the LER, as well as simulation verifications and a real design case study. Section IV demonstrates the sensitivity-based modeling method for both systematic and random variabilities with one system solve of capacitance extraction. Finally, Section V concludes the paper.

II. Background

Capacitance sensitivity computation based on the BEM has been introduced and proven in [4] and [5]. In fact, the concept of *panel sensitivity* has been used during the algorithm development but has not been well defined. Here, the sensitivity computation will be briefly introduced and the *panel sensitivity* will be defined more precisely.

A. BEM-based Capacitance Extraction

Capacitances used in SPICE netlists are in fact called *network capacitances* ($\mathbf{C}$), defined as

$$C_{ij} = \frac{Q_{ij}}{V_i - V_j} \tag{1}$$

where C_{ij} is the coupling capacitance between conductor i and j; Q_{ij} is the charge incident to C_{ij} and V_i is the potential of conductor i. The relation between charges and potentials can alternatively be written as

$$\mathbf{Q} = \mathbf{C_s}\mathbf{V} \tag{2}$$

where $\mathbf{Q}$ and $\mathbf{V}$ are $N \times 1$ vectors , representing the charges and the potentials on N conductors. $\mathbf{C_s}$ is an $N \times N$ matrix, known as the *short-circuit capacitance matrix* [15]. Its entry C_{sij} is equal to the charge on conductor i when conductor j is held at a unit potential and all other conductors are short-circuited to the ground. Network capacitances C_{ij} and short-circuit capacitances C_{sij} follow a simple relation:

$$C_{ij} = -C_{sij} \ \ \forall \ \ i \neq j. \tag{3}$$

When the BEM is applied for capacitance extraction, surfaces of conductors are discretized into panels. The short-circuit capacitances associated to the discretized panels before their association to conductors are called *partial short-circuit capacitances*, denoted $\bar{\mathbf{C}}_\mathbf{s}$ in this paper. An incidence matrix $\mathbf{B}$ is then used to associate $\mathbf{C_s}$ and $\bar{\mathbf{C}}_\mathbf{s}$:

$$\mathbf{C_s} = \mathbf{B}^T \bar{\mathbf{C}}_\mathbf{s} \mathbf{B} \tag{4}$$

where $\bar{\mathbf{C}}_\mathbf{s}$ is an $m \times m$ matrix and $\mathbf{B}$ is an $m \times N$ matrix, with m being the number of panels.

B. Panel Sensitivity

As presented in [5], the sensitivity of the coupling capacitance between two conductors i and j, w.r.t. a small displacement d_k of a panel k can be written as

$$\frac{\partial C_{ij}}{\partial d_k} = -\frac{1}{\varepsilon A_k} \sum_{a \in N_i} \sum_{b \in N_j} \bar{C}_{sk,a} \bar{C}_{sk,b} \tag{5}$$

where A_k is the area of panel k and ε is the material permittivity surrounding the panel. Again $\bar{C}_{sk,a}$ is an entry in the partial short-circuit capacitance matrix ($\bar{\mathbf{C}}_\mathbf{s}$), representing the short-circuit capacitance between panel k and a.

For ease of discussion, the following short-hand notation is introduced:

$$\mathcal{C}^*_{ki} = \sum_{a \in N_i} \bar{C}_{sk,a}, \tag{6}$$

where $\mathcal{C}^*_{ki}$ expresses the short-circuit capacitance between a panel k and a conductor i. With (5) and (6), the *panel sensitivity* of the coupling capacitance is defined as follows

$$\mathcal{S}_{k,ij} = -\frac{1}{\varepsilon A_k} \mathcal{C}^*_{ki} \mathcal{C}^*_{kj} \tag{7}$$

which expresses the capacitance sensitivity w.r.t. a small fluctuation of a panel k from its nominal position.

C. Sensitivity Based Modeling for Systematic Variability

Systematic variability often appears in the form of variations in the structural dimensions of interconnects or passive structures. Thus when using sensitivity based modeling to capture this variability, the sensitivity is defined to be w.r.t. a geometric parameter (p), for instance the width of a conductor, the thickness of each metal layer or the height of dielectrics. This dimensional sensitivity can be computed by assembling the associated panel sensitivities:

$$\frac{\partial C_{ij}}{\partial p} = \sum_{k \in S_p} \mathcal{S}_{k,ij} \tag{8}$$

where S_p is the set of panels incident to the geometric parameter p. In other words, these are the panels that show displacements according to the parameter variation. Dimensional sensitivities w.r.t. different geometric parameters are simply computed from different sets of corresponding panel sensitivities. Using the computed sensitivities, the variance of the capacitance due to the dimensional variation can be obtained easily:

$$var(C_{ij})_{sys} = (\frac{\partial C_{ij}}{\partial p})^2 \sigma_p^2 = (\sum_{k \in S_p} \mathcal{S}_{k,ij})^2 \sigma_p^2 \tag{9}$$

where σ_p is the standard deviation of parameter p. Details of the sensitivity modeling for systematic variability can be found in [4] and [5].

III. Panel Sensitivity based Modeling for LER

In this section, a statistical modeling method of capacitances based on the panel sensitivities is proposed to capture the impact of the random geometric variation LER.

A. Statistical Model of LER

The LER can be modeled with a sequence of random variables ρ, representing the fluctuation behavior along the line, which in this paper, is defined as y-direction (see Fig. 1). The fluctuation itself is in the direction orthogonal to y-direction, defined as x-direction. The LER thus can be characterized with

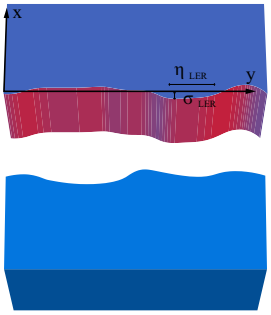

Fig. 1. Two parallel conductors with LER.

two parameters, namely the standard deviation (σ_{LER}), representing the absolute roughness amplitude orthogonal to the line-edge, i.e. in x-direction, and the correlation length (η_{LER}) along the line-edge, i.e. in y-direction, as shown in Fig. 1. The random variables are often assumed to be Gaussian spatially correlated along y-direction, described as

$$cov(\rho_i, \rho_j) = \sigma^2_{LER} exp(-\frac{|\mathbf{r}_{i,y} - \mathbf{r}_{j,y}|^2}{\eta^2_{LER}}) \qquad (10)$$

where $\mathbf{r}_{i,y}$ and $\mathbf{r}_{j,y}$ are the y-coordinates of the positions associated with ρ_i and ρ_j respectively. One can see that the closer two variables are located, the stronger they are correlated. The correlation length is a parameter that measures the strength of the correlation between two variables: if the distance (in y-direction) between them is much larger than η_{LER}, they can be considered independent.

B. Physical Model of LER

Although the physical model of LER is not needed for the modeling method of capacitances to be presented in the next section, it is necessary for conducting Monte Carlo simulations for verification purposes. In this paper, the same approach as presented in [6] is used to physically capture the LER. This is done by producing random line patterns generated from the inverse Fourier transform of the power spectrum of the Gaussian autocorrelation function. Then these random line patterns can be used for approximating the LER when MC simulations are performed as a comparison with the proposed method.

C. Statistical Model of Capacitances Using Panel Sensitivities

The statistical model of LER can be naturally applied to the BEM. The random variables can even be directly adopted as the displacement of the corresponding BEM discretized panels. These panels will be called *deviation panels* in the rest of the paper. Each rough line corresponds to a set of deviation panels. Different sets of deviation panels incident to different rough lines are independent.

A linear model for BEM-based extraction tools is thus proposed to capture the effect of LER on capacitances:

$$\Delta C = \sum_{l=1}^{L} \sum_{i=1}^{n_l} \mathcal{S}_i \rho_i \qquad (11)$$

where ΔC is the capacitance variation induced by the LER; $\mathcal{S}_i$ is the panel sensitivity associated with the panel displacement ρ_i; n_l is the number of deviation panels for rough line l while L is the number of rough lines.

Due to the linearity of (11), the variance of ΔC can be calculated as

$$\begin{aligned} var(\Delta C)_{LER} &= var(\sum_{l=1}^{L} \sum_{i=1}^{n_l} \mathcal{S}_i \rho_i) \\ &= \sum_{l=1}^{L} \left[\sum_{i=1}^{n_l} \mathcal{S}_i^2 var(\rho_i) + 2 \sum_{i,j:i<j} \mathcal{S}_i \mathcal{S}_j cov(\rho_i, \rho_j) \right] \end{aligned} \qquad (12)$$

where $var(\rho_i)$ is the squared standard deviation of ρ_i in x-direction, i.e. σ^2_{LER} , and the covariance $cov(\rho_i, \rho_j)$ follows from the correlation function (10). Note that this statistical model of capacitances (12) can be easily adjusted or extended if the model (10) of the geometric variations changes.

From the key equation (12), it follows that the statistical property of the deviated capacitance due to the LER can be easily obtained using the panel sensitivities introduced in Section II.B. Also note that the computational burden of (12) includes two parts, namely the calculation of the panel sensitivity $\mathcal{S}_k$ and the calculation of the covariance $cov(\rho_i, \rho_j)$. As has been addressed in (7), the panel sensitivity $\mathcal{S}_k$ is computed from $\mathcal{C}^*_k$ which is an accumulation of partial short-circuit capacitances incident to a conductor. These partial short-circuit capacitances $\bar{\mathbf{C}}_s$ are the intermediate data for calculating the nominal capacitance (4), thus they are already computed for the standard capacitance extraction. The time cost for accumulating $\mathcal{C}^*_k$, i.e. the calculation of $\mathcal{S}_k$ is negligible compared to a system solve for the nominal capacitance extraction.

As for $cov(\rho_i, \rho_j)$, the computational complexity is related to the correlation length. Within the distance of a correlation length, a certain number of panels are required in order to physically approximate the roughness, which can not be avoided. However, since the correlation $cov(\rho_i, \rho_j)$ decays rapidly as the ratio of $|\mathbf{r}_{i,y} - \mathbf{r}_{j,y}|$ and η_{LER} increases, the computational complexity can be greatly reduced by calculating only the non-negligible elements in the double summation $\sum_{i,j:i<j} \mathcal{S}_i \mathcal{S}_j cov(\rho_i, \rho_j)$. Meanwhile, the longer the interesting structure is (in y-direction) compared to the correlation length, the more panels are necessary and thus the longer computational time will be. However, as can be seen in Section III.E, once the dependence of the statistical property of a capacitance on the size of a structure is acquired, quick estimations can be done without having to simulate the complete structure.

D. Verification and Experiment I

This section presents an experiment to verify the accuracy and the efficiency of the proposed method for the LER effect. The method has been implemented in C/C++ language and the experiment has been conducted on a 3.00GHz Intel 2 Core CPU.

As shown in Fig. 1, there are two parallel conductors with the two sidewalls facing each other suffering from the LER. As

TABLE I
SIMULATION RESULTS AND CPU TIME FOR MODELING LER

	$\frac{\sigma_C}{C}$	Error	CPU Time
Proposed model	0.603%	11.5%	$50''$
MC simulation	0.681%	0	$48653''$

addressed earlier, the impact of LER depends greatly on the values of σ_{LER} and η_{LER}. These values are closely related to the materials and the manufacturing process. Thus in this experiment, the two parameters have been chosen according to the measurement data of Cu wires in meander-fork structures, provided by IMEC [12]:

$$\begin{aligned} \sigma_{LER} &= 3.5nm \\ \eta_{LER} &= 16nm \end{aligned} \tag{13}$$

The width/space of the conductors is $80nm/80nm$. The thickness is $100nm$ and the length is $200nm$.

It is common to use the relative standard deviation $\frac{\sigma_C}{C}$ which is always referred to as "mismatch" by designers, to model the effect of LER on capacitances. Using the proposed method, we can easily calculate $\sigma_C (= \sigma_{\Delta C})$ from (12).

To verify the result of the modeling method, a Monte Carlo (MC) simulation with 1000 samples on the physical LER model is performed as a reference. For each sample, the random line pattern for characterizing the LER is generated as described in Section III.B. The simulation results and the CPU time of the proposed method and the MC simulation are shown in Table I.

The table shows that the error of $\frac{\sigma_C}{C}$ given by the proposed model is around 10%. The error mainly comes from two parts. One is the computational error of the sensitivities. The other one is due to the fact that the presented model for the roughness is based on the piecewise constant function, thus the variational surface is not smooth. This has been studied in [11]. The proposed modeling method can be further improved to diminish the error by using the piecewise linear function, which is beyond the scope of this paper. However, a 10% error for modeling mismatch is well acceptable in most cases since the mismatch is already small compared to the nominal value. Thus, the introduced error is a second-order effect.

With respect to the CPU time, the proposed model is almost 1000 times faster than the MC simulation. More importantly, the CPU time in the table already includes the computation for the nominal value of the capacitance. With a simple calculation, it follows that the computational time for one system solve is $48.653s$ $(= 48653s/1000)$, while the additional time for the σ_C calculation using the statistical model is only 2.77% $(= (50s - 48.653s)/48.653s)$. Hence, the proposed modeling method is extremely fast, and results in little overhead.

E. Experiment II

Using the proposed model, one can easily study:

1. the relationship between $\frac{\sigma_C}{C}$ and the conductor length;

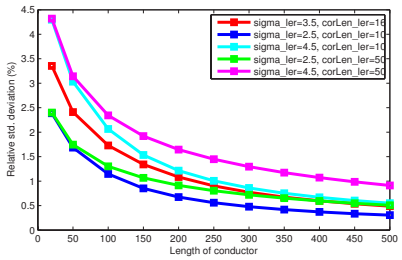

Fig. 2. The mismatch ($\frac{\sigma_C}{C}$) versus conductor length with various LER parameters.

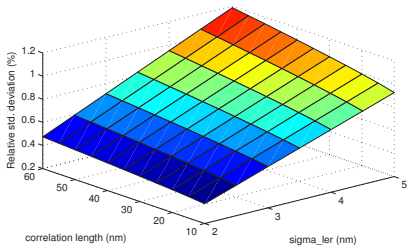

Fig. 3. The mismatch ($\frac{\sigma_C}{C}$) versus σ_{LER} and η_{LER} for a pair of $200nm$ long conductors.

2. the impact of parameters σ_{LER} and η_{LER} on $\frac{\sigma_C}{C}$.

Fig. 2 shows 5 examples of mismatch $\frac{\sigma_C}{C}$ as a function of the conductor length using the structure as in Fig. 1. Each plot is produced with a combination of various σ_{LER} and η_{LER}. All 5 plots indicate that the mismatch first drops rapidly with the increase of the conductor length and then tend to converge. Being able to identify such a trend is very helpful for certain designs with particular variability requirements. Sometimes, for instance, it is necessary to find a good tradeoff between high accuracy (i.e. small mismatch thus longer conductor length) and low power consumption (i.e. small layout area thus shorter conductor length). Then, the proposed modeling method provides a convenient tool to estimate the expected mismatch.

However, analyzing only 5 combinations of σ_{LER} and η_{LER} is far from enough for a real mismatch analysis. This is because these parameters are highly technology-dependent, thus any change from the fab could result in a different estimation of them. Besides, the measurement based estimation is normally given as a range but not a specific value. Hence the statistical modeling of mismatch should use two *sweeping* parameters (σ_{LER} and η_{LER}) instead of two particular values. Fig. 3 shows the simulation results of mismatch with sweeping parameters using the proposed method, which costs about an hour. For MC simulation, this would have taken 43 days.

From Fig. 2, Fig. 3 and the above discussion, one can see that the proposed modeling method provides a fast and practical tool for circuit designers to estimate mismatches and optimize dimensions of critical structures accordingly.

F. A Case Study

Following the experiment in the previous subsection, this section shows a real design case that can benefit from the pro-

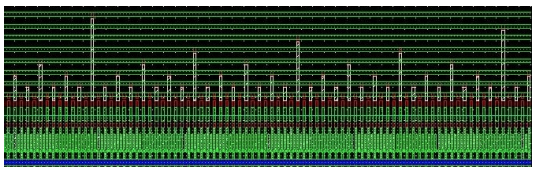

Fig. 4. Partial layout of the 8-bit binary-scaled charge-redistribution DAC.

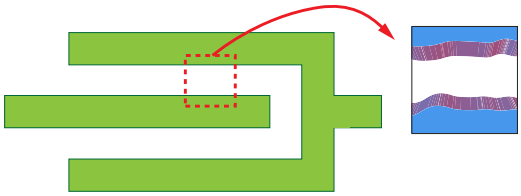

Fig. 5. The $0.5fF$ unit capacitor implementation, with a zoom-in window for indicating the LER effect.

posed statistical modeling method.

Fig. 4 shows a partial layout of an 8-bit binary-scaled charge-redistribution DAC, which is a component of a SAR ADC [7]. The designers have implemented the binary-scaled capacitors $C_{7,\ldots,0}$ with $255(=2^8-1)$ identical unit capacitors. The values of the capacitors have been minimized for high power efficiency. Thus a custom metal-metal unit capacitor, as illustrated in Fig. 5 with an extremely small value of $0.5fF$ is created by the designers.

The major consideration regarding this implementation is the mismatch of these unit capacitors due to their very small nominal values. In this case of a metal-metal structure, the sidewalls of two metals facing each other are the main contributions of the intended parasitic capacitance. In other words, the distance between the sidewalls of the conductors is a crucial parameter. Hence, the LER effect is considered to be the main cause of this mismatch (see Fig. 5).

For this design with an 8-bit resolution, a unit-capacitor mismatch ($\frac{\sigma_C}{C}$) of less than 1% is required. Our simulation result using the proposed modeling method estimates the mismatch caused by the LER to be around 0.25%. While not being able to get the estimation of σ_{LER} and η_{LER} from the technology based on which the chip has been fabricated, the estimation from IMEC (13) is used for this simulation, as it is the closest measurement data available on a similar scale technology. Although there unavoidably are also other random variations during the manufacturing process, considering LER is the primary contributor, the design should have enough margin to be fabricated. In the end, measurements on 9 sample chips indicate a random mismatch of the unit capacitors better than 0.6%. Since the measured mismatch includes various fluctuations and noises from all aspects during the fabrication and the measurement processes, it agrees well with the simulation results. Only with a proper modeling tool as proposed, the designers can confidently make such a small-size high-precision design, as the matching is a major requirement to successfully achieve the desired performance.

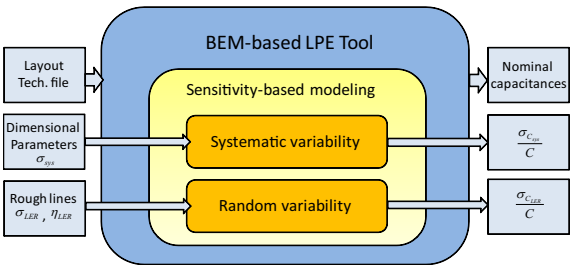

Fig. 6. Diagram of the proposed sensitivity-based method integrated in BEM-based LPE tools for both systematic and random variabilities.

IV. Sensitivity Based Modeling for Both Systematic and Random Variations

From Section II and III, the following observations can be made:

1. Nominal capacitances are computed with the partial short-circuit capacitances $\bar{\mathbf{C}}_\mathbf{s}$, using an incidence matrix (3) and (4);
2. The dimensional sensitivity for modeling systematic variabilities is computed by assembling the associated panel sensitivities (8);
3. The statistical modeling for random variation LER also counts on combinations of the panel sensitivities (12);
4. The computation of panel sensitivities solely relies on $\bar{\mathbf{C}}_s$.

From these observations, one can conclude that: a sensitivity-based algorithm can be developed to model both the systematic and the random variabilities with only ONE system solve, integrated with the standard capacitance extraction. This is illustrated with a diagram (see Fig. 6). The sensitivity-based modeling method can be integrated in BEM-based LPE tools to account for both variabilities simultaneously. With the additional inputs of the dimensional parameters with their process spreads (σ_{sys}), and the interesting rough lines characterized with σ_{LER} and η_{LER}, the resulting statistical properties of the capacitance $\frac{\sigma_{C_{sys}}}{C}$ and $\frac{\sigma_{C_{LER}}}{C}$ can be obtained together with the nominal capacitance with one system solve.

Note that the input for the systematic variability can be multiple dimensional parameters, including the widths of all conductors, the thicknesses of all metal layers and the heights of all dielectric layers. Windowing technique can be applied to handle large structures. Similarly, the input for the random variability represented by LER in this paper can be multiple rough lines with different characterizing parameters σ_{LER} and η_{LER}. Most importantly, this can all be done with one system solve with an additional computational time being a small portion of that for a standard solve without considering any variability.

To demonstrate the proposed sensitivity-based modeling method for both systematic and random variabilities, an illustrative example is conducted. As before, consider a structure with two parallel conductors with the width/space being $2\mu m/2\mu m$, the thickness being $2\mu m$ and the length being $8\mu m$. It is assumed that all four edges along the conductor in the length direction are suffering from the LER. The characterizing parameters are $\sigma_{LER} = 0.03\mu m$, $\eta_{LER} = 2.00\mu m$ for

TABLE II
SIMULATION RESULTS AND CPU TIME FOR BOTH SYSTEMATIC AND RANDOM VARIATIONS

	MC simulation	Proposed model
$\frac{\sigma_{C_{sys}}}{C}$	2.22%	2.05% (7.72% error)
$\frac{\sigma_{C_{LER}}}{C}$	0.21%	0.24% (14.23% error)
$\frac{\sigma_{C_{sNr}}}{C}$	2.22%	2.06% (7.18% error)
CPU Time	$38h52'$	$58''$

one conductor and $\sigma_{LER} = 0.04\mu m$, $\eta_{LER} = 2.88\mu m$ for the other. With this experiment, it is also interesting to compare the impacts of the systematic and the random variations on capacitances. In order to do so, it is necessary to take the conductor width as the geometric parameter for systematic variations, with a standard deviation (σ_{sys}) being the same as the associated σ_{LER}, i.e. $0.03\mu m$ and $0.04\mu m$ for the two conductors respectively. All parameters in this example are chosen based on pure assumptions.

To verify the accuracy and the efficiency of the proposed method, three Monte Carlo (MC) simulations with 1000 samples each, are performed for the systematic variation, the random variation and a superposition of them respectively (3000 samples in total). Since systematic and random variations are resulting from different sources during the manufacturing process, they are often considered independent. Hence, the proposed model estimates their superposition effect as

$$\frac{\sigma_{C_{sNr}}}{C} = \sqrt{\left(\frac{\sigma_{C_{sys}}}{C}\right)^2 + \left(\frac{\sigma_{C_{LER}}}{C}\right)^2}. \qquad (14)$$

Simulation results are shown in Table II. The errors of the relative standard deviations of the capacitance given by the model are less than 15% compared to the results of MC simulations. Also notice that the systematic variation is the dominant one, given the same standard deviation of parameters as for the random variation. Thus, for designs that are sensitive to both variations, attentions should be mainly paid to improving the systematic variability. On the other hand, some designs, for instance the 8-bit DAC, are only vulnerable to random variations. Therefore, being able to distinguish the two variations and apply the appropriate modeling technique is essential.

One can see from this experiment as well as the one in Section III.E, that the extremely high efficiency of the proposed method enables the possibility to analyze, from various aspects, the mismatches of the capacitance caused by both systematic and random variations. With a good enough accuracy for most application purposes, this method provides a fast and useful tool for Design-for-Manufacturability (DFM).

V. CONCLUSION

In this paper, a sensitivity-based modeling method is presented to capture the effects of the systematic and the random geometric variations. The nominal value of the capacitance as well as its statistical properties accounting for both variations can be obtained with only one system solve of capacitance extration. The additional computational time is negligible compared to that of a standard system solve without considering any variation. This highly efficient modeling method is very convenient for studying manufacturing variabilities and can be a useful extension of BEM-based LPE tools for DFM purposes.

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