A Precise SystemC-AMS Model for Charge Pump Phase Lock Loop Verified by its CMOS

Tao Xu, Huib Lincklaen Arriëns, Rene van Leuken, Alexander de Graaf *

***Abstract*—SystemC-AMS as an extension of SystemC provides the essential capability to describe a mixed-signal heterogeneous system, so that a virtual-prototype model can be generated to help analyze a whole mixed-signal system and further guide the circuit design. This paper presents a novel SystemC-AMS model of a high frequency Charge Pump Phase Lock Loop, including digital models like Phase/Frequency Detector and clock N-divider, and analog models like Charge Pump, Low Pass Filter and Voltage Controlled Oscillator. In order to prove the model's accuracy, the SPICE simulation result from the corresponding CMOS circuits based on the same structure of these models is used for comparison, and PLL SystemC-AMS model is validated.**

***Index Terms*—SystemC-AMS, Charge Pump, PLL, CMOS**

I. Introduction

When designing a high-speed mix-signal CMOS circuit, more complexity and unforeseen factors occur and it is not wise to analyze the performance after the layout design which takes a long time. SystemC-AMS as an extension of SystemC provides the essential capability to describe a mix-signal heterogeneous system [1], so that a virtual-prototype model can be generated to help analyze a whole mix-signal system and further guide the circuit design. To design a high-speed Charge Pump Phase Lock Loop(CP-PLL) is an example of proving SystemC-ams as a function of the bridge between the high-level system analysis and the specified bottom CMOS design. To approach a more precise result about this CP-PLL model, the key components are described at a low level in SystemC-AMS while others are at a high level. To prove the veracity, the simulation from SystemC-AMS model has to be compared with the waveforms of the real CMOS circuit, and then some modifications to the model may be necessary.

II. Charge Pump Phase Lock Loop Theory

A basic Phase Lock Loop(PLL) contains Phase/Frequency Detector(PFD), Low Pass Filter(LPF) and Voltage Controlled Oscillator(VCO). If PLL is used to multiply clock frequency, a clock divider is also included. A Charge-Pump PLL(CP PLL) inserts a charge pump between the PFD and LPF.

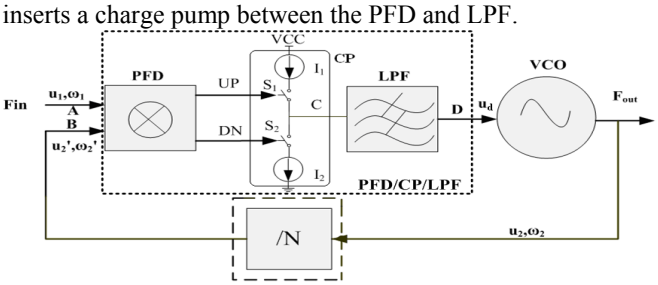

Fig. 1. A Charge Pump PLL Blocks

Here u_1 and ω_1 at A point are the input reference clock and its angular frequency; u_2 and ω_2 are the feedback clock and its angular frequency. The outputs of PFD, which are two boolean signals UP and DN, controls the switches within CP and further performs the charging or discharging operation. Normally the charging current I_1 and discharging current I_2 are the same constant called I_S. Grouping PFD, CP and LPF, their output is u_d, and if the divider is ignored, then $u_2' = u_2$ and $\omega_2' = \omega_2$ at B point.

When there is a phase difference Φ by ω_1 before ω_2 at time t=0, then a boolean UP=1 with a width $\Phi T/(2\pi)$ as T is u_1 period time. If a capacitor C_P is adopted for LPF, the charging current I_S will increase the voltage on the C_P by $(Is/Cp)\Phi T/(2\pi)$ and while Φ keeps unchanged, then u_d will response approximately as a linear function with a constant slope. If ω_1 is behind ω_2, the same situation happens but with a negative slope.

$$u_d(t) = \frac{I_S \cdot \phi}{2\pi C_P} t \cdot u_0(t)$$

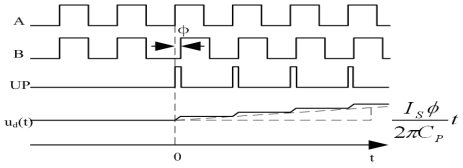

Fig. 2. Linear Function of PFD/CP/LPF

Therefore the whole PLL can perform as a linear system and its closed transfer function can be attained according to Fig.3.

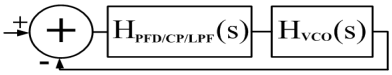

Fig. 3. A Closed Loop Transfer Function

Usually 3rd-order PLL is adopted and a detail analysis about the 3rd-order PLL is given in [4], and an additional small C_g is introduced to reduce the ripple on its output u_d [2][4][5] shown in Fig.4.

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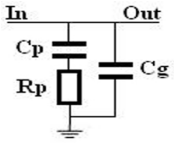


Fig. 4. LPF Practical Circuit

If Cg <0.2Cp [3][4], 2nd order PLL can approximately analyze the performance of a 3rd-order PLL

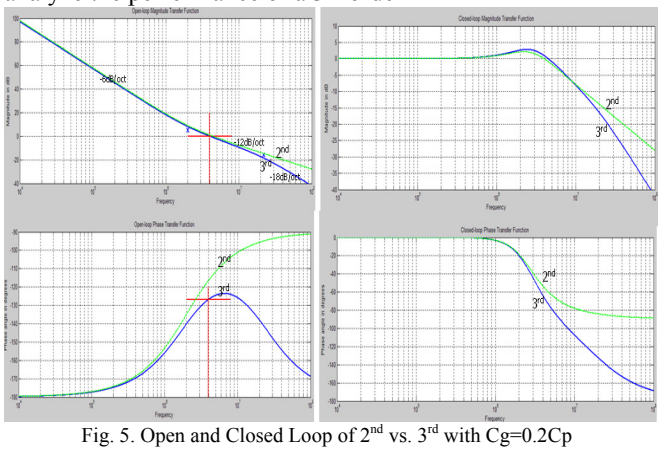


Fig. 5. Open and Closed Loop of 2nd vs. 3rd with Cg=0.2Cp

Then transfer function and some intermediate variables for a 2nd order PLL are shown below,

$$H_{PLL}(s)|_{open} = \frac{I_S}{2\pi}\left(R_P + \frac{1}{C_P \cdot s}\right)\frac{K_{VCO}}{s}$$

$$H_{PLL}(s)|_{closed} = \frac{\frac{I_S K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_S K_{VCO} R_P}{2\pi} s + \frac{I_S K_{VCO}}{2\pi C_P}}$$

$$\omega_n = \sqrt{\frac{I_S K_{VCO}}{2\pi C_P}}, \quad \zeta = \frac{R_P C_P}{2}\omega_n$$

Here ω_n is the VCO natural angular frequency, and ζ is the PLL damping factor.

Given K_{vco}, the VCO gain, I_S, the (dis)charging current, At meantime since $I_S K_{VCO} > 0$ the poles of $H_{PLL}(s)|_{closed}$ are

$$s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$

Therefore, in the real design, only choose R_P and C_P carefully in order to make that $\zeta \approx 1$. If $\zeta \ll 1$ then the complex $S_{1,2}$ poles make PLL instable, and if $\zeta \gg 1$ then the convergence time will be long and the locked status will be harder to be acquired.

III. SystemC-AMS Models for PLL

SystemC-AMS can describe a mixed signal system at a high level and also can provide a detail description about specified networks or at a register transfer level. The charge pump(CP) and low pass filter(LPF) are characteristic for a CP-PLL[6] and determine the performance of the whole PLL. To improve the accuracy, describe CP/LPF in detail in a low circuit level while other parts are abstracted at a high level.

A. Phase/Frequency Detector

According to the theory, the function of a PFD in CP-PLL is to detect the difference between the reference clock ω_1 and the feedback clock ω_2 and produces "UP = 1, DN = 0" when ω_1 is ahead of ω_2 or "UP = 0, DN = 1" when ω_1 is behind ω_2. Based on Fig.3, the digital PFD is described in SystemC.

The kernel idea here is to subtract ω_1=ref and ω_2=fdbk at the rising edge of either of input signals, and then certain pulse is generated when there is difference between 'ref' and 'fdbk'. A simulation result of this PFD is shown in Fig.6, which displays a consistent waveform as its theory.

```
SC_MODULE(phd) {
  sc_in<bool>  ref,  fdbk;
  sc_out<bool> UP,  DN;
  double diff;
  void sig_proc() { ...      ...
  diff = ref_binary - fdbk_binary;
     if(diff >  0) {UP.write(true); DN.write(false); }
     else if (diff < 0) {UP.write(false);DN.write(true); }
     else{UP.write(false); DN.write(false); }     }
  SC_CTOR(phd) {
   SC_METHOD(sig_proc)
    sensitive_pos << ref;  sensitive_pos << fdbk; }};
```

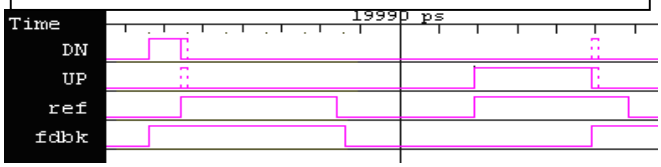
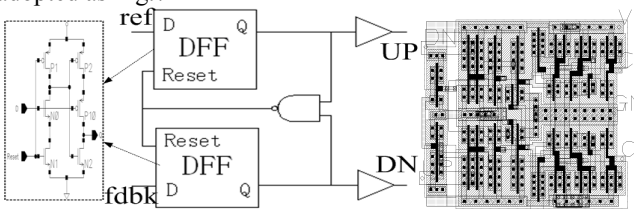
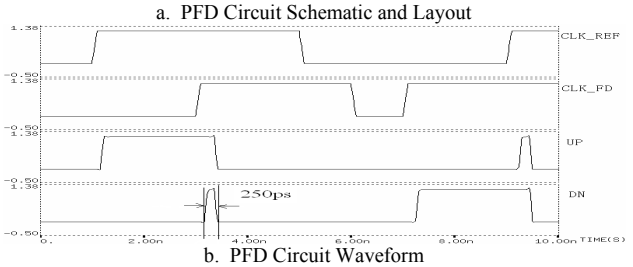


Fig. 6. PFD SystemC Model Simulation

For its circuit counterpart, a classical structure[5][9] is adopted as Fig.7



a. PFD Circuit Schematic and Layout



b. PFD Circuit Waveform

Fig. 7. PFD CMOS Circuit

Comparing Fig.6 and Fig.7b, the main function is demonstrated the same, but there is an additional pulse with a width of around 250ps on UP or DN in the layout simulation when it's zero in the SystemC abstracted simulation. This is caused by the intrinsic timing delay of a MOS DFF device, which will not influence the performance of the PFD but benefit its sensitivity[5].To modified SystemC model purposely, the dotted line in Fig.6 can be generated.

B. Voltage Controlled Oscillator

The output frequency of VCO is determined by the input

controlled voltage(Vc) u_d in Fig.1. Defining VCO linear dynamic range △f, its central frequency $f_0=2\pi\omega_0$ and the range of its controlled voltage △Vc, then

$$K_{VCO}=\frac{\Delta f}{\Delta Vc}[Hz/V],\quad f_{VCO}=f_0\pm\frac{\Delta f}{2}$$

Considering Vc∈[0.1,0.5], f_0=1.25GHz and △f=500MHz as the dotted line in Fig.8 and . After the circuit design as Fig.10, actually Vc ∈ [0.09,0.4] and △ f=470MHz then $K_{VCO}=1.48\times10^9$[Hz/V]. Then The SystemC-AMS code in the abstracted level for this VCO is attached below.

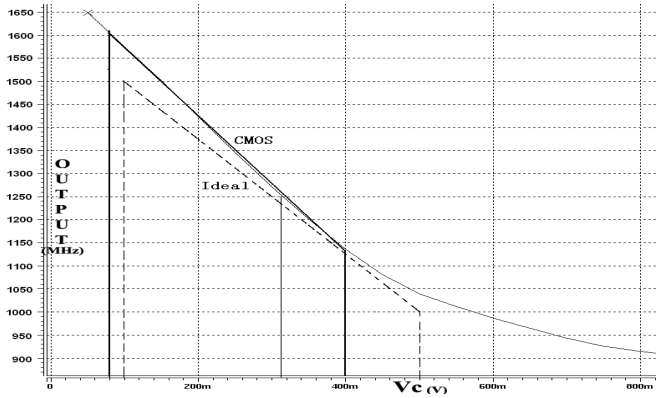


Fig. 8. VCO Dynamic Range

```
SCA_SDF_MODULE(vco) {… …
double kvco_Hz;//sensitivity [Hz/V]
double fc;    //central frequency [Hz]
double vfc;   //control voltage when output fc
void init() { th_mulfac = 2.0*M_PI * 1e-12;//1ps
void sig_proc() {
 ctr_v = Vc- vfc; //Vc: input voltage
 fvco = (fc - kvco_Hz*ctr_v);
 theta += th_mulfac*fvco;//2*pi*fvco*1ps
 wave=sin(theta + cont * bias);
… …} };//sine into square wave
```

A simulation of this VCO SystemC-AMS model when controlled voltage Vc=0.3V is shown in Fig.9, and the sine wave here is the VCO output before a shaping operation.

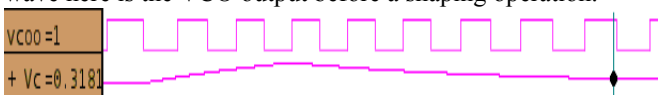
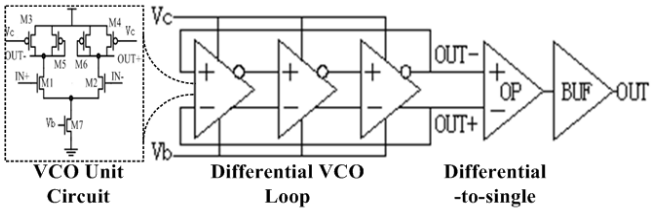
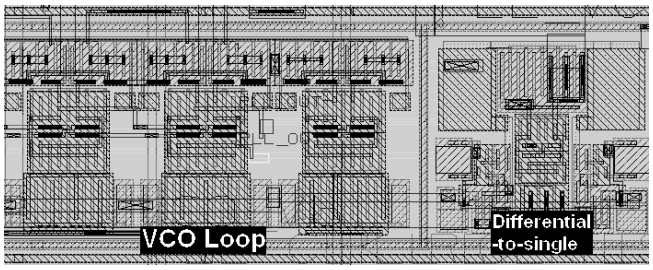


Fig. 9. VCO SystemC-AMS Model Simulation

For its circuit counterpart, an analog 3-stage differential VCO[14][15] is used in Fig.10



a. VCO Circuit Schematic



b. VCO Circuit Layout

Fig. 10. VCO CMOS Circuit Layout

A simulation based on the RC-extracted SPICE netlist from VCO layout shows the same as Fig.9 and an expected 1.25GHz output with the central controlled voltage Vc=0.31V.

C. Clock Divider

A clock divider is an optional element in Fig.1 for a CP-PLL, but when CPPLL is aimed to multiply the clock frequency, a clock divider must be involved. When N=10, a 125MHz reference clock is needed while VCO output 1.25GHz.

```
SC_MODULE(divider) {  … … … …
  sc_signal<sc_uint<4> >  inter;
  void sig_proc() {
     inter =  inter.read() + 1;
     if (inter.read() == 9)
     {  clkout = ! clkout.read();  // 1/10 divider
        inter.write(0); }  }
  SC_CTOR(divider) {
   SC_METHOD(sig_proc)
    sensitive_pos << clkin;}};
```

The above SystemC code is for this 1/10 divider, and its simulation is shown in Fig.11.

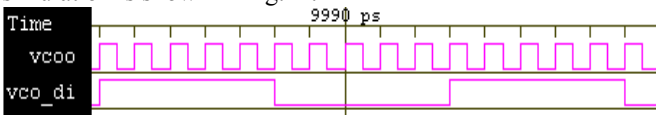


Fig. 11. 1/10 Divider SystemC-AMS Model Simulation

This SystemC code can be synthesized into a digital circuit and the simulation result keeps the same.

Because the N=10 divider is included, the parameter K_{VCO} in transfer function $H_{PLL}(s)|_{closed}$ should be replaced by K_{VCO}/N.

D. Charge Pump and Low Pass Filter

A basic Charge-Pump is shown in Fig.1, but a significant shortcoming of the 3rd-order CPPLL is that there is a voltage drop on the resistor R_P which causes impulses on the controlled voltage of VCO. To compensate this, an equipotential connection is one solution [5][7][8] shown in Fig.12, where SystemC-AMS network model is attached.

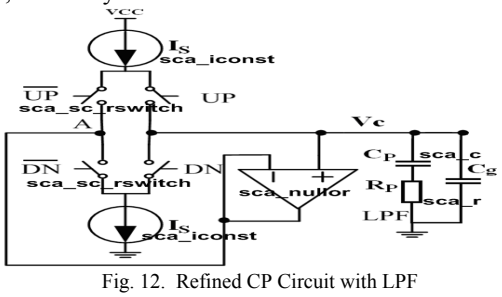


Fig. 12. Refined CP Circuit with LPF

Here Is=20uA is assumed, and N=10, K_{VCO}=1.48 *10^9[Hz/V] are known. Considering C_P=8pf and R_P=10kΩ, then PLL damping factor: ζ = 0.769≈1.

Fig.13 shows the simulation result of CP-LPF model, from which a smooth rising or falling on the controlled voltage (Vc) is seen.

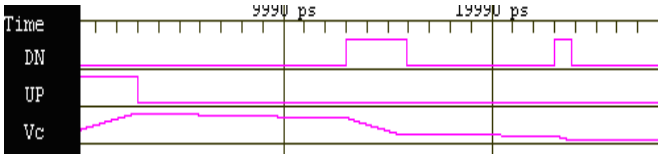


Fig. 13. CP-LPF SystemC-AMS Model Simulation

As mentioned before, this part is described in a low level in SystemC-AMS, and its circuit counterpart adopts the same structure as Fig.14 and the simulation keep as same as Fig.13.

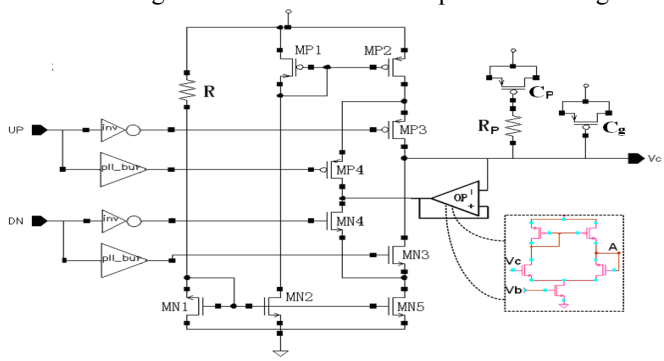


Fig. 14. CP-LPF CMOS Circuit

E. Integration of CP-PLL

So far, all the components in this CP-PLL are introduced and here they are integrated into a loop. Under the condition of that C_P=8pf, R_P=10kΩ, Is=20uA, N=10 and K_{VCO}=1.48 ∗10^9Hz/V, with a 125MHz reference clock input, a SystemC-AMS model is shown below and its simulation is shown as Fig.16aTo compare the performance of the whole loop, its circuit counterpart is also designed in 130um CMOS process as Fig.15, and the simulation of its RC-extracted SPICE netlist of CPPLL CMOS layout is shown as Fig.16b.

```
SC_CTOR(CPPLL){
phd i_phd("phd");
  i_phd.in1(ref);
  i_phd.in2(vco_di);
  i_phd.UP(UP);
  i_phd.DN(DN);
cp_lp i_cp_lp("cp_lp");
  i_cp_lp.UP(UP);
  i_cp_lp.DN(DN);
  i_cp_lp.out(Vc);
vco i_vco("vco");
  i_vco.in(Vc);
  i_vco.out(vcoo);
  i_vco.out.set_T(sc_time(1.0, SC_PS));
  i_vco.kvco_Hz = 1250e9;
  i_vco.fc      = 1250e6; //1.25GHz
  i_vco.vfc     = 0.31;//0.31V
  i_vco.jitter  = 1e6; //0.1%
divider ck_div("divider");
  ck_div.clk(vcoo);
  ck_div.clkout(vco_di); )
```

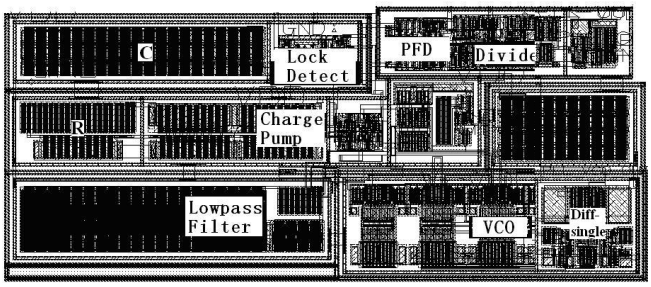
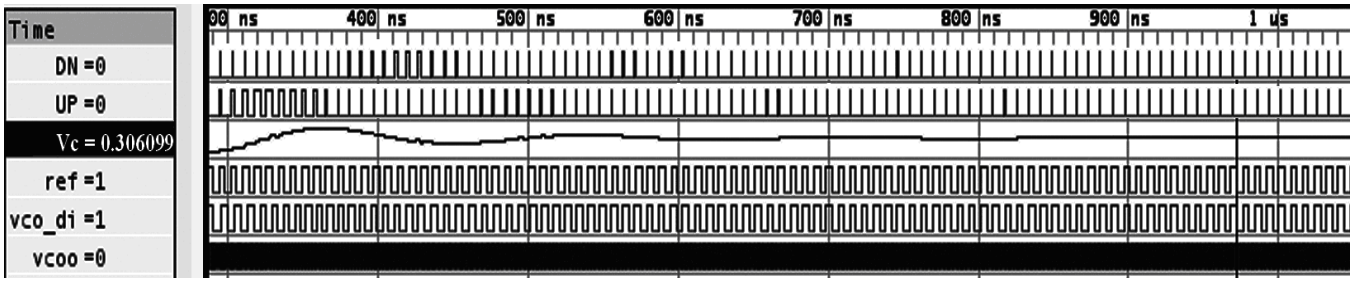
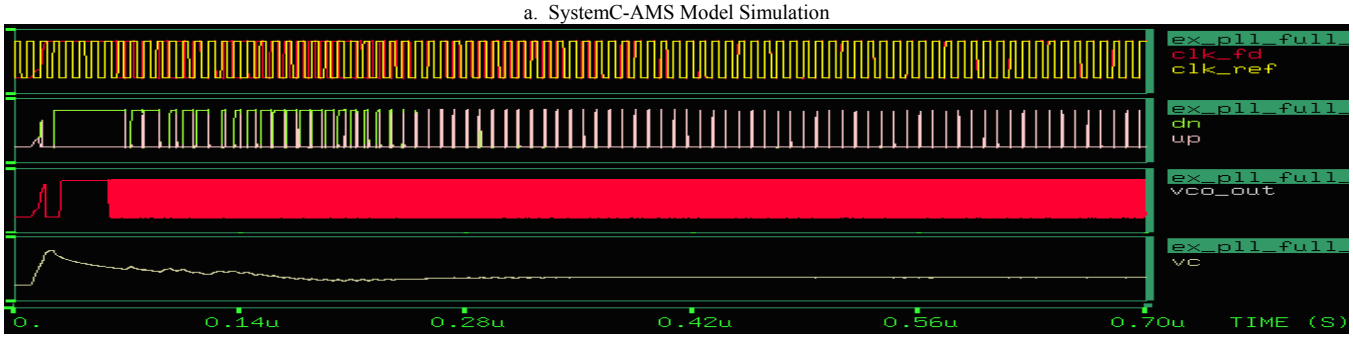


Fig. 15. CP-PLL CMOS Circuit Layout

Comparing this waveforms and Fig.16a and b, they prove the same function as PLL, but with several differences.



a. SystemC-AMS Model Simulation



b. CMOS Circuit Simulation

Fig.16 CP-PLL Simulation

The rudimental pulse on UP/DN signal was explained before and can be kept the same at high level description in SystemC-AMS.

But a significant distinctness between SystemC-AMS model and the CMOS circuit result is the locked time of CPPLL which is inflected from the waveform of the controlled voltage Vc. In fact the locked time is determined by its damping factor ζ, and this ζ is influenced by R_P and C_P, that was discussed in former section. In our CMOS circuit design, a polysilicon rectangle is to realize the resistor and a PMOS junction capacitance is to realize the capacitor, then it is hard to produce a precise resistor and capacitor with low costs, because the values of these R_P and C_P depend on the CMOS process parameters which vary along with many factors like temperature. And also the parasitical RC parameters in the CMOS layout and devices will influence change R_P and C_P too. Therefore it is improbable to make the locked time of a SystemC-AMS model at a high level and the locked time of this CMOS circuit exactly the same all the time. However their locked times are in the same time-level, of around from 400ns to 800ns, and this is enough for a system designer.Another difference is the initial status of these two simulations. For SystemC-AMS model, it's deterministic at the initial stage but for a mixed-signal CMOS circuit, it's hard to attain all its initial status although the SPICE simulation can set initial point for its netlist. However this difference doesn't influence the performance of the PLL.

From a high level, the SystemC-AMS model is considered to be the same as its CMOS circuit counterpart at the interface when PLL is stable.

IV. OFF-CHIP TEST MODEL

High frequency output should be tested through certain wired channel, so an off-chip test model in SystemC-AMS is needed sometimes. Paper[19] gave an insight reference to model the channel in Systemc-ams, and further provided a method to transfer the standard IBIS model of the package into a Systemc-ams file. And report[20] provided information about how to deal with an IBIS model for high-speed LVDS interface.

In this paper a basic LVDS driver and a symmetrical segment for the distributed double-wire model with simple package model are described as Fig.17.

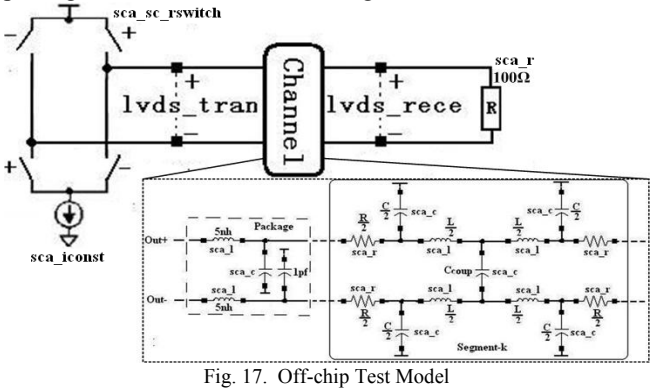


Fig. 17. Off-chip Test Model

On the wire channel, the self-resistance **R**, self-capacitance **C**, self-inductance **L** and the mutual-capacitance **Ccoup** on a Printed Circuit Board(PCB) are calculated[21] as below, while the mutual-inductance is ignored:

$$R = 0.641 \cdot \frac{l}{\omega}[m\Omega], \quad C = 0.0885 \cdot \frac{\omega}{H}[pF/cm]$$

$$L = 0.002 \cdot \ln(\frac{8T}{\omega} + \frac{\omega}{4T})[\mu H/cm],$$

$$C_{coup} = \frac{0.0885\pi}{\cosh^{-1}(D/T)}[pF/cm]$$

Here T is the wire thickness, H is the height of this wire layer above the power/group plane, w and l are the width and the length of the wires.

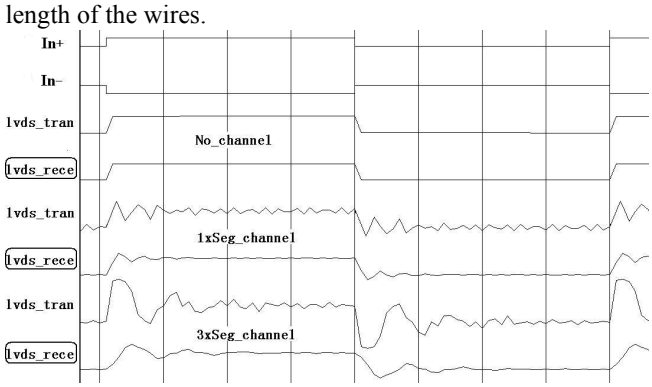


Fig. 18. Simulation with Wire Channel

From this graph, it can be known that the performance gets worse when more channel segments are involved so that certain equalization circuits are needed before the LVDS driver if PLL outputs off-chip clocks.

V. CONCLUSION

A precise SystemC-AMS modeling for a CP-PLL is designed in detail, and its simulation is compared with the waveform from its CMOS circuit. Their consistency proves the accuracy of the CPPLL model when PLL is stable. A simple wired channel and LVDS driver in SystemC-AMS as an off-chip test model is also mentioned.

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