Transistor-Level Waveform Evaluation for Timing Analysis

Qin Tang, Amir Zjajo, Michel Berkelaar, Nick van der Meijs
Circuits and Systems Group, Delft University of Technology
Q.tang@tudelft.nl

***Abstract*—In (Statistical) Static Timing Analysis, one of the crucial steps in gate level design flow, delay modeling has focused on gate-level models. However, the black-box property of the gate-level models introduces limitations for the accuracy of timing analysis, especially in nanometer technology. In this paper, we present an efficient transistor model (Xmodel) to build up gate models, which, benefiting from transistor-level details, is independent of input waveform, output load and circuit structures. Additionally, the proposed model provides both high accuracy and efficiency in comparison with Spice/Spectre for all analysis scenarios including multiple-switching, and for all cell types including cells with high stacks. We also present a statistical extension of the proposed model (SXmodel) since the parameter variations are not negligible any more for nanometer technologies. Using General Threshold (GVT) library in Nangate 45nm package, experiments showed high accuracy and efficiency of the proposed gate modeling and waveform evaluation methodology.**

Keywords- transistor-level, gate modeling, timing analysis, statistical, parameter variation.

I. Introduction

The simulation of logic gates, the basic blocks of digital circuits, is of paramount importance in macrocell/block characterization and (statistical) static timing simulation (S/STA). By using gate-level models (GLMs) such as CCS [1] and ECSM [2], S/STA calculates delay and slew much faster ignoring accurate waveform information. GLMs model delay and slew as a function of input slew and output effective capacitance (C_{eff}) for a given cell arc and store the characterized data in lookup tables (LUTs) or polynomial functions. In nanometer technology, however, the intrinsic limitations of GLMs significantly affect the S/STA accuracy and efficiency. Firstly, the simple saturated ramps can no longer represent the input signals since the shape of signal waveform starts to be affected by process variations and other variabilities such as crosstalk noise. Secondly, GLMs fail to work with a multi-port coupled interconnect load because the load is simplified and modeled only by C_{eff}. Additionally, GLMs fail to efficiently capture multi-input switching (MIS) and internal charge effects for high-stack and complex cells. Not modeling MIS for timing would result in as much as 100% error in stage delay and slew calculation [3].

Lately, intensive research efforts are being made to address the above issues. With recent proposals of optimized GLMs, there is a clear trend to sacrifice some performance, mostly adding complexity, to improve accuracy. In [3] and [4], gate delay and output slew are modeled as a function of node voltages to capture full waveforms and MIS scenario. The work in [3] has been extended in [5] by exposing internal nodes as virtual ports to model the internal states of the cell. All these works attempt to optimize GLMs to maintain acceptable accuracy for all types of gates. Unfortunately, the fact that GLMs are black-box models, where the internal structure of the gates is hidden, is the essential root of all these issues.

Clearly, an efficient modeling and waveform evaluation approach that is accurate within a few percent of Spice/Spectre, uniformly for all gate types and arcs, is required for nanometer technology. Combined with advanced algorithm and proper utilization of available computer resources, it becomes practical to use transistor-level cell models in multi-million gates STA runs [6]. In nanometer technology, however, the sophisticated transistor model (e.g. BSIM4) evaluation dominates and dramatically slows down the Spice/Spectre simulation, which makes it impractical for timing analysis. Therefore, an efficient and accurate transistor model is a key component for transistor-level waveform evaluation for timing analysis. In this well-studied field, it has been recognized that LUT-based models combined with advanced interpolation methods can provide both accuracy and speed.

The $3D$ tabular drain-current model for a single transistor for precise circuit simulation [7] and the corresponding monotonic piecewise cubic interpolation method demonstrate the speed [8] and accuracy [9] advantages of the LUT-based model, in both digital and analog applications, in comparison to the conventional analytical models. The LUT-based models have also been used for RF circuit simulation [10], SOI devices [11] and timing analysis [6], [12], [13]. In the LUT approach, the exact behavior of the device is accounted for without any approximations, and thus the long and difficult analytical model development phase is avoided. Furthermore, the LUT approach is independent of technologies since the data are measured or simulated from sufficiently accurate models. In general, the transistor model requires accurate representation of both the transistor's current sources and the intrinsic capacitances. Nowadays, the analytical model [12] or a single value [6] are still the dominant methods for capacitance modeling in transistor-level timing analysis, which is either too complicated or too simplified. The LUT approach is a potential alternative for capacitance modeling for the accuracy and computation time trade-off [14].

In most well-known circuit simulation programs (e.g. Spice), a numerical integration method is used to convert

the nonlinear differential equations to nonlinear algebraic equations for time-domain waveform evaluations, and then Newton-Raphson (NR) method is applied for the nonlinear solver. Since the NR method requires C^2 conditions (first and second derivatives of the system are both continuous), the interpolation method suitable for LUT approach has been developed. Linear interpolation is not recommended for NR method since it only meets C^0 condition. The monotonic piecewise cubic interpolation method was originally proposed in [8] and has been widely used in this field. Although the interpolation method assures both the smoothness and the monotonicity of drain current, it also introduces complexity and longer simulation time. A simple and fast piecewise linear interpolation and corresponding compatible nonlinear solver could provide both accuracy and speed advantages.

In this paper, we propose an accurate and technology-independent transistor model (Xmodel) and its statistical extension (SXmodel) for gate modeling and a waveform evaluation methodology. In our model, each transistor in a gate is represented by the Xmodel composed of a DC current source and a set of intrinsic capacitances. Additionally, we also introduce the construction method for LUTs, as well as the waveform evaluation algorithm for timing analysis. The sizes of tables are optimized according to the specific characteristics of current and every capacitance in the model. A discrete waveform model, piecewise linear interpolation and specific extrapolation methods combined with Broyden's nonlinear solver guarantee the efficiency of the waveform evaluation.

II. Accurate LUT-based transistor model

The proposed statistical SXmodel represents each transistor by a nominal current source I_{ds}, a statistical current source $\delta_{i_{ds}}$ caused by process variations and five parasitic capacitances which have statistical parts with respect to any statistical parameters of interest as well. The SXmodel representation is shown in Fig. 1, where Δ_p is the process variation vector. The nominal current source $I_{ds}(t)$ and capacitances without process variations compose the proposed Xmodel.

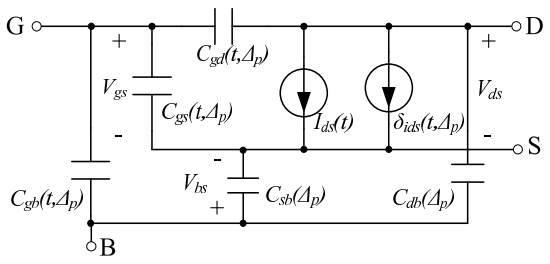


Fig. 1. The proposed SXmodel for gate modeling

A. MOS transistor drain current modeling

Generally, the MOS transistor drain current (I_{ds}) is modeled by compact models like BSIM4 at 45nm and below. With several hundred process parameters, BSIM3/4 determines drain current and sixteen intrinsic capacitances by solving complex equations, which are functions of the process parameters in the model. The physical properties are accurately represented by those parameters, however, the huge amount of computation time makes it impractical for fast timing analysis. In order to capture the main effects while still maintain the simple formulas, we previously proposed a BSIM4-based simplified analytical model in [15] for 45nm PTMLP technology. Although this model is accurate and efficient for most of the standard cells, the accuracy of the model in [15], when applied to the high-stack complex gate cells is limited due to: i) when V_{gs} is smaller than V_{th} by a small amount, I_{ds} is under-estimated; ii) the effect of V_{bs} on some parameters like mobility, early voltage, etc. is ignored except V_{th}. Avoiding approximating data to expressions, the model proposed in this paper addresses these issues by directly using measured or simulated data. Moreover, in comparison with advanced analytical models, the proposed table-based model gains significant speed advantage, by using the efficient interpolation and extrapolation methods and resourceful implementation of LUT sizes.

In nanometer technology, V_{th} is not only a function of V_{bs} but also V_{ds}, which implies that a $2D$ LUT for I_{ds} with entries V_{ds} and $V_{gs}-V_{th}$ is not practical. The influence of V_{bs} on I_{ds} is not just represented by V_{th} which is assumed independent of V_{ds} [7]. In the Xmodel, we use a $3D$ LUT for I_{ds} determined by three operating voltages: V_{gs}, V_{ds} and V_{bs}.

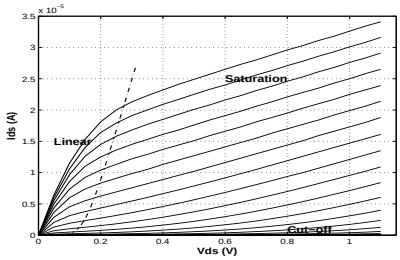


Fig. 2. The nonlinear properties of minimum-sized NMOS device

A simple piecewise linear interpolation method is adopted for current continuity and computation saving (section III). For memory-capacity and accuracy trade-offs, the table sizes and extrapolation method are optimized. The $I_{ds}(V_{gs}, V_{ds})$ characteristics have almost the same shape under different V_{bs} when V_{bs} is not close to the supply voltage, implying a possibility of reducing data points corresponding to V_{bs}. For constant V_{bs}, I_{ds} displays different nonlinearity in three operating regions as shown in Fig. 2. In the linear region, the current I_{ds} increases rapidly along with V_{ds} while shows nearly linear dependence on V_{ds} with relatively much slower slope in the saturation region. In the cutoff region, however, the current is close to zero and shows a weak relationship with V_{ds} and V_{gs}. Therefore we choose more datapoints along the operating voltage V_{ds} when $V_{ds} \leq V_{dd}/2$ and 3-5 datapoints for larger V_{ds}. Similarly, we select fewer datapoints along the voltage V_{gs} when $V_{gs} \leq V_{th0} - 0.2$. According to our experiments, $V_{th0} - 0.2$ is an efficient turning point to capture the current from subthreshold to strong inversion. We observe that selecting 15-25 datapoints along the operating

voltages (V_{ds}, V_{gs}) and 5-10 sample points for V_{bs} provides an extremely accurate transistor current model justifying the storage requirements.

In the $3D$ tables, the range for every operating voltage is $[0, V_{dd}]$. A value outside the range is determined as following:

1. The value, which is in $[V_{dd}, +\infty]_{|V_{ds}|}$ and $[V_{dd}, +\infty]_{|V_{gs}|}$, is extrapolated by using the boundary condition and boundary value.
2. The value in $[-\infty, 0]_{|V_{bs}|}$ and $[V_{dd}, +\infty]_{|V_{bs}|}$ is fixed to the boundary value to avoiding reverse current.
3. The value in $[-\infty, 0]_{|V_{gs}|}$ is approximated to zero.

We generate a continuous piecewise linear surface for the current curve using trilinear interpolation [16], which is very inexpensive compared with explicit model evaluation and monotonic piecewise cubic interpolation [8] or spline cubic Hermit interpolation [9]. Note that the derivative of the current is not continuous. As a consequence, the model is not optimized for NR method. In that sense, to find the appropriate solution, the nonlinear solver proposed in section III-B avoids the derivative calculation at every iteration by replacing it with finite difference approximation.

B. Transistor capacitance modeling

The transient response of a combinational logic gate is sensitive to the transistor intrinsic capacitances in the gate. If the intrinsic capacitances are not modeled accurately, the error introduced can accumulate when the transient pulse propagates through the logic chain. GLMs model a gate capacitance to a constant value C_{eff}, ignoring the nonlinear property of the intrinsic capacitances hidden in the gate. One way to model nonlinear intrinsic capacitances is to represent them as voltage-dependent terminal charge sources (BSIM4). The sixteen capacitances of a transistor are computed from the charge by $C_{ij} = \partial Q_i / \partial V_j$ at every time step, where i and j denote the transistor terminals. Although this method may be the most accurate by means of sophisticated charge formulations, the performance and characterization runtime would be problematic for S/STA.

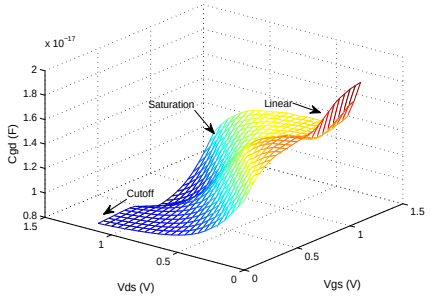


Fig. 3. Non-linearity properties of C_{gd} of a 45nm NMOS transistor

In the 45nm node and beyond, the intrinsic capacitance becomes increasingly nonlinear. As an example, C_{gd} is shown in Fig. 3. In order to accurately capture the capacitances, analytical models still play a dominant role in transistor-level timing analysis [12] - [17]. In [6], the constant capacitance values based on the initial state (cutoff or linear state) are used for the entire transition, assuming the capacitances influence the output waveform mostly at the beginning. However, the assumption would result in deviations at the end of the transition, adding errors for output slew due to the strong nonlinearity of capacitances in 45nm and below. It is clear from Fig. 3 that the capacitance in the cutoff region is much smaller than that in the linear region.

In order to improve accuracy while still maintaining good computational efficiency, Xmodel treats the five capacitances differently. The gate capacitances C_{gs}, C_{gd} and C_{gb} use $2D$ LUTs while constant values are characterized for junction capacitances C_{sb} and C_{db}. Strictly, the gate capacitances are functions of V_{gs}, V_{ds} and V_{bs} like I_{ds}. According to our observation, however, the difference between gate capacitances at maximum $|V_{bs}|$ and minimum $|V_{bs}|$ is within $3/2$ times. As a result, we select a $2D$ LUT model for gate capacitances. On average, the junction capacitances are two orders of magnitude smaller than gate capacitances, and normally, C_{db} is negligible compared to output load, so using constant values for them promises fast performance without accuracy loss. For tabular gate capacitances, 5-15 datapoints in V_{ds} and V_{gs} can provide sufficient accuracy. Bilinear interpolation is used for gate capacitances. When operating voltage $|V_{ds}|$ or $|V_{gs}|$ is outside the range $[0, V_{dd}]$, the value is fixed to the boundary value.

C. Statistical extension of Xmodel (SXmodel)

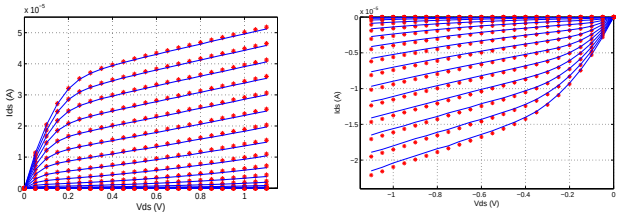
In addition to the nominal values for the dc current source and intrinsic capacitances, the statistical extension of Xmodel (SXmodel) contains the sensitivities of these model elements to any statistical parameter of interest. The statistical description of the current and the intrinsic capacitance in SXmodel are evaluated as:

$$\begin{aligned} i_{ds}(\Delta_p) &= I_{ds} + \delta_{i_{ds}}(\Delta_p) = I_{ds} + \sum_{k=1}^{m} \frac{\partial I_{ds}}{\partial p_k}|_{p_k=p_{k0}} \cdot \Delta_{p_k} \\ &= I_{ds} + \sum_{k=1}^{m} \chi_k \cdot \Delta_{p_k} \qquad (1) \\ C_j(\Delta_p) &= C_{j0} + \sum_{k=1}^{m} \frac{\partial C_j}{\partial p_k}|_{p_k=p_{k0}} \cdot \Delta_{p_k} \\ &= C_{j0} + \sum_{k=1}^{m} \zeta_k \cdot \Delta_{p_k} \qquad (2) \end{aligned}$$

where p_k is the k_{th} random parameter which is the sum of nominal value p_{k0} and random variable ξ_k with zero mean (μ) and same standard deviation (σ) as p_k. Δ_p is the the parameter deviation from the nominal value p_0 sampled from ξ. χ and ζ are the sensitivities of current and capacitance to the statistical parameters respectively. C_{j0} in (2) is the nominal value of the j_{th} capacitance in Fig. 1. The variable t is omitted in (1)-(2) for notational simplicity. Note that the correlations among the statistical variables are submissive to accuracy-speed trade-off.

The numerical sensitivity is characterized by perturbing the statistical parameter being modeled above and below (e.g. $\pm\sigma$)

its nominal value. Assume the statistical parameter is effective channel length (L) with $\sigma_L = 10\% \times \mu_L = 5nm$. Fig. 4 shows the approximated current ($*$) when $\Delta_L = 3nm$ by using the proposed SXmodel, which is sufficiently accurate compared with the drain current ($-$) simulated from Spectre.



(a) NMOS(ΔL=3nm, W=90nm) (b) PMOS(ΔL=3nm, W=135nm)

Fig. 4. Current accuracy using the SXmodel

Standard cell libraries today consist of hundreds of cells with many process corners. Therefore, GLMs require a significant amount of CPU time to characterize all the standard cells. The proposed transistor-level gate model has modest characterization requirements: it only needs to characterize the unique transistors in the cell library. It is also worth mentioning that i_{ds} and the gate capacitances are roughly proportional to W/L and WL, respectively, which gives the possibility to limit ourselves to only a few table models for each MOS type.

III. Waveform Evaluation Algorithm

Waveform representation and propagation are two essential steps for timing analysis. In this section, we first present a waveform approximation method. Based on the approximation method, we present an algorithm to generate and propagate the waveform for timing analysis.

A. Waveform Approximation

Traditionally, the saturated ramp is widely used for waveform representation in S/STA to achieve high speed. However, this model is too simple to accurately compute the transient response of complex logic gates and the real shape affected by noise and parasitics. The accumulated error introduced by the ramp model makes it unsuitable to estimate the transient response after propagating through several logic gates.

In this paper, we use discrete values of the waveform to approximate the waveform. At every defined time step, the voltage value is calculated or sampled. The time step is adaptively changed to assure efficient and accurate calculation.

B. Time-domain waveform evaluation

In general, for transistor level time-domain analysis, modified nodal analysis (MNA) leads to non-linear ordinary differential equations or differential algebraic equations systems that, in most case, is transformed to a non-linear algebraic system by means of numerical integration methods [18]. At every integration step, a Newton-Raphson-type method is then used to solve the nonlinear algebraic system. Although the Backward Euler method has been widely used in GLM-based S/STA because it leads to simpler nonlinear algebraic system, it has only first order accuracy and may cause oscillation if the system is complex. We use trapezoid rule predictor-corrector method which is explicit and has second order accuracy.

The NR method shown in Eq. 3 is employed by most simulators like Spice to solve the nonlinear system.

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \qquad (NR) \tag{3}$$

where x_n and x_{n+1} are the approximated roots at the n_{th} and $(n+1)_{th}$ iterations respectively. $f'(x_n)$ denotes the derivative of function f at the n_{th} iteration. NR linearizes the nonlinear elements and solves the resulting linearized circuit iteratively until a convergence condition is achieved. Theoretically, it has a quadratic rate of convergence with an initial estimate in the vicinity of the exact solution. In NR method (Eq. 3), both $f(x_n)$ and its derivative $f'(x_n)$ need to be evaluated at every iteration. For nonlinear devices, the runtime cost is generally the CPU time required to evaluate the device model and all of the related partial derivatives. With advanced device models (e.g. BSIM4) having several hundred parameters, this task turns out to be very expensive and dominates the overall runtime [19], especially for small to medium sized circuits. On the other hand, LUT-based transistor model significantly reduces the complexity of the model itself. Unfortunately, direct use of table-based model to speed up the waveform evaluation with the NR-based algorithm is less efficient, since it requires high-order spline methods for continuous and smooth partial derivatives [8] - [9]. In order to solve the above issues, we utilized the nonlinear system solver based on the Broyden's method [16]. In contrast with NR, Broyden's method avoids derivative calculation by replacing it with the finite difference approximation $J_n^\star$:

$$\begin{aligned} x_{n+1} &= x_n - J_n^{\star -1} f(x_n) \qquad (Broyden) \\ J_n^\star &\simeq \frac{f(x_n) - f(x_{n-1})}{x_n - x_{n-1}} \end{aligned} \tag{4}$$

The iterations for both methods are shown in Fig. 5. As seen from Fig. 5, Broyden's method could reach the solution with as few iterations as NR method. In theory, the order of convergence in Broyden's method is about 1.62. Although the order of convergence is smaller than the quadratic convergence of NR method, the cost of one Broyden iteration is relatively cheaper. As mentioned above, the NR method additionally requires continuous device model derivatives in order to avoid divergence. This continuity is usually considered in analytical transistor models at the expense of extra parameters and more complicated equations, and in table-based models by spline cubic interpolation. Furthermore, NR method can also perform a slower convergence rate with a step-limiting or damping scheme that controls the solution update [20]. By avoiding derivative evaluation, Broyden's method alleviates the requirements for table-based transistor models and therefore saves significant computation time. The convergence of Broyden's method is better than successive chord method in [12] which greatly depends on the slope value used for all iterations.

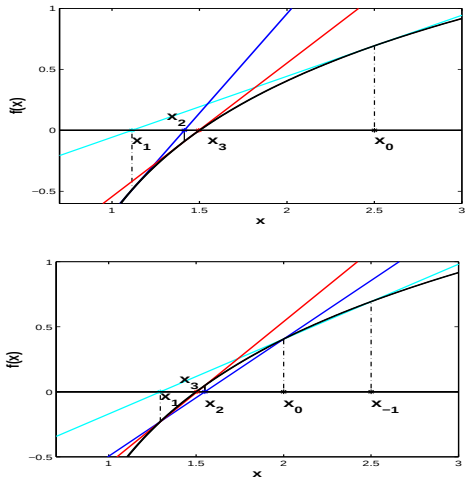


Fig. 5. Upper: NR method; Bottom: Broyden's method

In order to accurately evaluate the waveform during transition while keeping computational efficiency at the same time, we use a dynamic time step algorithm based on the finite difference approximation of the output. As initial conditions are crucial for fast convergence of Broyden's method, the initial conditions are calculated or checked (if given) in the beginning.

IV. RESULTS

The effectiveness of the proposed approach was evaluated on several most commonly used standard cells using GVT library in the latest Nangate 45nm package [21]. The Xmodel and waveform evaluation algorithm were implemented in MATLAB. After reading the netlist, the transistors in any circuit are replaced by the proposed Xmodel and then the MNA equations are constructed by parsing the netlist. The equations are solved by means of our waveform evaluation algorithm explained in section III. For the comparison purpose, BSIM4 analytical drain current model is also implemented in Matlab. Generating 23 points to approximate I_{ds} curve using BSIM4 I_{ds} model needs $1s$, approximately 40 times slower than using Xmodel. In the simulations, we selected $100ps$ input slew and $2.5ns$ time period.

The upper figure in Fig. 6 shows the voltage waveform at the output of a NAND2_X1 standard cell for a timing arc from the middle transistor on the stack. The middle and bottom figures in Fig. 6 show the waveform evaluation accuracy using Xmodel for XOR2_X1 and AOI211_X1 cells respectively. It is worth noticing that even the internal node voltage waveforms can be accurately evaluated in our algorithm.

Fig. 7 shows the accuracy of Xmodel when used in a multi-input simultaneous switching scenario. The simulation consists of NAND2_X1 standard cell where both inputs are rising at the same time. Fig. 8 shows the waveform evaluation and comparison of a NAND4_X1 standard cell with 4 inputs, indicating the accuracy of Xmodel for high-stack cells.

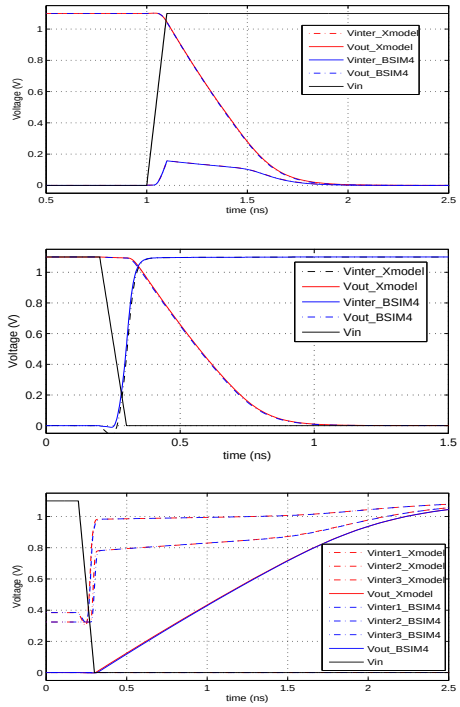


Fig. 6. Upper: NAND2_X1; Middle: XOR2_X1; Bottom: AOI211_X1

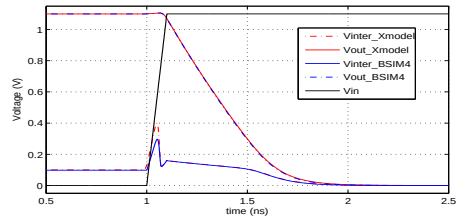


Fig. 7. Simultaneous multi-input switching

In Table I, we compare the delay and output slew evaluation using our Xmodel and transistor-level Spectre simulation using BSIM4 model for several standard cells from the Nangate 45nm library. Using the table-based Xmodel demonstrates high accuracy for standard cells. In the simulations, the output load is $20fF$ for all the cells except INV which uses $10fF$. The

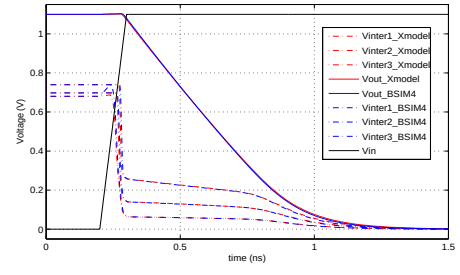


Fig. 8. Waveform evaluation of the NAND4_X1 cell

relative errors of falling delay and falling output slew with respect to Spectre are similar to the rising delay and slew. Our analysis shows that we are within 1% of Spectre for both delay and slew calculation. The rising and falling delay and output slew errors for simultaneous multi-input switching of multi-input standard cells in the library are also within 1%, indicating excellent ability to deal with multi-input gates with high stack effects.

TABLE I
DELAY AND OUTPUT SLEW EVALUATION (MX - XMODEL; MB - BSIM4)

Stand. cells	rising delay (ns)			rising output slew (ns)		
	MX	MB	| error| ($\%$)	MX	MB	| error | ($\%$)
INV	0.2777	0.2766	0.40	0.3831	0.3851	0.53
BUF	0.5246	0.5229	0.32	0.7459	0.7442	0.23
NAND2	0.5239	0.5220	0.36	0.7517	0.7482	0.47
NOR2	0.8385	0.8338	0.56	1.1420	1.1385	0.31
AND2	0.5324	0.5329	0.09	0.7481	0.7443	0.51
XOR2	0.8620	0.8664	0.51	1.1566	1.1566	0.00
AOI211	0.9494	0.9555	0.64	1.1959	1.1854	0.89
MUX2	0.5338	0.5334	0.07	0.7502	0.7445	0.77
NAND4	0.5528	0.5564	0.64	0.7787	0.7773	0.18

We also evaluated the statistical extension of Xmodel (SX-model) using the same library for all the standard cells. Xmodel-based cell models enable the propagation of our waveform model mentioned in section III-A, without having to abstract them into delay/slew pairs like GLMs. Monte-Carlo method is applied to evaluate the statistical delay using the SXmodel. The sensitivity tables of model elements to process parameters of interest have been characterized. Considering the effective channel length (L) has significant effect on the transistor behavior, we assume the statistical variable L has: $\mu = 50nm$ and $3\sigma = 18\% \times \mu$. The mean ($\mu$) and standard deviation (σ) error of delay for the standard cells of Table I are are within 2% and 10%, respectively. The main sources of the error are the sensitivity characterization and the first-order Taylor expansion for SXmodel introduced in section II-C. Better accuracy can be achieved by region-wise sensitivity characterization and higher-order statistical model, however, at the cost of increased complexity and slower calculation.

V. CONCLUSION

In this paper, instead of optimizing gate-level models at the expense of complexity, we propose an accurate transistor model for gate-level cell modeling. Based on the transistor-level representation, the gate models are independent of input waveform and output load, faster to be characterized and able to deal with multi-input high-stack cells. The overall simulation methodology is based on Broyden's nonlinear solver that delivers high efficiency for analysis of logic cells and avoids the continuity and smooth derivative requirements for the LUT-based Xmodel. Compatible with Broyden's method, the Xmodel uses inexpensive piecewise linear interpolation for the elements in Xmodel. The sizes and dimensions of tables are considered and optimized for current source and intrinsic capacitances differently to maintain high accuracy and efficiency. We also showed the capabilities of the statistical extension of the Xmodel. The experimental results showed high accuracy and efficiency of the proposed SXmodel and waveform evaluation algorithm compared with the transistor-level Spectre simulation using BSIM4 model in different standard cells and arcs for Nangate 45nm technology.

REFERENCES

[1] Synopsys. Ccs timing white paper. [Online]. Available: www.synopsys.com/products/solutions/galaxy/ccs/cc_source

[2] Cadence. Effective current source model (ecsm). [Online]. Available: www.cadence.com/datasheets/ecsm_ds.pdf

[3] C. Amina, C. Kashyap, N. Menezes, K. Killpack, and E. Chiprout, "A multi-port current source model for multiple-input switching effects in cmos library cells," in *DAC*, Jun. 2006, pp. 247–252.

[4] A. Goel and S. Vrudhula, "Statistical waveform and current source based standard cell models for accurate timing analysis," in *DAC*, California, USA, Jun. 2008, pp. 227–230.

[5] C. Kashyap, C. Amin, N. Menezes, and E. Chiprout, "A nonlinear cell macromodel for digital applications," in *ICCAD*, Nov. 2007, pp. 678–685.

[6] S. Raja, Varadi, M. Becer, and J. Geada, "Transistor level gate modeling for accurate and fast timing, noise, and power analysis," in *DAC*, Jun. 2008, pp. 456–461.

[7] T. Shima, T. Sugawara, S. Moriyama, and H. Yamada, "Three-dimensional table look-up mosfet model for precise circuit simulation," *IEEE Journal of Solid-State Circuits*, vol. SC-17, no. 3, pp. 449–454, Jun. 1982.

[8] T. Shima, H. Yamada, and R. L. M. Dang, "Table look-up mosfet modeling system using a 2-d device simulator and monotonic piecewise cubic interpolation," *IEEE Trans. on Computer-Aided Design*, vol. CAD-2, no. 2, pp. 121–126, Apr. 1983.

[9] P. E. Allen and K. S. Yoon, "A table look-up model for analog applications," in *ICCAD*, Nov. 1988, pp. 124–127.

[10] S. N. Agarwal, A. Jha, D. V. Kumar, J. Vasi, M. B. Patil, and C. Rustagi, "Look-up table approach for rf circuit simulation using a novel mearsurement technique," *IEEE Trans. on Electron Devices*, vol. 52, no. 5, pp. 973–979, May 2005.

[11] D. Nadezhin, S. Gavrilov, A. Glebov, Y. Egorov, and V. Zolotov, "Soi transistor model for fast transient simulation," in *ICCAD*, Nov. 2003, pp. 120–127.

[12] E. Acar, F. Dartu, and L. Pileggi, "Teta: transistor-level waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design*, vol. 21, pp. 605–616, May 2002.

[13] Pathmill: Transistor-level static timing analysis. [Online]. Available: http://www.synopysys.com/products/analysis/pathmill_ds.pdf

[14] E. Acar, "Linear-centric simulation approach for timing analysis," Ph.D. dissertation, Carnegie Mellon University, Dec. 2001.

[15] Q. Tang, A. Zjajo, M. Berkelaar, and N. van der Meijs, "A simplified transistor model for cmos timing analysis," in *ProRisc*, 2009, pp. 289–294.

[16] J. F. Epperson, *An Introduction to Numerical Methods and Analysis*. John Wiley & Sons, Inc, 2002.

[17] M. Chen, W. Zhao, F. Liu, and Y. Cao, "Fast statistical circuit analysis with finite-point based transistor model," in *DATE*, Apr. 2007, pp. 1–6.

[18] A. Brambilla, A. premoli, and G. S. Gajani, "Recasting modified nodal analysis to improve reliability in numerical circuit simulation," *IEEE Tran. on Circuits ans Systems*, vol. 52, no. 3, pp. 522–534, Mar. 2005.

[19] R. A. Saleh and A. R. Newton, *Mixed-Mode Simulation*. New York: Kluwer, 1990.

[20] W. J. McCalla, *Fundamentals of Computer-Aided Circuit Simulation*. New York: Kluwer, 1988.

[21] Nangate 45nm open cell library. [Online]. Available: http://www.nangate.com/index.php?option=com_content&task=view&id=137&Itemid=137