AN APPROACH FOR SPECIFYING THE ADC AND AGC REQUIREMENTS FOR UWB DIGITAL RECEIVERS

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Abstract

Digital pulsed ultra wideband (UWB) receivers offer numerous advantages compared to architectures based on analogue correlation, but present unique implementation challenges. The specification of the Analogue-to-Digital Converter (ADC) resolution constitutes one of the most critical activities in the design of digital UWB receivers. Moreover, multi-bit ADCs must be associated with an Automatic Gain Control block which avoids the sub-optimal regimes of the ADC dominated by quantisation or saturation noise. This paper shows how to determine the ADC resolution requirements and the optimal Automatic Gain Control (AGC) settings for the general class of digital receivers. We conclude that 3 bits provide sufficient resolution on condition that the AGC scales the input signal at a reference root mean squared (RMS) level of half the ADC saturation voltage.

1 Introduction

The design of UWB receivers presents unique challenges. The most popular receiver is based on matched filtering (correlation) with the transmitted pulse followed by a RAKE structure capturing the multipath diversity of the channel. However, the pulse distortion introduced by the transceiver antennas and the channel can vary among the multipaths. As a result, the RAKE receiver can not achieve the optimal performance. Moreover, sampling at twice the chip rate leads to unaffordable sampling rates for high bit rate applications. This issue is even exacerbated in fractionally spaced receivers. Transmitted reference (TR) systems [5] sample the received signal at the pulse repetition rate and avoid the need for local template generation, but require extremely wideband delay lines in the analogue domain which are particularly difficult to realise.

On the other hand, digital based receivers provide more flexibility and benefit from CMOS technology scaling, but require ADCs sampling at Nyquist rate which are hardly realisable and highly power consuming. Flash ADCs constitute the standard solution for the sample rates and resolution required for digital UWB architectures (Figure 1). As the ADC power consumption of Flash ADCs scales linearly with the sampling rate and as a factor close to 4 with the bit width [16, 8], the UWB system architect can choose

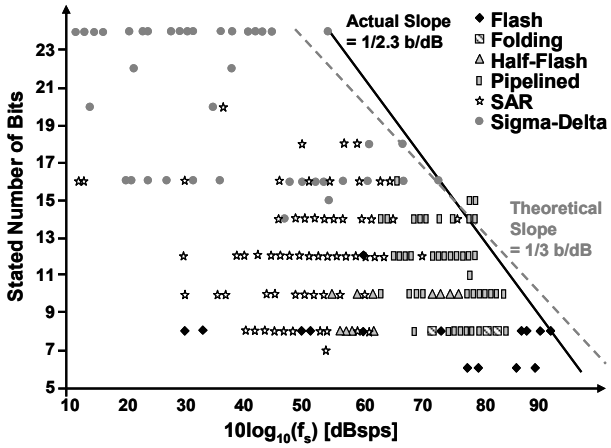

Figure 1: ADC achievable sampling rates vs. resolution [3].

either a high (Nyquist) sample rate or multi-bit resolution but not both. Several high speed 1-bit receiver architectures have been proposed, for example in [13,6]. However, 1-bit receivers suffer from poor robustness against interferers, which must be improved using notch filters in the RF front-end or by shaping appropriately the transmitted pulse. The first solution comes at the cost of flexibility, whereas the second requires the transmitter to know the interference at the receiver via a feedback loop, for example.

Parallel multi-bit ADC architectures based on signal channelisation in time [6,1] or frequency domain [3,9] reach an aggregate sampling rate equivalent to Nyquist's criterion and support interference cancellation in the digital domain. However, this advantage comes at the cost of increased area and power consumption, as each ADC typically consumes about 100 mW using state-of-the-art Flash ADCs, see e.g. [14,12]. The sampling rate speed is relaxed in [7] by using a bank of discrete-frequency matched filters followed by parallel ADCs. Nevertheless, all these solutions require careful control of the circuit mismatches between the parallel branches.

Subsampling techniques provide an attractive alternative [15,2]. As an example, a receiver based on such techniques has been proposed in [15] and can offer data rates in the order of magnitude of 100 Mb/s at sampling rates below 500 MHz.

Few results have been published about the bit width requirements of digital receivers for pulsed UWB [10,2].

However, no unified framework has been proposed yet which takes into account the combined optimisation of the ADC and the AGC parameters, using realistic pulses in the 3.1–10.6 GHz band and in multipath environment. Using the methodology presented in this paper, we show that 3 bits provide sufficient resolution if the AGC scales the input signal at a reference root mean squared (RMS) level of half the ADC saturation voltage.

2 Methodology

The nonlinear nature of the ADC makes a deterministic analysis of the effect of quantisation on the performance problematic. A statistical approach is traditionally taken, where the quantisation error is modelled as an additive uniform random noise with zero mean and power $\sigma^2_n = q^2/12$ for rounding ADCs, where $q = R/2^b$ is the quantisation step. $R = 2V_{sat}$ is the input range of the ADC, which clips the input signal below $-V_{sat}$ and above V_{sat}. This noise modelling is appropriate if the quantisation step q is small compared to the range R, but becomes less accurate as the bit resolution decreases. As UWB signals are immersed in additive white Gaussian noise (AWGN), the required ADC resolution is moderate (< 5 bits) compared to classical narrowband systems. Moreover, the multipath UWB channel modifies the distribution of the samples over the ADC range, compared to an ideal single path channel. The channel response must be therefore taken into account in the bit width decision process. As a result, we will determine the ADC precision requirements by simulation.

Contrary to narrowband fixed-point analysis, we cannot assume quantisation to be the dominant source of noise. For narrowband systems, the minimum SNR required at the detection device in order to reach a desired bit error rate (BER) is identified, and the number of bits is then determined so that the SNR remains above this minimum value. This approach is not suitable for UWB systems, since the AWGN and interference noise are the dominant sources of noise at the output of the ADC. Instead, we will observe the SNR degradation introduced by the quantisation and decide the number of bits so that the decrease in SNR remains limited.

Contrary to high speed 1-bit ADCs, narrowband interference is not a critical problem with multi-bit ADCs. In particular, the subsampling receiver presented in [15] can remove the interference in the digital domain or avoid it by choosing a band free from interferers. We will therefore leave the issue of interference out of the scope of this paper.

3 UWB Signal Model

The received signal is modelled as a stream of PPM and/or PAM pulses affected by AWGN $n(t)$:

$$s_{rx}(t) = \sum_{n=-\infty}^{+\infty} \sum_{l=1}^{L} \alpha_l \, c_n \, p(t - n\,T_f - t_n - \tau_l) + n(t) \quad (1)$$

where $c_n \in \{0, \pm\Gamma, \pm 3\Gamma, \ldots\}$ and $t_n \in \{0, \Delta, 2\Delta, \ldots\}$ correspond to the pulse modulation. We use the standard IEEE channel models CM1 – CM4 [4] as the channel model

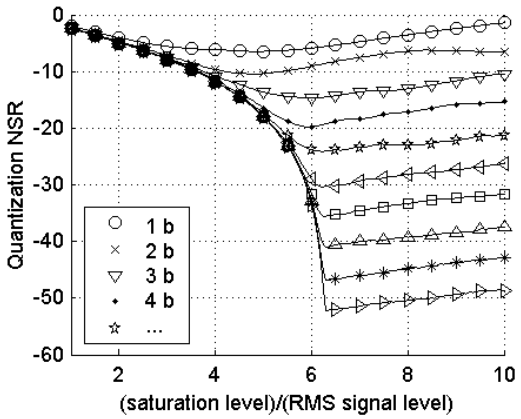

Figure 2: Quantisation noise to signal ratio vs. V_{sat}/RMS_{in} , no channel.

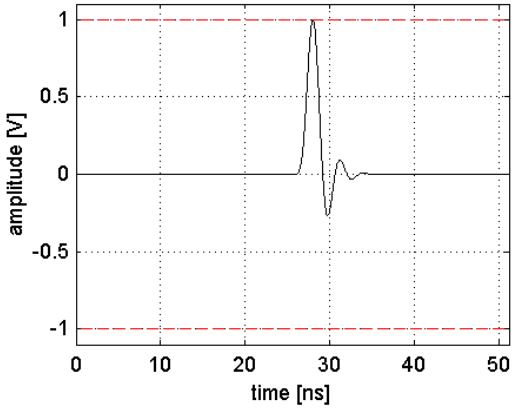

Figure 3: AGC scaling the ADC input to V_{sat}, no channel.

$$h(t) = \sum_{l=1}^{L} \alpha_l \, \delta(t - \tau_l) \quad (2)$$

where we have grouped the multipaths from different clusters in a single summation. We do not include in (1) the time hopping or direct sequence spreading code for the sake of simplicity, without restricting the scope of the results presented in this paper.

4 ADC Requirements and AGC Settings

For a given number of bits, the ratio of the saturation level V_{sat} to the signal standard deviation at the input of the ADC RMS_{in} must fall within a certain range in order to minimise the quantisation noise. If V_{sat}/RMS_{in} tends to zero, the probability of ADC saturation/clipping is high and the saturation noise power quickly increases. If the ratio is too large, the quantisation noise to signal ratio increases as the RMS signal level decreases. This behaviour is illustrated for different bit widths in figure 2. The role of the AGC is to set the signal RMS level to an optimal attack point of the ADC

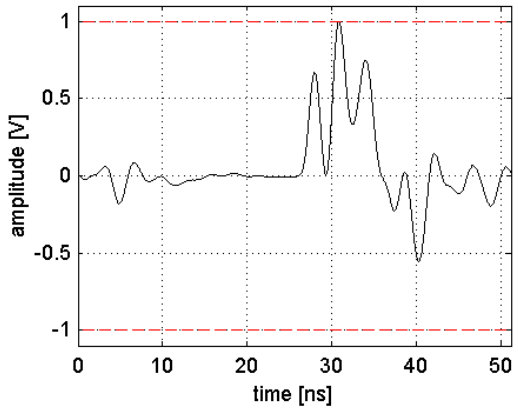

Figure 4: AGC scaling the ADC input to V_{sat}, channel model CM1 (realisation 1).

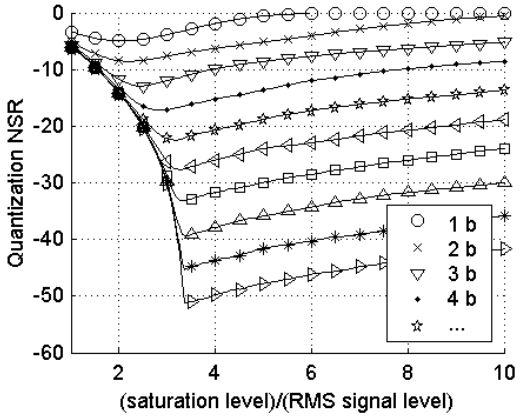

Figure 5: Quantisation noise to signal ratio vs. $V_{sat}/\ RMS_{in}$, channel model CM 1 (realisation 1).

RMS_{ref} , which results from the trade-off between minimising quantisation noise and avoiding the region of operation dominated by saturation noise, on the left of fig. 2.

The effect of the transmission channel must be taken into account in this trade-off analysis, or a conservative choice will result. As an example, figure 3 shows a typical received pulse in absence of noise. The AGC scales this pulse to the input of the ADC such that any clipping is avoided, by fitting the received signal to the whole range $[-V_{sat}, V_{sat}]$, where we assume V_{sat} = 1V. Figure 4 shows the effect of a typical UWB channel model. The received signal is not only spread in time but also along the vertical axis: the samples are more uniformly spread over the input range of the ADC. As a result, the crest factor of the received signal V_{peak}/RMS_{in} decreases and affects the optimal attack point of the ADC, as it is visible from figure 5.

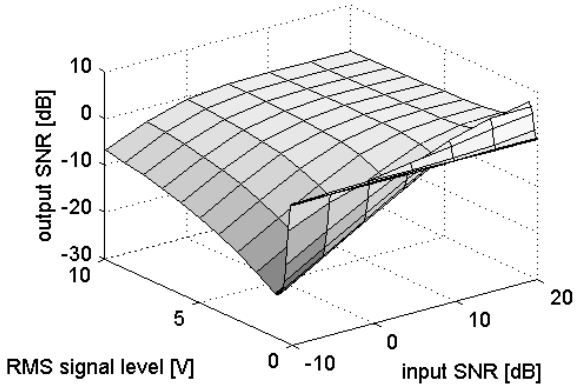

Figure 6: SNR at the ADC output vs. SNR at the ADC input and RMS signal level, 1-bit ADC, channel model CM1 (realisation 1).

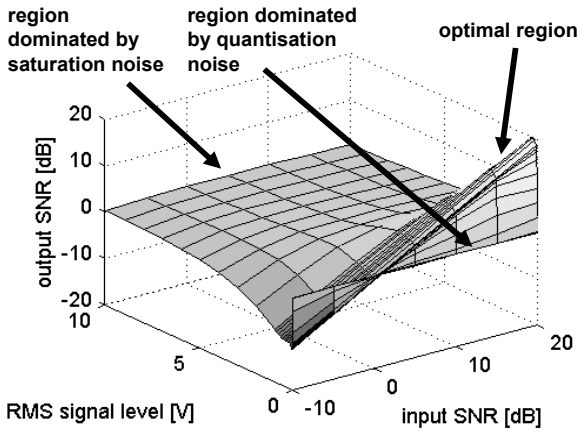

Figure 7: SNR at the ADC output vs. SNR at the ADC input and RMS signal level, 4-bit ADC, channel model CM1 (realisation 1).

Another aspect to take into account is the AWGN level. Quantisation noise may be dominant in narrowband systems if the SNR at the ADC input is high enough. This situation is much less likely to occur in UWB systems. As a result, the required number of bits is determined so that the SNR degradation due to quantisation is limited, e.g. less than 0.1 dB, over the range of SNR values which allow for reliable reception. In this paper, we do not include the spreading gain for the sake of generality and consider an SNR range from −10 to 20 dB. The optimal ADC attack point corresponds to the AGC gain which minimises the SNR degradation.

Figures 6−7 illustrate the relationship between the SNR at the output (SNR_{out}) and at the input (SNR_{in}) of the ADC, for different signal RMS levels (i.e. different AGC gains). Three regions can be identified:

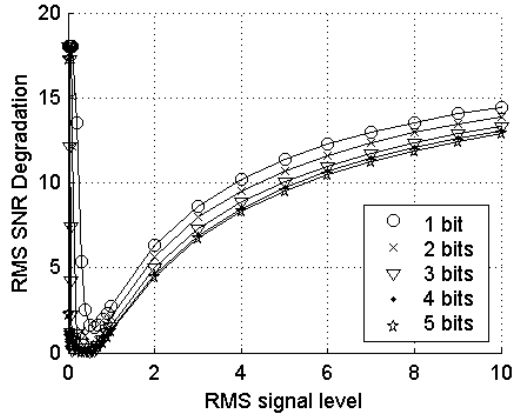

Figure 8: Root mean squared degradation of the overall SNR due to quantisation, as a function of the input RMS level, channel model CM1 (realisation 1).

ADC Resolution	$RMS_{in,opt}$ *CM1*	*CM2*	*CM3*	*CM4*
1 bit	0.591	0.592	0.597	0.598
2 bits	0.572	0.573	0.571	0.571
3 bits	0.533	0.536	0.535	0.536
4 bits	0.483	0.486	0.487	0.489
5 bits	0.429	0.438	0.441	0.444

Table 1: Optimum RMS value at the ADC input.

ADC Resolution	$RMSE_{opt}$ *CM1*	*CM2*	*CM3*	*CM4*
1 bit	1.496	1.479	1.507	1.502
2 bits	0.313	0.266	0.249	0.237
3 bits	0.074	0.064	0.062	0.063
4 bits	0.010	0.013	0.014	0.017
5 bits	0.006	0.004	0.004	0.005

Table 2: Root mean squared SNR degradation due to quantisation, at the optimum input RMS level of table 1.

- At high RMS levels (above 1 V), the output SNR at the output of the ADC converges to zero due to the saturation noise.
- At low RMS levels (below 0.2V approximately), the output SNR converges also to zero, due to the high quantisation step with respect to the RMS level.
- At intermediate RMS levels (between 0.2V and 1V), a linear relationship exists between the SNR at the input and at the output of the ADC, which indicates that the degradation introduced by quantisation is bounded. The degradation is minimal for the optimal value $RMS_{in,opt}$ which minimises the difference between the optimal linear relationship between the SNR at the input and the output of the ADC

$$SNR_{out} = SNR_{in} \tag{3}$$

and the actual relationship characterised by the specific function f_{ADC} plotted in figures 6−7

$$SNR_{out} = f_{ADC}(RMS_{in}, SNR_{in}) \tag{4}$$

We choose to minimise the Root Mean Squared Error for a given bit width b, i.e.

$$RMSE(b) = \left[\int \left[SNR_{in} - f_{ADC}(b, RMS_{in}, SNR_{in})\right]^2 \mathrm{d}SNR_{in} \right]^{1/2} \tag{5}$$

Figure 8 illustrates the RMSE for different bit widths and RMS_{in} values. Table 1 shows the average optimal values $RMS_{in,opt}$ which minimise (5) for 100 different realisations of the IEEE channel models [14]

$$RMS_{in,opt}(b) = \arg\min_{RMS_{in}} \left[RMSE(b)\right] \tag{6}$$

For a given resolution, the optimal $RMS_{in,opt}$ is approximately the same for different channel models and channel realisations. It decreases with increasing resolution, since smaller quantisation steps allow decreasing the RMS level, preserving the accuracy for small values while decreasing the clipping ratio. Smaller bit widths present a higher risk of falling into the situation where the quantisation noise or the saturation noise degrades the output SNR performance. As a result, more severe constraints are set on the precision of the gain and the measured signal power. As shown in table 2, the root mean squared SNR degradation due to quantisation is negligible for $b \geq 3$ at the optimal RMS_{in} values corresponding to table 1.

5 Conclusions

Flash ADC architectures constitute the basic choice for the sample rates and resolution required for digital UWB architectures, but they normally achieve poor linearity for high resolution. As we have shown in this paper that the bit width requirement is moderate, this issue is not critical for digital UWB receivers. Instead, power consumption is the major concern. It is therefore of uttermost importance to minimise the bit width and scale the received signal with respect to the ADC dynamic range, using techniques appropriate to the UWB peculiarities, such as we have presented in this paper. We have shown that a 3-bit ADC is a suitable choice provided that the AGC scales the input signal at a reference RMS level of half the ADC saturation voltage.

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