17.5 An Intrinsically Linear Wideband Digital Polar PA Featuring AM-AM and AM-PM Corrections Through Nonlinear Sizing, Overdrive-Voltage Control, and Multiphase RF Clocking

Mohsen Hashemi[1], Yiyu Shen[1], Mohammadreza Mehrpoo[1], Mustafa Acar[2], René van Leuken[1], Morteza S. Alavi[1], Leonardus de Vreede[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Ampleon, Nijmegen, The Netherlands

To fully benefit from the progress of CMOS technologies, it is desirable to completely digitize the TX, replacing its final stage with a digitally controlled PA (DPA). The DPA consists of arrays of small sub-PAs that are digitally controlled to modulate the output amplitude, thus operating as an RF-DAC [1-6]. DPAs are normally designed in a switched mode (Classes E/D/D^{-1}, etc.) to achieve high efficiency while using high sampling rate to attenuate and push the spectral images to higher frequencies. However, they suffer from high nonlinearity in their AM-code-word (ACW) to AM and ACW-to-PM conversion. To correct for such nonlinearities, digital pre-distortion (DPD) of the input signal is often used [1-3], typically implemented by look-up tables (LUT). Unfortunately, DPD approaches suffer from large signal-BW expansion due to their inherently nonlinear characteristics. This, combined with the already present BW regrowth in a polar TX in the AM and PM paths, yields significant hardware-speed/power constraints when the signal BW becomes large. For a Cartesian TX, the use of LUT-DPD is even more complicated since a full 2D LUT is typically required [2]. To relax the overall system complexity, it is highly desirable to have a PA with a maximum inherent linearity without compromising its power or efficiency. In this work, an ACW-AM correction based on nonlinear sizing along with controlling the peak voltage of RF clocks (overdrive voltage tuning) and a ACW-PM correction based on multiphase RF clocking are introduced to linearize the characteristic curves of a Class-E polar DPA with intent to avoid any kind of pre-distortion.

Figure 17.5.1 depicts this concept featuring 9b amplitude modulation. The DPA consists of 8 differential sub-PA segments. These segments are nonlinearly sized to linearize the ACW-AM. The PVT/load impedance variations are compensated by digitally tuning the supply voltage of PA buffers with an on-chip programmable LDO. The input PM RF clock is amplified and fed to the multiphase RF-clocking circuit, which generates 5 differential RF clocks with different phase offsets. The output clocks are applied simultaneously to different sub-PA segments to flatten the ACW-PM curve. Explicit capacitive tuning between the DPA differential outputs is used to enhance the efficiency at full power against clock skewing and duty-cycle variation. A passive mesh structure equalizes the delays for all RF clock lines from the multiphase RF-clocking circuit to the DPA. P_{OUT}-aware clock gating is used to reduce driver power in back-off. Coarse time alignment between the amplitude and phase information is performed in the digital domain; fine adjustments are handled by a 4b delay line in the path of the ACW sampling clock.

Figure 17.5.2 shows the ACW-AM linearization concept (top) and its simplified circuit implementation (bottom). In a Class-E (or D^{-1}) DPA, which uses transistor on-resistance (R_{ON}) for AM control [1], the ACW-AM curve is a strongly nonlinear function of R_{ON}-to-R_{Load} ratio. Conventionally, the total size of the switched-on devices is a linear function of ACW [1-6]. By nonlinearly sizing the sub-PA segments based on the inverse of the ACW-AM curve, the overall ACW-AM curve of the DPA is piecewise linearized (Fig. 17.5.2 top). Since the transistor R_{ON} is a function of the overdrive voltage (V_{OD}) too, it is used for compensating the PVT/load variations with insignificant impact on the peak drain efficiency (DE) and P_{SAT}. A 6b programmable on-chip LDO controls the V_{OD} for the whole DPA by controlling the V_{DD} of RF-clock buffers. It has a resolution of 9 to ~10mV with an output range of 0.6 to 1.2V. Once programmed for optimum linearity, it is fixed during the normal DPA operation.

Figure 17.5.3 shows the ACW-PM correction based on multiphase RF clocking. It consists of a bank of 5 static phase shifters implemented by programmable delay lines. For a nonlinearly sized Class-E DPA with the conventional single-phase RF clocking, the output phase decreases with increasing ACW (Fig. 17.5.3 top). In time domain, this translates to an increment in the delay at the output. In order to reduce the phase error, the RF clocks of smaller sub-PA segments are applied with larger fixed delays (larger phase offsets) and the larger segments are fed with smaller fixed delays (smaller phase offsets). In this technique, in contrast to a conventional DPA with a DPD approach, no dynamic phase correction is needed for each ACW code. For example, at 6dB back-off power, the sub-PA segments 1-2, 3-4 are fed simultaneously with phase offsets $\Delta\phi_1 > \Delta\phi_2$, respectively, while other segments are turned off and at full power, the sub-PA segments 1-2, 3-4, 5-6, 7, 8 are fed simultaneously with phase offsets $\Delta\phi_1 > \Delta\phi_2 > \Delta\phi_3 > \Delta\phi_4 > \Delta\phi_5$, respectively. The output currents of these individual sub-PA segments are summed, and the overall output phase is inherently averaged, allowing a controllable and considerable reduction of phase error in the ACW-PM curve. The phase-offset of each clock is digitally controllable over a range of 80° with a resolution of 5°, which is more than enough to cover errors caused by PVT/load changes.

The circuit is prototyped in 40nm bulk CMOS. The core area is 1mm×0.45mm (Fig. 17.5.7). The raw ACW is applied to the DPA using an on-chip 4K SRAM running at 625MHz. The input RF signal is phase modulated off-chip. All measurements are done without applying any kind of DPD. Measured ACW-AM and ACW-PM for a digital input ramp are shown in Fig. 17.5.4(top). The effectiveness of PVT/load compensation for ACW-AM is measured and plotted for different control-bit settings. The ACW-PM curves before averaging (for one ramp period) and after averaging (over 256 ramp periods) are shown. The two-tone measurements (Fig. 17.5.4 bottom) with a 1.2MHz bandwidth show an IM3 and IM5 of -60dBc and -50dBc, respectively, at 2 to 2.1 GHz. Peak P_{OUT}, DE and PAE are measured and plotted vs. frequency for different PA V_{DD} (Fig. 17.5.4 bottom). It can be seen that by increasing the drain voltage, the peak P_{OUT} and PAE increase, while the peak DE does not change significantly. However, for reliability concerns, the drain voltage is kept less than 0.6V during the normal operation. With a V_{DD}=0.6V, the peak P_{OUT}, DE and PAE are 16.1dBm, 43.7% and 32%, respectively.

Figure 17.5.5 shows the dynamic performance for QAM modulated signals measured at f_c=2GHz. ACPR1 is as low as -49 to -40dBc for modulation bandwidths of 1.2 to 40MHz. The measured EVM is -33dB for 16-QAM and -31dB for 64-QAM signals with a 40MHz BW.

Figure 17.5.6 summarizes and compares this work with the state of the art. The nonlinear sizing with V_{OD} tuning and multiphase RF clocking provide a very high DPD-less RF-DAC linearity (EVM/ACPR) for wideband signals (>=20MHz) without sacrificing output power or efficiency. In fact, its linearity competes with state-of-the-art DPD-less Cartesian DPA [4] while the output power and efficiency performance are superior by 5 to ~6dB and 10 to 12%, respectively.

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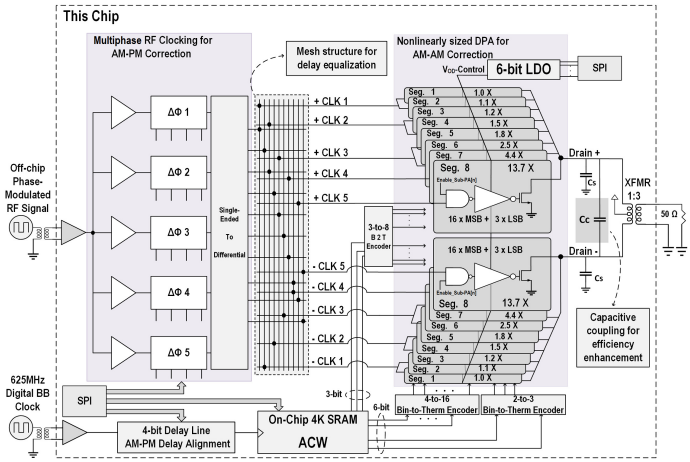


Figure 17.5.1: Overall block diagram of the linear DPA.

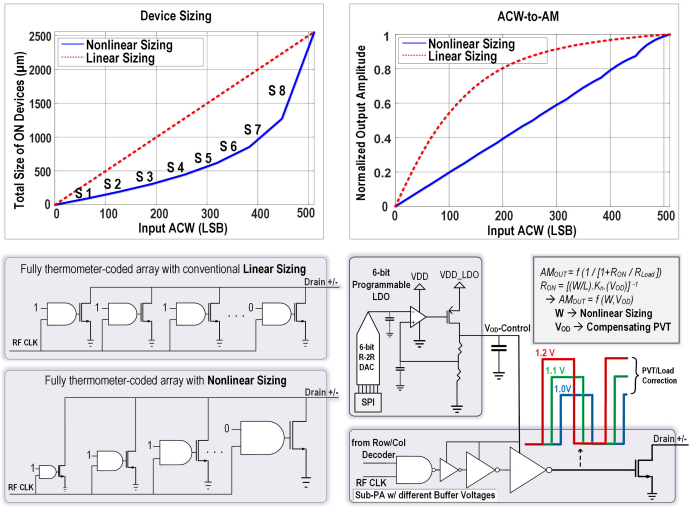


Figure 17.5.2: ACW-AM linearization concept and circuit.

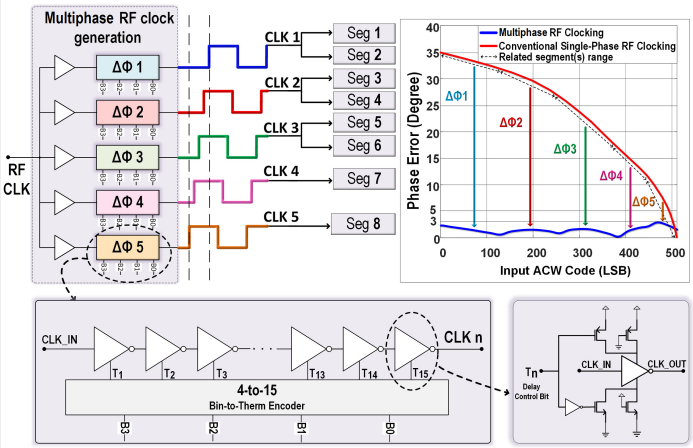


Figure 17.5.3: ACW-PM linearization concept and circuit.

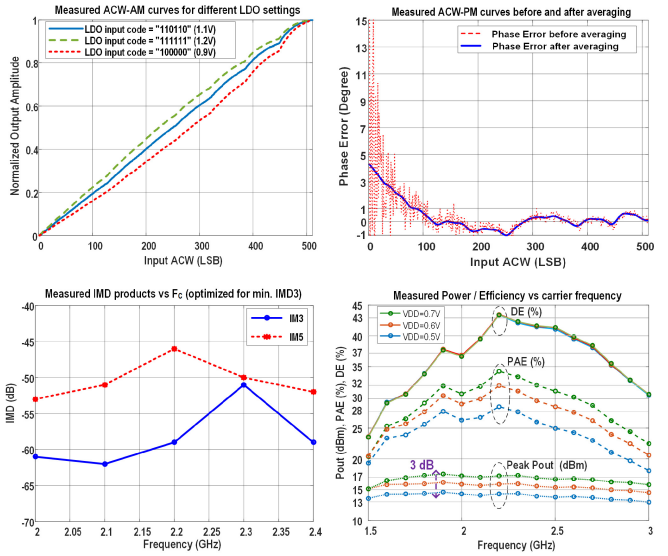
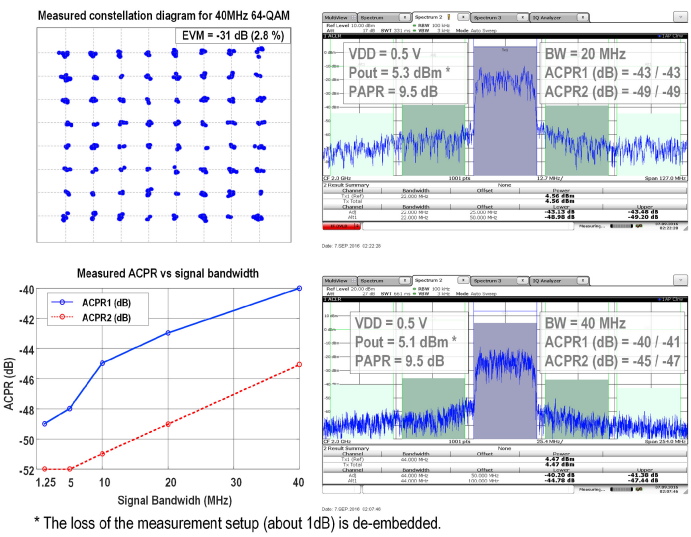


Figure 17.5.4: Measured ACW-AM/PM and Pout/DE/ IMD vs f_c.



* The loss of the measurement setup (about 1dB) is de-embedded.

Figure 17.5.5: Measured 40MHz 64-QAM EVM and ACPR vs BW.

	[1] JSSC'11	[2] JSSC'16	[3] JSSC'16	[4] ISSCC'15	[5] JSSC'15	[6] ISSCC'16	This Work		
Architecture	Polar DPA	IQ SC-DPA	Polar DPA	Cartesian QDAC	Polar DPA	Polar SC-DPA	Polar DPA		
Bandwidth (MHz)	20	10	8	20	20	2	10	20	40
ACPR1 / ACPR2 (dBc)	-40 [a] / NA (Emission @20MHz)	-30.7 / -38.5	-27.9 / NA	-42 / -47[b] (Adj. Ch. 5 MHz)	-28 [a] / NA (Emission @20MHz)	-42 [a] / NA (Emission @2MHz)	-45 / -51 @ Fc=2GHz	-43 / -49	-40 / -45
EVM (dB)	-28 (OFDM)	-28 (64-QAM)	-36.3 (256-QAM)	NA	28 (64-QAM)	-27.1 (64-QAM)	-33 (40MHz 16-QAM) -31 (40MHz 64-QAM)		
(Digital) Pre-Distortion	YES	YES	YES	NO	NO	NO	NO		
Fc (GHz)	2.25	2	2.6	1	2.1	0.93	2.2		
Supply (V)	1	1.2/2.4	1	0.9 / 1.8	2.1	1	0.5 [c]		
Peak P_{OUT} (dBm)	22	20.5	28.1	8 [a]	24	8	14.6		
Peak DE (%)	44	NA	40.7	27.4 [a]	35	NA	43.8		
Peak PAE (%)	38	20	35	15.3 [a]	NA	45	28.8 [d]		
Average P_{OUT} (dBm)	14	14.5	20.4	1	13.8	0	6.1 [e]		
Average DE (%)	18	NA	16.3	5.5 [a]	14.5 [a]	26.3 [a]	17.5 [e]		
Average PAE (%)	16.8 [a]	12.2	NA	3 [a]	NA	NA	14.3 [d, e]		
Output Matching Network or Balun	On-chip	On-chip	On-chip	Off-chip	On-chip	Off-chip	On-chip		
Technology (nm)	65	65	65	28	65	40	40		
Area (mm^2)	1.7 [a] (w/ on-chip balun)	1 [a] (w/ on-chip inductor)	0.96 (w/ on-chip balun)	0.25	1.2 [a] (w/ on-chip balun excluding ADPLL)	0.18 [a] (Excluding ADPLL)	0.45 (w/ on-chip balun)		

(a) Calculated or Estimated from the paper Figures or Tables

(b) Measured with 20MHz TX channel but 5MHz Adj. channels at 12.5MHz/17.5MHz offset

(c) The RF clock buffers VDD is supplied by the on-chip LDO which has a 1.2V DC supply.

(d) PAE includes the power consumption of all the drivers and encoders (34mW at peak power, 5mW at average power) but not the power consumption of the multiphase RF clock generation circuit (7mW).

(e) For a 10MHz QAM signal with PAPR = 8~9 dB.

Figure 17.5.6: Performance summary and comparison table.

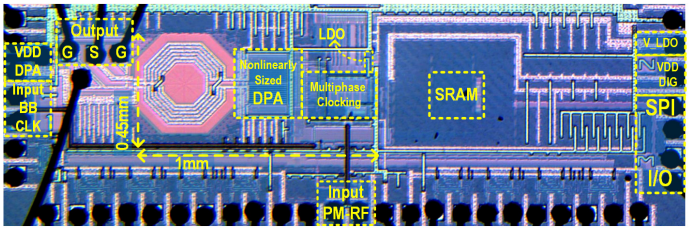


Figure 17.5.7: Die micrograph.

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