A CMOS 0.23pJ Freeze Vernier Time-to-Digital Converter

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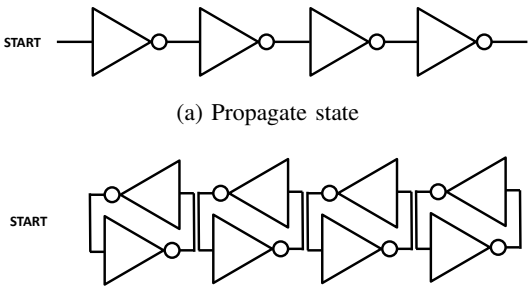
***Abstract*—A novel Time-to-Digital Converter architecture for high resolution and low power is proposed. The Freeze Vernier Delay Line is a Vernier-type TDC, where the state of the slow delay line can be frozen by the fast delay line, omitting the power-hungry time capture elements like D-registers or arbiters that are usually employed in a Vernier TDC. The two main issues of the design, the charge kickback between the delay lines and the imperfect freezing are solved with extra circuitry. The overall TDC consists of inverters and transmission gates only. A proof-of-concept design has been simulated in 90nm CMOS with a typical resolution of 10.05 ps, a dynamic energy consumption of 0.232 pJ per conversion and an area of 10.503 μm^2.**

I. Introduction

With the ever-increasing integration of functionalities onto silicon chips, the so called time-to-digital converters (TDCs) [1] have been introduced which can be made with standard CMOS processes. These are stopwatches with picosecond resolution [2] that can measure the time difference between two signal edges. The downscaling of CMOS technology has brought more and more different architectures in the state-of-the-art [3].

The original counter-based solutions had proven to be limited by the clock period [4], so sub-clock period resolution TDCs were proposed. Taking the analogy from analog-to-digital converters, the flash-type TDCs [5] are based on delay line(s) with identical delay stages like buffers or inverters. The single delay line architecture utilizes a single chain of delay line where the start signal propagates. The sequence of nodes is sampled on the edge of the stop signal. This a widely-used architecture, however, the resolution here is still limited by the delay of the individual stages. There are several different architectures for sub-gate delay resolution not explored here like time residue amplification [6], passive interpolation [7], etc. The solution analyzed is about implementing two delay lines in parallel, which is the so-called Vernier delay line [8]. Here the timing resolution is dependent on the delay difference of the delay elements of the two lines, thus it can in theory, take an arbitrarily small value. This is not possible because of the time capture elements, process spread and drive/load mismatch [9]. The output is captured with D-registers or arbiters.

An attempt to omit the power-hungry time capture circuitry is the Vernier Gated Ring Oscillator [10], where the delay stages are frozen by and external enable/disable signal. Wherever the signal was frozen in transition, the analog voltage value is preserved long enough to be read out by a counter. Thus the time capture elements are omitted and the design consumes considerably less power. Also, the charge kickback from the time capture elements is no longer present.



(a) Propagate state

(b) Hold state

Fig. 1: Functional Description of the Freeze Vernier Delay Line

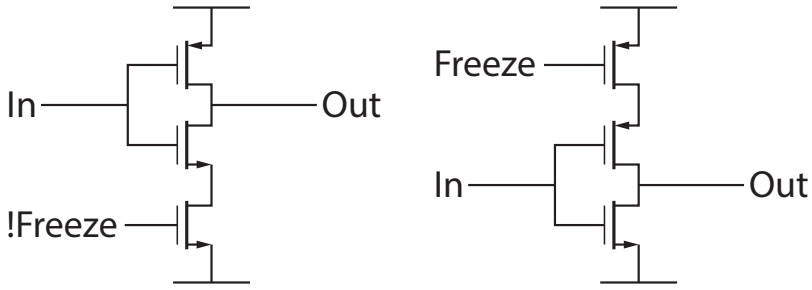
The disadvantage of the Gated Vernier Ring Oscillator is that the external signal has to drive a large capacitive load consisitng of all the delay elements in the loop. Furthermore, the start and the stop signal have to go through extra circuitry to operate the TDC. Finally, the ring oscillator itself has a nonideal layout which introduces delay mismatch between the stages, thus the timing error increases linearly with time.

In this paper, to create a low-power TDC and eliminate the loop error and the heavily loaded enable signal in the Vernier Ring Oscillator, the Freeze Vernier Delay Line is proposed. It is a Vernier delay line where, just like in the Vernier Gated Ring Oscillator, the delay lines can be frozen with the current starving technique. Unlike in the Vernier GRO, however, here the stop line acts as a disable input for the delay elements of the start line. This eliminates the extra circuitry in the Vernier GRO, and the disable signal is no longer heavily loaded as one disable signal is only connected to one delay stage. Furthermore, the proposed architecture is not in loop, thus the timing error does not increase by time as regular layout can be made.

The next section introduces the novel architecture. Then in section III the simulation results are presented. Finally conclusion is given.

II. Architecture

The proposed Freeze Vernier Delay architecture uses the principles of the Vernier-Gated-Ring-Oscillator [11]. In a



(a) N-Freezer Inverter (b) P-Freezer Inverter

Fig. 2: Freeze Inverters

gated-Vernier delay line [10], a ring oscillator is frozen [12] by disabling the delay elements. While conventionally this is done by an external signal for all delay elements synchronously, the novel architecture uses the stop signal to freeze the start line in a linear Vernier delay line. That is, the start and the stop signal are directly fed into the slow and fast line, respectively. When the stop signal reaches a certain stage in the fast line, it freezes the same stage in the slow line. At the end of the measurement, the start line is entirely frozen and the transition point indicates where the stop signal has caught up with the start signal. Usually at that point there are digitally invalid analog values, which need to be regenerated in order to provide the thermometer signal.

The functional description of the Freeze Vernier Delay Line is depicted on Figure 1a and 1b. While the stop signal has not reached the start signal, the start-line ideally behaves as a delay line with stages of identical delay. This phase of operation is the 'propagate' mode (Figure 1a) as the signal on the start-line is advancing uninterrupted. In a conventional Vernier architecture, the TDC operates only in this phase since there are external time capture elements. However, the proposed architecture has a second phase - the 'hold' mode (Figure 1b). This is when the measurement ouput must be provided by the delay line. In order to achieve this, the individual nodes must be independent from each other, i.e. the logic value of one cell should not influence the other. As a consequence the freeze inverters must separate their input from the output, with the freeze transistors (Figure 2a and 2b).

The proposed Freeze Vernier architecture fully benefits from the Vernier principle without the need for early-late detectors (ELD, usually a D-register or an arbiter [1]). This is done by freezing the node voltage of the slow line exactly at the moment when it is supposed to be sampled by an ELD. The stop signal, which had to drive, for example, the clock input of a D register, is now connected to a current-starved inverter [13] as an enable/disable input. Two options have been investigated - one where a delay element is only a current-starved inverter, and one where an additional inverter has been placed in one delay element, making it a buffer. In the case of the chain of inverters, the stop signal acts as either a true or complementary freeze signal. This means that every node is either connected to an active-high freeze input (header, Figure 2b) or an active-low freeze input (footer, Figure 2a) inverter in an alternating order, as it is depicted on Figure 3. With buffers, only active-low freeze current-starved inverters were used as the signal is not changing polarity (Figure 4).

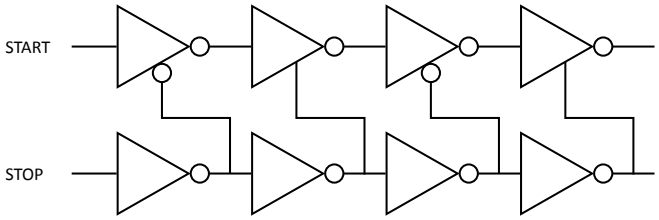


Fig. 3: Vernier Delay Architecture

The advantages of such a novel architecture are the following: the time capture blocks have been eliminated, thus it is not necessary to burn a lot of power to increase resolution. The measurement rate is also better as the start and the stop line are not loaded as heavily as they would be with an early-late detector. Also, the core can be extended with a coarse counter without much of an effort. The dead time has also improved as there is no external time capture circuitry which inevitably has a setup and hold time. The core does not need any type of reset signal - it resets on the falling edge of the stop and the start signal. The area is also much less with the lack of ELD's, which makes designing a chip with thousands of channels much easier. However in the frozen state, there are invalid logic values which generate large static power consumption and have to be regenerated with extra circuitry to provide valid bits. Similarly the stop line suffers from charge injection from the start line, causing second-order INL.

The Freeze Vernier architecture makes use of current starved inverters which can be enabled/disabled. This results in invalid digital logic values at the stages where the stop signal catches up with the start signal. The invalid logic values are present due to the finite transistion time of the freeze inverters; once the stop-line catches up with the start-line, the latter is frozen by the former. In some cases the start-line gets frozen during transition, this results in an invalid logic value. These invalid logic signals are regenerated by adding a bi-stable circuit to the output nodes, which are composed of a cross-connected inverter pair and a transmission gate. In order to

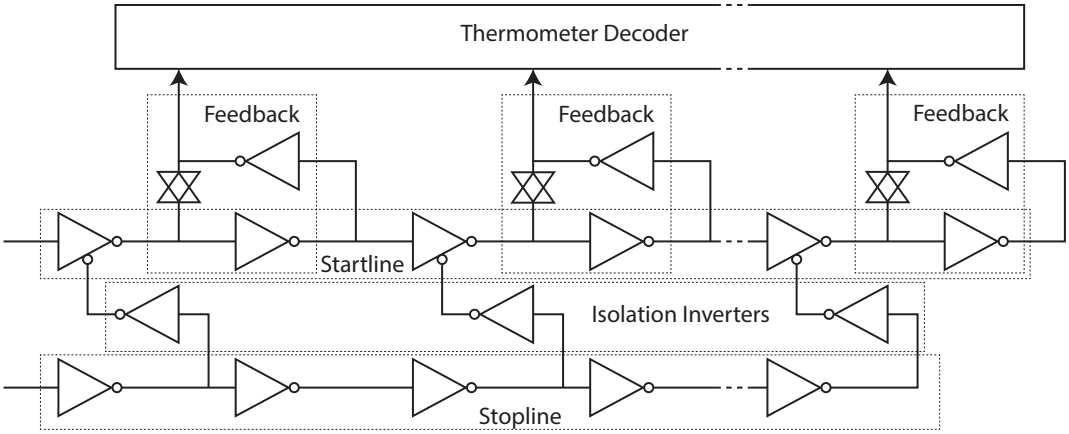


Fig. 4: Simplified Overview of the Buffer Stage Vernier Delay Architecture

provide a fast and precise start-line delay and maintain low power consumption, the feedback inverter of the inverter pair is connected to a transmission gate (see Figure 4). The control input of the transmission-gate is connected to the stop-line, which switches during each measurement since there are no freeze inverters in the stopline.

The Freeze Vernier architecture can utilize buffer and inverter delay elements. Usually, buffers stages are preferred over of inverter stages, since DNL in a TDC of inverter stages would be a major issue. With inverter stages, the Freeze Vernier architecture would use an inverter with NMOS footer transistor in the even stages, while the odd stages would be implemented with a PMOS header as freeze input. This causes considerable DNL, which is easily solved by using buffer stages. The area and power cost of using buffer stages is relatively high, however one of the two inverters needed for the output regeneration can be reused for the start-line buffer (Figure 4).

The start- and stopline are coupled through the enable/disable transistor in the freeze inverter. When the start signal propagates through the freeze inverter a small amount of charged is kicked back into the freeze transistor. The charge kickback causes a shift in the delay of the stopline stages which are near the switch point (point where the stop signal catches up with the start signal). The result is a second order INL. In the present design it was decided to shield some of the charge kickback by introducing an isolation inverter between the start- and stopline (see isolation inverters in Figure 4). This protects the stopline from most of the charge.

III. Simulation

We evaluated proposed Freeze Vernier TDC in 90 nm CMOS process. A buffer-based design in 65 nm is currently being investigated. We intend to report in the final manuscript a comparison of the two simulations.

The circuit was analyzed for the FF, SS, TT, FNSP and SNFP corners. In each of these corners the merits were calculated for different input delays. From the output code, the INL, DNL and resolution were extracted, as well as the supply current values were used to calculate the average power consumption, as it can be seen in the Table I.

TABLE I: Simulation results in SS, TT, FF corners

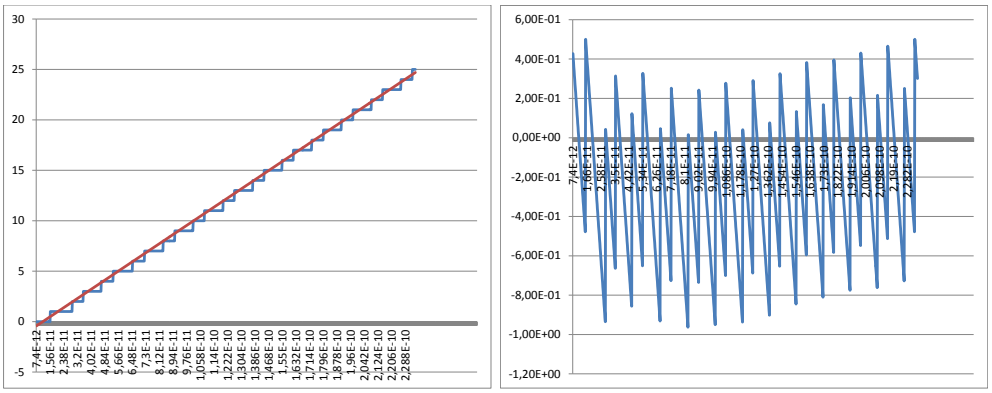
	SS	TT	FF	FNSP	SNFP
Resolution	13.6ps	9.06ps	6.493ps	9.46ps	9.07ps
Power	0.219pJ	0.239pJ	0.245pJ	0.212pJ	0.216pJ
INL	0.658	0.7313	0.567	0.469	2.71
DNL	0.813	0.963	1.139	0.939	1.09
Offset	10.4ps	6.74ps	5.306ps	8.94ps	4.39ps

In Figure 5 the DNL and INL result of the TT corner simulation is presented. The obtained DNL can be easily improved with a buffer-based Freeze Vernier TDC at the negligible cost in power. The INL is slightly above the half LSB level. The obtained DNL is to be improved with a buffer-based Freeze Vernier TDC, which will have slightly higher power.

The power consumption of the Freeze Vernier TDC - unlike that of the conventional Vernier TDC - depends heavily on the input delay, as shown in the Figure 6. The dependence of the power consumption on the input delay is a result of the architectural choice. Due to the freeze action the propagation of the start line is discontinued, therefore the rest of the start line does not switch state. In average this saves half of the power consumed by the start line for a random input. For the FF corner, the energy consumption for the entire range is 0.256pJ.

The area of the design sums up to 10.503 μm^2, the average resolution is 10.05 ps and the average energy consumption per conversion is 0.232 pJ for a power supply of 1 V, which corresponds to 0.232 mW power consumption for 1 GS/s sampling rate. The latter result shows considerable improvement over the state-of-the-art [3].

For future work, it would be possible to reduce the supply voltage - in the present work the supply voltage is 1.0 V, while decreasing it to 0.7 V will halve the power at the expense of higher DNL and lower resolution. Similarly, sizing the regeneration inverter will decrease the time the start delay line has invalid logic value, thus decreasing the power consumption.



(a) DNL for TT corner

(b) INL for TT corner

Fig. 5

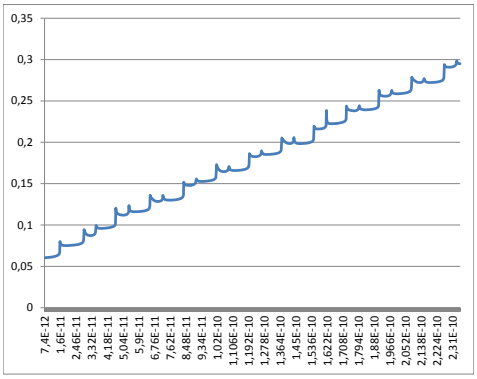


Fig. 6: Energy for TT corner

TABLE II: Comparison with other papers

	This Work	[10]	[14]	[6]
Resolution (ps)	13.6	3.2	4.7	1.25
Power (mW)	(core) 0.23	3.6/4.5	3.6	3
Area(mm^2)	(core) 0.00001	0.027	0.02	0.6
Technology (nm)	90	90	90	90

IV. Conclusion

The proposed Freeze Vernier Delay TDC is a high-speed, simple and reliable architecture with very low power consumption and a small area. The overall TDC consists of inverters and transmission gates only, omitting the power-hungry time capture elements like D-registers or arbiters that are usually employed in a Vernier TDC. A proof-of concept design has been simulated in 90 nm CMOS technology with a typical resolution of 10.05 ps, a dynamic energy consumption of 0.23 pJ per conversion and an area of 10.503 μm^2.

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