Designing pixel parallel, localized drivers of a 3D 1Gfps image sensor family

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Abstract

Currently, the highest frame rate achieved by a solid-state image sensor is 16.7 Mfps. To further increase the frame rate to 1Gfps, an image-sensing unit is proposed, which consists of a cluster of CCD pixels and a CMOS driver circuit in close proximity to it. Each pixel has multiple collection gates (MCG) that are driven by a local ring oscillator (RO) through level shifters and XNOR gates. One tape-out was completed, where several pixel arrays and driver circuits were implemented separately in a IMEC 0.13μm CMOS technology. Based on our results, a complete image sensor featuring localized drivers, 3D stacking, and backside illumination is currently being designed to achieve 1Gfps.

1. Multi-Collection-Gate Image Sensor

Figure 1 shows the MCG pixel structure of the test chip, where there are six gates surrounding the center of the pixel on the front side: one collection gate which is connected to the drain (B1) is denoted as drain gate (A1) and the other five collection gates (A2~A6) for electron collection are connected to the neighboring storage gates (B2~B6) [1]. The driving voltage VH, which is 3.3V higher than VL, is applied to one of the collection gates to exclusively collect signal electrons generated in the backside layer of the sensor chip. To start the collection operation, VL is applied to the drain gate; when to stop the collection, VH is applied. A simulation analysis of the sensor chip is presented in a sister paper [2].

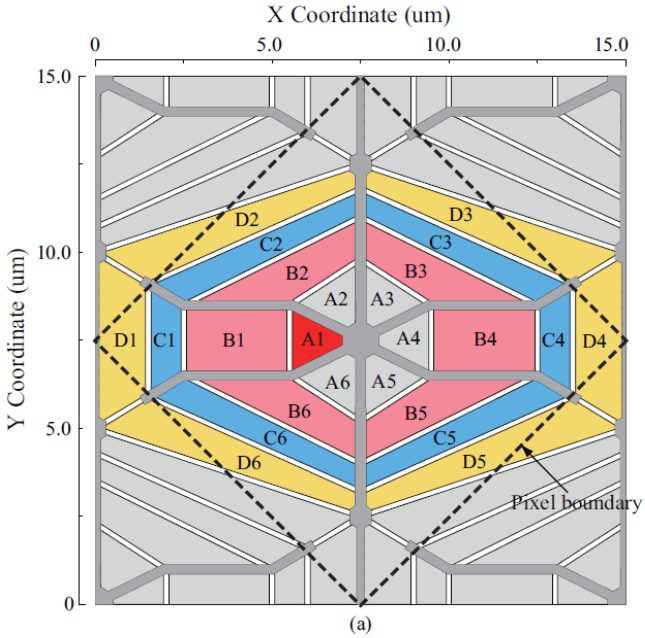


Fig. 1 Hexagonal MCG pixel model (A pixel is defined by a shaped p-well which guides signal electrons generated in the backside layer to the center of the pixel on the front side, where:
A1 and B1: drain gate and drain
A2-A6: collection gate
B2-B6: storage gate
Others: gates for signal transfer after an image capturing operation.)

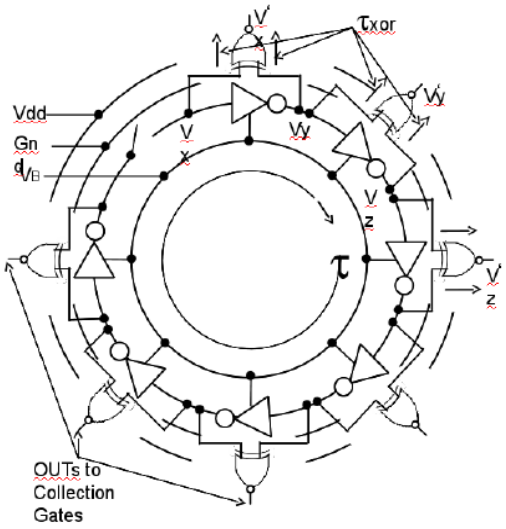


Fig. 2 Diagram of a RO-XNOR driver.

2. RO-XNOR Driver

The target of the driver is to generate continuous pulses with a pulse width that is programmable from 100ps to 1ns. The circuit that achieves this functionality comprises a ring oscillator (RO), level shifters, and XNOR gates,

as shown in Figure 2. A chip was fabricated in 0.13μm CMOS technology from IMEC to test the driver under actual operating conditions; the layout of the fabricated chip is shown in Figure 3.

At this time, the swing of MCG driving signals is 3.3V, but in future designs 1.2V will be used. Lower swing is helpful to increase frame rate to 10 Gfps and to reduce power consumption, due to the large parasitic capacitance of MCG pixels. To meet this requirement, a 1.2V RO was designed and level shifters were used to convert the voltage to 3.3V.

The RO needs to satisfy several requirements: (1) an accurate 50% duty cycle to ensure identical pulse widths for each cycle, (2) low power consumption to ensure scalability up to several Mpixels, (3) output voltage stability to ensure sensitivity and frame rate uniformity across the array. Considering these conditions, a 6-stage pseudo-differential RO was designed with 5 taps generating as many identical signals shifted by 1/12 of the clock period, which are then level shifted from 1.2V to 3.3V, maintaining the duty cycle unchanged. XNOR gates generate 5 continuous pulses with the designed pulse length by combining adjacent taps (see a simulation of the signals in Figure 4). The architecture is scalable and it enables high stability in terms of supply voltage variations. Temperature stability is achieved by locking a replica oscillator in a PLL with an external crystal. The actual signals generated by the fabricated chip are shown in Figure 5 (a) and (b), whereas the measured signals are compared with the original 5-corner simulations. The schematic of the RO-XNOR driver is shown in Figure 6 [3].

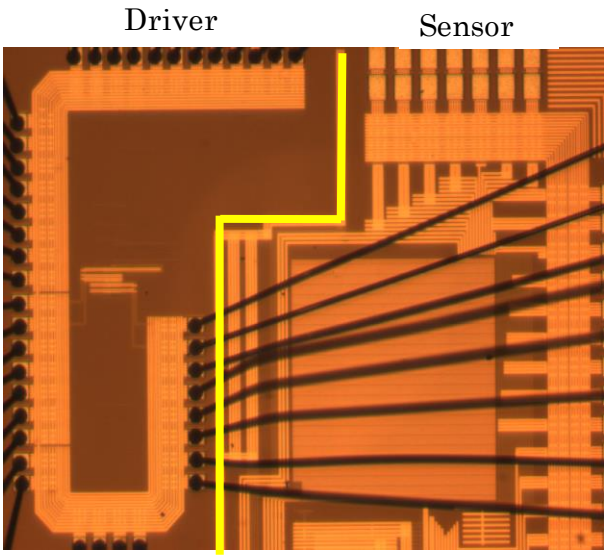


Fig. 3 Photomicrograph of driver and sensor.

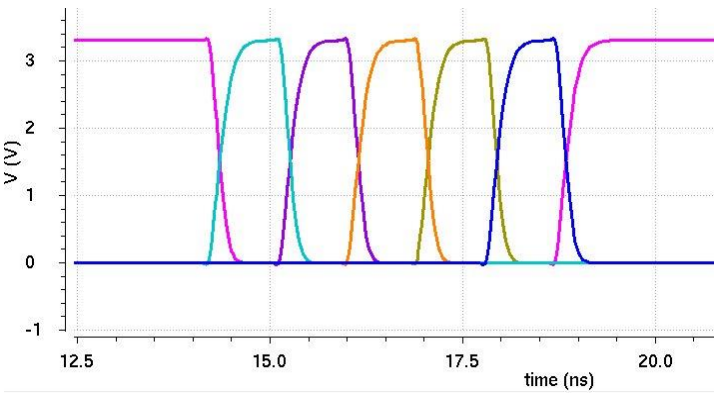
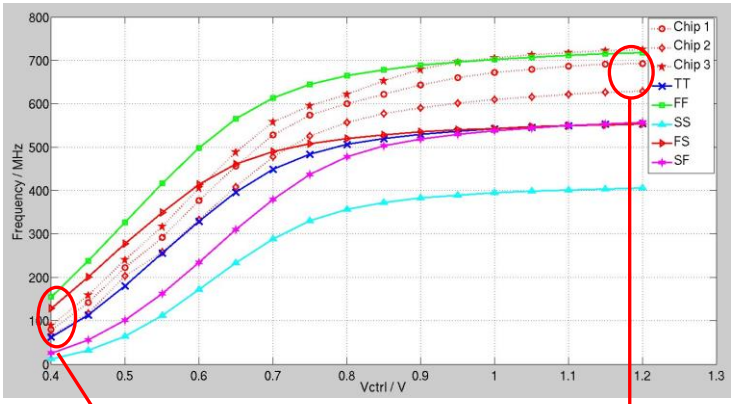
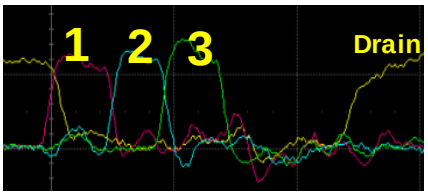
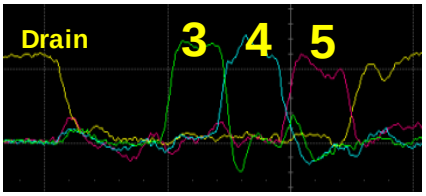


Fig. 4 Outputs of a RO-XNOR driver for the hexagonal BSI MCG image sensor
: Driving signal of the drain gate A1
: Driving signals of MCGs

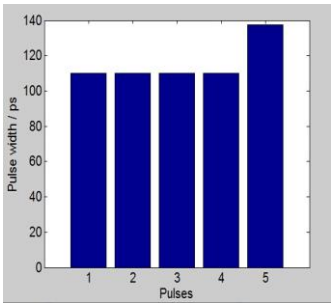


(a)





(b)



(c)

Fig. 5 (a) RO frequency versus control voltage (dashed curves are measurement results, solid curves are simulations at 5 corners); (b) MCG driving signals observed with oscilloscope with the width of 2.2ns to 3ns; (c) pulse width measured by TDC at about 700MHz.

In conventional up-convert level shifters (Figure 7 (a)), because of the high threshold voltage of PMOS transistors, 1.2V input cannot turn off MP1 and MP2 completely. So large input NMOS transistors (MN1, MN2) are needed to pull down the output voltage, thus increasing static current and load capacitance of the RO [4]. In this design, a 2-stage level shifter is proposed, which addresses this issue, as shown in Figure 7 (b). In the first stage, two NMOS transistors (MN3, MN4) are biased in triode region and connected in series to VDD, so the effective supply voltage drops to '3.3-Vthn', which dramatically reduces the static leakage current. While the output voltage still can pull up to 3.3V due to the absence of two cross-coupled PMOS transistors (MP3, MP4). To improve the pulse uniformity, the second stage was used to optimize the duty cycle to be exactly 50%.

Since the pulse width is too short to be observed directly, a Vernier-Delay-Line TDC was utilized to accurately measure the pulse width and uniformity [5]. The 'Start' and 'Stop' signals are triggered by the rising and falling edges of the pulse respectively, thus the time difference will be measured by the TDC, which stands for the width of pulse. The TDC has 40 stages with a latency of approximately 1.1ns and an LSB of 27.5ps. The TDC diagram is shown in Figure 8(a) and DNL/INL measurement results are shown in Figure 8(b) and (c). The pulse uniformity characterized through the TDCs is shown in Figure 5(c), for a clock frequency of 700MHz, whereas the pulse width is about 120ps.

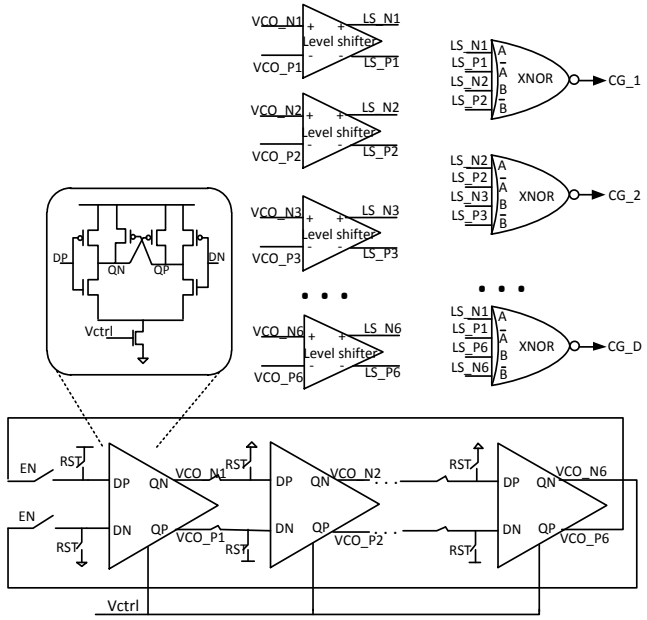


Fig. 6 RO-XNOR driver circuits, where CG_1 ~ CG_5 are driving pulses for the 5 collection gates, CG_D is for the drain gate. Level shifters will be removed when 1.2V pulses are applied.

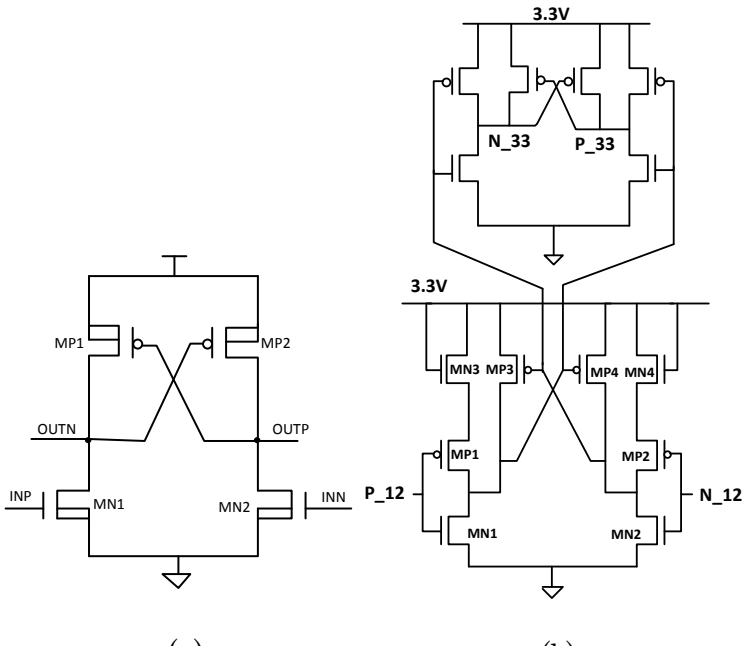


Fig. 7 (a) Conventional level shifter; (b) Proposed 2-stage level shifter.

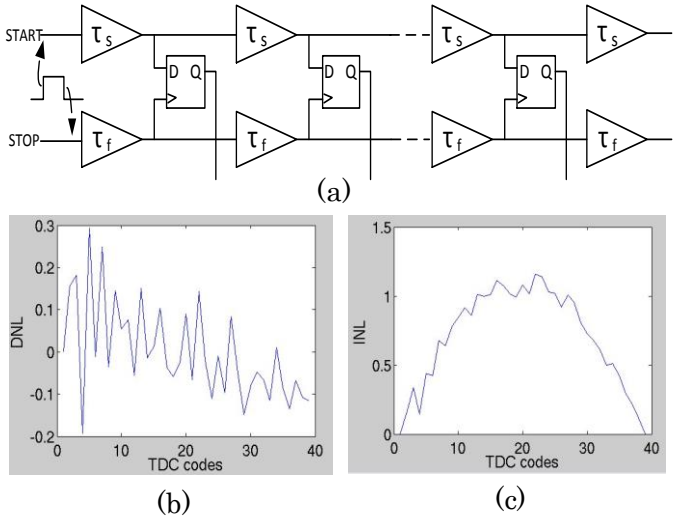


Fig. 8 (a) Vernier-Delay-Line TDC; measurement results of (b) DNL and (c) INL

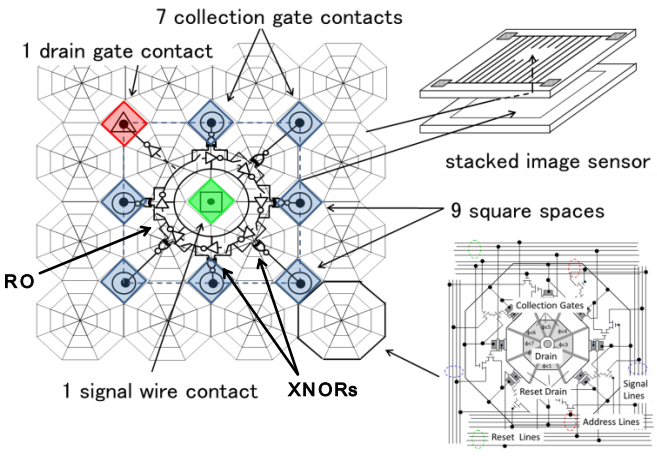


Fig. 9 A 3D-stacking image sensor demonstrator with octagonal MCG pixels and pixel-based RO-XNOR drivers.

3. 3D BSI 1Gfps Image Sensor

To achieve a fill factor of nearly 100%, the MCGs are backside illuminated (BSI), while the driving signals are generated in a separate chip stacked underneath to reduce parasitic capacitance and to minimize skew across the image sensor; these measures are necessary to ensure 1Gfps with large pixel counts. The structure of the proposed 3D BSI image sensor with localized drivers is shown in Figure 9, where a 512x512 MCG BSI pixel array will be implemented. The MCGs are located in the top chip and the localized RO-XNOR driver array in the bottom chip; the interconnections between chips are achieved by high-density micro-bumps with a fine pitch of 18µm that are part of the 3D stacking technology from IMEC utilized in this project. Each RO-XNOR driver is to be shared by one or several pixels, so that the load capacitance for each driver is further reduced.

The RO frequency will be controlled by the PLL, while pixels will be driven simultaneously by the RO-XNOR drivers to minimize smearing. To minimize the effects of power consumption peak upon activation, a large, localized array of decoupling capacitances will be distributed across the array and on the periphery. Due to the speed and skew challenges, in this design we are adopting strict RO matching, IR drop mitigation, synchronized timing control, and global power control.

References

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