A 1.2V 84dB 8mW Time-Interleaved Sample and Hold Circuit in 90 nm CMOS

Amir Zjajo
Circuits and Systems Group
Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands
amir.zjajo@ieee.org

***Abstract*—This paper reports design, efficiency and measurement results of time interleaved sample and hold circuit based on closed loop switched capacitor technique. The prototype sample and hold with 84 dB dynamic range at 120 MS/s has been fabricated in standard single poly, six metal 90 nm CMOS, consumes only 8 mW at 1.2 V power supply and measures 0.22 mm^2.**

I. INTRODUCTION

In highly integrated telecommunication systems, moving analog-to-digital converters (ADCs) capable of IF-sampling towards the high frequency front-end maximize economic value-exploiting system complexity. However, the rapidly decreasing feature size and power supply voltage of deep-submicron CMOS technology increases the pressure on converter requirements. Combining time-interleaved sample and hold (S/H) circuit with efficient moderate speed converter [1]-[2] can result in a high speed, high resolution ADC with low power consumption, making it effective for embedding in system-on-chip. In this paper, we present compact, low-area, low-power time-interleaved sample and hold circuit based on closed-loop switched capacitor technique and suitable for multi-step/pipelined analog-to-digital converters.

II. TIME-INTERLEAVED SAMPLE AND HOLD

The sampling rate of a multi-step/pipelined ADC is increased with time-interleaved technique [3], where a higher sampling rate is obtained by running the system in parallel (Figure 1), although at different clock phases. For proof of concept, we choose the three-time interleaved S/H consisting of three identical units. Since the clock signals are one high out of three, each sample-and-hold unit is sampling during one clock period and holding during the other two enabling different actions on each of the separate channels to proceed at the same time on different analog samples as shown in Figure 2. At the sampling phase, the sampling behavior depends on the unit gain bandwidth and phase margin of the circuit. On the other hand, at the hold phase, the settling behavior mostly depends on the closed-loop time constant of the amplifier only. Because the feedback factor is smaller than one, the phase margin is not an issue at the hold phase. To avoid switch on-resistance non-linearity, the sample switch is bootstrapped. The opamp in S/H units is implemented as folded cascade amplifier with gain-boosting auxiliary amplifier. The op amp size and its bias current for a given speed requirement and minimum power dissipation is determined using time constant τ versus hold capacitance C_H curve. In the front-end S/H, where the clock is used to sample a continuous time signal, any deviation of the sampling moment from its ideal value results in an error voltage in the sampled signal equal to the signal change between these two moments [4]. The clock skew between the sampling clocks of distributed S/H circuits can be calibrated by measuring its value and controlling tunable delays of a DLL [5]. Nevertheless, in general, calibration of the skew between S/H circuits has two significant drawbacks. First, skew measurement is complex and second, the tuning of the delays requires high accuracy from the calibration hardware and algorithm. In this design, we obtained timing alignment within the required accuracy by using a master clock to synchronize the different sampling instants while matching the channels clock and input signals lines. Additionally, the delays of any active buffers within the clock distribution network are kept to the minimum. Besides timing mismatch, time-interleaved S/H suffers from offset, gain and bandwidth mismatch [6]. One limitation of the offset cancelling method [7] from a systems point of view is the fact that the static offset has to be measured before the calibration. The gain mismatch can be calibrated digitally by measuring the reference levels and storing them in a memory. The ideal output code can be recovered using these measured reference levels [8]. In our implementation the resulting *dc* offset is mainly cancelled with design percussions, such as differential signal path, bottom plate sampling, small feedback switches, opamp high common-mode rejection ratio and by using the closed loop sampling architecture such that consequent offset mismatch is sufficiently low for the required resolution. By dimensioning the open loop *dc*-gain of the operational amplifiers large enough, the effect of gain mismatch is suppressed below the quantization noise level. With careful sizing and layout, capacitor matching sufficient for more then twelve bit resolution is achieved. By increasing the bandwidth, the impact of the bandwidth mismatch at the signal frequency becomes lower. For this reason, the bandwidth of each S/H unit is larger than what is required when just looking at signal attenuation.

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A prototype sample and hold was fabricated in a standard single poly, six metal 90 nm CMOS (Figure 1). The stand-alone circuit occupies an area of 0.22 mm^2 operates at 1.2 V supply voltage and dissipates 8 mW. In order to reduce wiring capacitance in the input path, front-end sample and hold input is routed as symmetrical and short as possible. Power and ground lines with maximal allowed width are overall routed to reduce the voltage drop. Since the analog sections are susceptible to noise coupling from the digital sections, they are constantly kept separated. Critical clock lines have been provided with shielding. In measured spectrum in Figure 3, the largest spike, other than the fundamental input signal, is the spurious harmonic which appears at $fs/3 \pm f_{in}$ and is 84 dB below the fundamental signal. The SNR, SFDR and THD as a function of input frequency at a sample rate of 120 MS/s are shown in Figure 4. Measurements across 25 samples show ±0.2 ENOB variations. The degradation with a higher input signal is mainly due to the parasitic capacitance, clock non-idealities and substrate switching noise. Parasitic capacitance decreases the feedback factor resulting in an increased settling time constant. The three latter errors reduce the time allocated for the setting time. A locked histogram test revealed a 0.5-ps rms jitter in the system including the clock generator, the synthesizer, the A/D comparator chip and the board, which translates to a 74-dB SNR at 60 MHz approximately. This confirms the observation that the performance of sample and hold is limited by the clock jitter at high input frequencies.

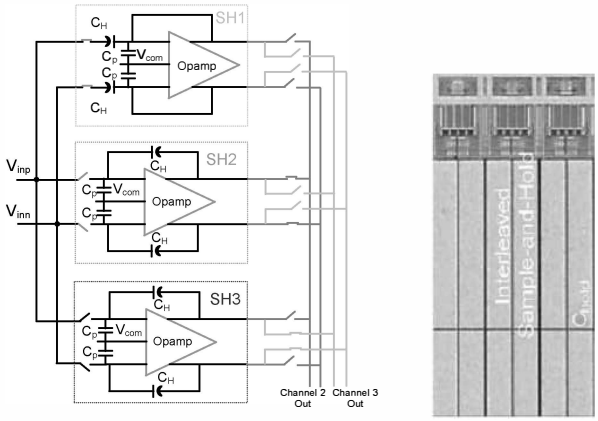

Figure 1: Left) Total S/H circuit consisting of three time interleaved S/H units at the moment when S/H1 is sampling and S/H2 and S/H3 are holding, Right) Chip micrograph.

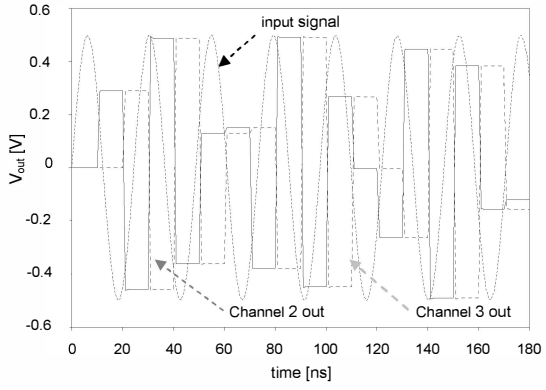

Figure 2: Simulated time domain sample and hold output.

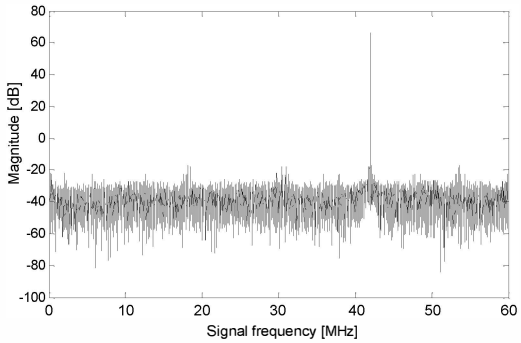

Figure 3: Measured spectrum the time-interleaved S/H at 120MS/s

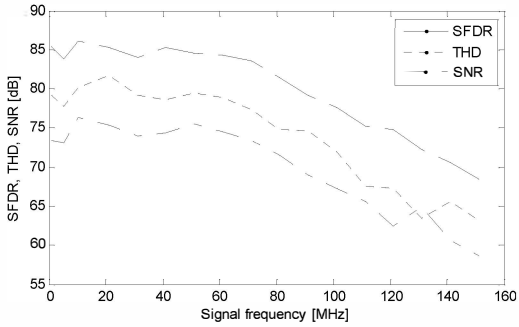

Figure 4: Measurement result of the time-interleaved S/H at 120MS/s

III. CONCLUSIONS

The feasibility of the method has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal 90 nm CMOS. The stand-alone sample and hold with 84 dB dynamic range at 120 MS/s occupies an area of 0.22 mm^2 operates at 1.2 V supply voltage and dissipates 8 mW.

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