A Low-Power Digitally-Programmable Variable Gain Amplifier in 65 nm CMOS

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ABSTRACT

This paper reports a new topology for a switched-capacitor variable gain amplifier (SC-VGA), which allows discrete-time periodic analog signal generation and in essence fulfils the function of the D/A converter. The proposed circuit exploits a pipelined, cascaded gain stages, which leads to simpler circuit implementation, lower power consumption and reduced *kT/C* noise, compared to the conventional implementation. The method has the attributes of digital programming and control capability, robustness and reduced area overhead. The two-stage SC-VGA has been fabricated in standard single poly, 65-nm CMOS with the core area of 0.17 mm^2 and shows the maximum gain variation of 70 dB and 81 dB linear range, while consuming 11 mW.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and design styles - VLSI

General Terms

Performance, Design, Reliability.

Keywords

Variable gain amplifier, waveform generator, discrete-time amplifier.

1. INTRODUCTION

The variable gain amplifier (VGA) is an essential component of many mixed-signal applications such as hearing aids, disk drives, wireless receivers, power-line communication, etc. The VGAs processing continuous time signal usually employ nonlinear characteristics of transistors to obtain exponential gain control [1]-[5]. On the other hand, the VGAs, which process a sampled signal usually utilize switched-capacitor circuits with programmable capacitor arrays. To achieve exponential gain control in the switched-capacitor circuits, the effective capacitances of the arrays should be controlled exponentially. To obtain a fine step gain control, the capacitor array should be composed of many capacitors with different sizes [6], which make the design and layout complicated. To overcome these problems, a circuit topology in [7] employs the first order approximation of the exponential function [8]. Additionally, in a switched-capacitor variable gain amplifier, parameters such as finite *dc* gain, linear settling and slew rate can raise the quantization noise floor or introduce distortion depending on the circumstances. Thermal noise introduced by the sampling process as well as by the amplifiers adds directly to the quantization noise. Finite amplifier *dc* gain degrade both the distortion and noise performance and change the positions of the poles in a switched-capacitor VGA. The pole shift has an impact on the choice of operational amplifier topology in practical designs. Since the effects of the pole shifting are difficult to calibrate due to its small values, the amplifiers with large *dc* gains have to be employed. Linear settling and slew rate specify the small signal and large signal speed performance of a VGA, respectively. A linear settling error results in a VGA gain error while slew rate results in harmonic distortion. Due to the low g_m/I ratio of short channel CMOS devices and the required high speed operation, this distortion constraint will be satisfied if the amplifier slews for a small fraction of the settling period and spends the majority of its time in a linear settling regime. Maximizing the output swing will increase the maximum signal handling capability. For a *kT/C* noise limited design, this will minimize the required sampling capacitance and power dissipation.

The proposed VGA is not sensitive to parasitic capacitance at the output node as the VGA does not have to swing a large voltage range; it can tolerate larger and more nonlinear parasitic capacitance and be less sensitive to noise. Furthermore, high-output-impedance amplifier is used as it tends to have higher unity-gain frequencies, be simpler and have less power dissipation. Similarly, the classic VGA suffers from two important drawbacks. First, the input-dependent charge injection of input switch introduces nonlinearity in the charge stored on the hold capacitance. Second, the nonlinear capacitance resulting from the source/drain junctions of input switches leads to a nonlinear charge-to-voltage conversion. In SC-VGA, although its output is a continuous waveform that does not incur any large slew-rate requirement, such a circuit will also amplify the *1/f* noise and opamp offset voltage with the gain *G*. To suppress finite offset and opamp gain as well as *1/f* noise, correlated double sampling is employed. Additionally, with a new topology, a wide gain range (-10 to 60dB) with a fine gain step and small gain nonlinearity is achieved.

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2. DESIGN OF DISCRETE-TIME WAVEFORM GENERATOR

2.1 On-Chip Waveform Generator System

Conventional sine-wave signal generation methods relay on an analog oscillator consisting on a filtering section and a non-linear feedback mechanism [9] or by adapting digital techniques, which facilitates a digital interface for control and programming tasks [10]-[13] or by employing the programmable integrator followed by filtering segment [14]. In an analog oscillator based techniques a non-linear feedback mechanism forces the oscillation while the filtering section removes the unwanted harmonics. However, the quality of the generated signal depends on the linearity and selectivity of the filter and the shape of the nonlinear function (smooth functions are needed for low distortion), which requires a lot of area and power. In digital techniques, by exploiting the noise shaping characteristics of ΣΔ encoding schemes use of the D/A converter is avoided [10]-[13]. In essence, a one-bit stream ΣΔ encoded version of an *N*-bit digital signal is generated and the shape of a filter is matched with the noise shaping characteristics of the encoded bit stream. Although, these schemes are valid for single and multi-tone signals they require large bit-stream lengths and a highly selective filter to remove the noise. In addition, these approaches are frequency limited due to the need of very high over-sampling ratios. On the other hand, the proposed programmable VGA allows discrete-time periodic analog signal generation and in essence, fulfils the function of the D/A converter.

The block diagram of the proposed system for the on-chip waveform generation is shown in Figure 1. It consists of a non-overlapped clock generator, a programmable (two-) gain stage combined with linear time-variant filter forming a programmable sine-wave generator, a clock mapping blocks, gain decoders, and a digital control unit. Based on an external master clock, the non-overlapped clock generator generates the appropriate clock signals for the signal generator and the programmable filter. The amplitude of the generated signal is adjustable to make it suitable for the input range of the device-under-test. The signal generator has two cascaded gain stages: a first gain stage (FGS) and a second gain stage (SGS), where the overall gain is the sum of the gains, of the FGS and SGS. The amount of gain realized by the first- and second gain stages is controlled by an array of non-overlapped clocks coming from the FGS and SGS gain mapping block, respectively. The select signal serves as a sequential selection signal feeding reference values to the programmable gain amplifier gain stage. Consequently, and in order to have independent control of the gain stages, the first- and second gain clock mapping units generate a different array of clocks. Gain decoders generate combinational logic information on how a particular gain is realized in the first and second gain stages. Two decoders are therefore needed, an FGS gain decoder, and a SGS gain decoder for independent gain control. A state machine and two control muxes control the manner in which the information from the digital decoder is fed to the first- and second gain clock mapping unit, respectively. The programmable, high-Q bandpass filter selects the proper harmonic component at the output of the generator for magnitude response or harmonic distortion characterization of the device-under-test (DUT). One of the main advantages of the proposed system is its inherent synchronization; both the stimuli frequency and the filter center frequency are controlled by the master clock; when it is swept, both the signal generator and the filter follow these adjustments. The proposed testing strategy does not require any device-under-test re-configuration and is able to directly test frequency response related specifications. Before the characterization of the DUT, the functionality of the method can be easily verified by bypassing the output of the signal generator. A timing diagram showing the processing of data through the gain stages is illustrated in Figure 2. When FGS or SGS select is high, first or second gain stage is processing data, respectively.

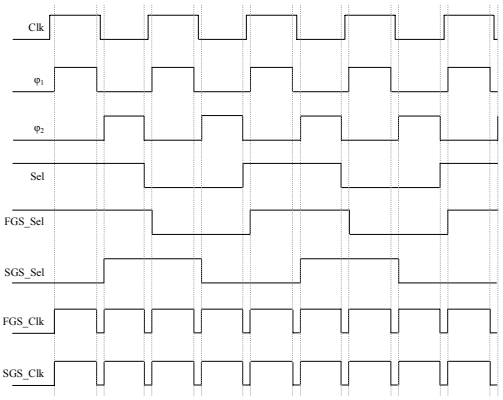

Figure 2: Timing diagram of the system

At the clock rising edge, the first gain stage starts acquiring data. When the FGS starts holding, the second gain stage starts attaining the FGS data. When the first gain stage finishes holding the SGS has fully acquired the signal from the first gain stage. It should be noted that the FGS_Sel and SGS_Sel signals are 90 degrees out of phase due to the reversal of roles between φ_1 and φ_2 in the two stages.

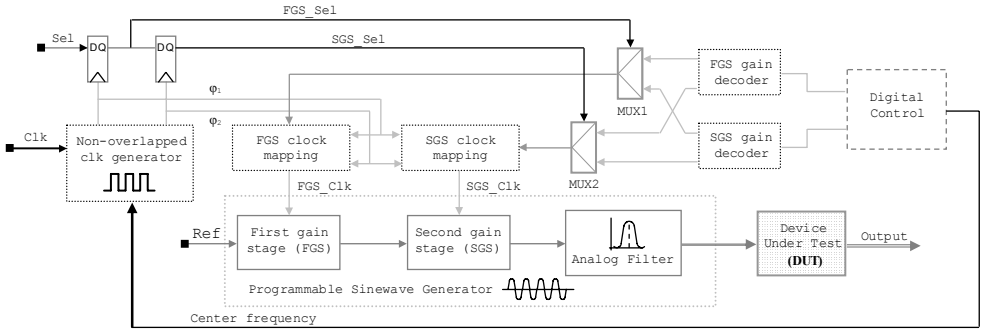

Figure 1: Overview of the proposed system for the on-chip analog signal generation

2.2 Variable Gain Amplifier

In order to achieve a wide gain range of 70 dB, precise gain settling, lower harmonic distortion and high clock rate operation while maintaining low power dissipation, FGS and SGS of the programmable waveform generator, shown in Figure 1 and given in Figure 3, employ two pipelined stages. The first stage is designed to have a coarse gain tuning control while the second stage provides the fine gain tuning. The circuit includes seven fully differential amplifiers and high-resolution capacitive banks for accurate segments definition of a discrete-time periodic analog signal. The FGS stage is a cascade of three amplifiers of FG_1, FG_2 and FG_3 while the SGS stage is designed with a parallel connection of three weighted gain amplifiers of SG(H), SG(M) and SG(L). Each pipelined cascaded SC amplifier operates with two clocks, φ_1 and φ_2, which are non-overlapping. In the φ_1 phase, the reference signal is sampled at the input capacitors of the first stage to be transferred, and in the next phase, on the feedback capacitor. Simultaneously, the output signal of the first stage is sampled by the input capacitor of the next stage. Each stage of Figure 3 operates in the same manner. The overall operation is shown in the timing diagram of Figure 4. With the exploit of a four step capacitor array as the analog up-sampler programmable gain stages (FGS and SGS) whose preset gain stages correspond to the values of an ideally sampled and held sine wave can be constructed. The gain in the first stage is set by the feedback capacitance. For example, in the first pipelined amplifier stage FG_1, the input capacitance is chosen as $4C_{F1}$, and the feedback capacitance is then given by $4C_{F1}/G_{F1}$, where G_{F1}=1, 2 or 4. The switches s_1 through s_4, which control feedback capacitances are closed sequentially for one clock period to generate the four steps of the sine wave. Once the maximum value of generated waveform is obtained, the switches close sequentially for one clock period in the opposite direction (from s_4 to s_1) to generate the second quarter-period; in this case the polarity of the reference voltage is changed through φ_{in} to generate negative and positive amplification, respectively. The charge injected by the input capacitors is integrated on the feedback capacitors to generate the first quarter-period of the sinusoidal waveform. Two small capacitors are added to subtract error voltage from the input signal (applied to the opamp input) during s_4, when this error is the largest. Bottom plate sampling is implemented with the clock phase s_{1a}, which is a slightly more advanced version with respect to the clock phase s_1. The parasitic capacitances at the top plate of the holding capacitor and at the input of the operational amplifier are always connected to a fixed potential and therefore do not affect the operation of the circuit.

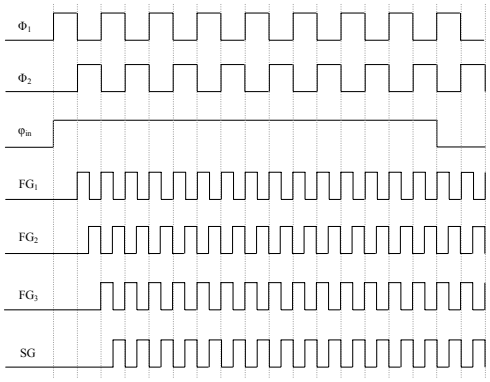

Figure 4: Timing diagram of the two gain stages

Parasitic capacitances at the input and output of the operational amplifier only have an effect on the settling speed of the operational amplifier, and do not introduce error, if taken into account in the characterization of the settling time of the operational amplifier.

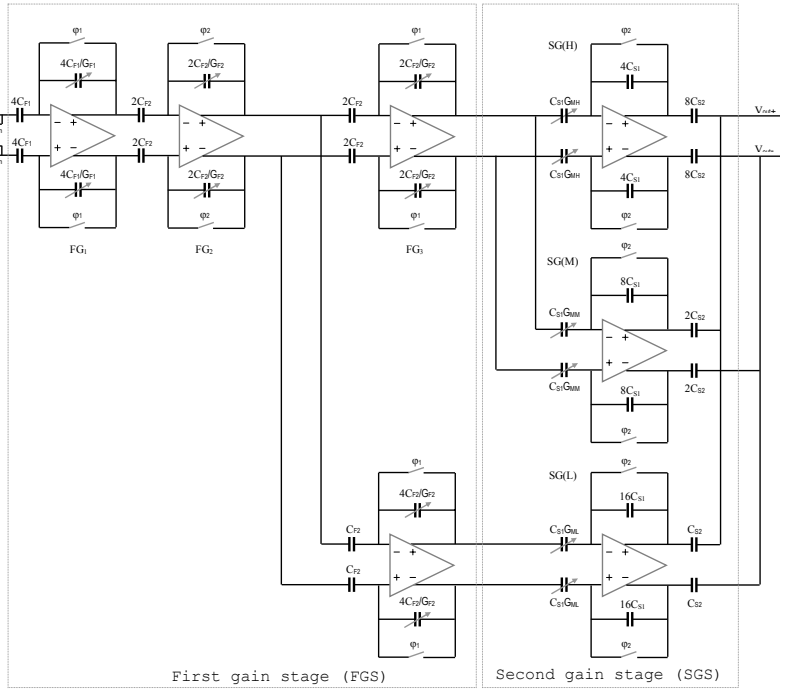

Figure 3: Variable Gain Amplifier schematic

The effect of the parasitic capacitances at the bottom plate of the hold capacitor is also canceled. Even though the parasitic capacitances are charged to the input voltage V_{in} in the first phase, the parasitic capacitances are discharged to a fixed potential in the second clock phase and no discharge current flows through the hold capacitor. In the second stage, the gain is set by the input capacitance. The high resolution of the gain is achieved by the parallel connection of three SC amplifiers. To illustrate that, consider, the SG(H) stage, where the input capacitance is chosen as $C_{S1} \times G_{MH}$ with G_{MH}= 2, 3,…, 7, so that the gain is set to $C_{S1} \times G_{MH}/4C_{S1}=G_{MH}/4$. To avoid inaccurate waveform generation matching between two or more capacitors is of the utmost importance. However, with a use of various layout techniques such as integer ratios of unit capacitors, deployment of unit elements with the same shape or area to perimeter ratio, and unit elements centroide form, layout matching of <0.05% was feasible. To realize the desired capacitance with adequate accuracy, the size of each unit element is, thus, not to small, otherwise its desired value would be submerged by normal fabrication tolerances. When the gain is changed in discrete steps, there may be a transient in the output signal. There are two different causes of transients when the gain of a programmable gain amplifier is changed. The first is the amplification of a *dc* offset with a programmable gain, which produces a step in the output signal even when the amplifier has no internal *dc* offsets or device mismatches. Second, when the gain of a programmable gain amplifier is changed in a device, in which *dc* current flows, the *dc* offset at the output may be changed due to device mismatches, even when there is no *dc* offset at the input of the amplifier. In the first case, the cause of a transient is in the input signal, which contains a *dc* offset. In the latter case, the output *dc* offset of the programmable gain amplifier depends on the gain setting because of changes in the biasing, i.e. the topology of the VGA and mismatches cause the transients. The step caused by a change in the programmable gain may be a combination of both effects, although if properly deployed, the following high-frequency low-pass filtering stage will filter out this step if sufficient small time constant is deployed.

2.3 Gain Stage Amplifiers

The opamps in the first and second gain stages were implemented as gain-boosted folded cascode amplifiers as shown in Figure 5. To reduce the power consumption, the opamps used in the second gain stage are implemented with a lower gain-bandwidth product than the first gain stage opamps due to the larger range of feedback factors required to realize the different FGS gains. Since FG1 amplifier experiences no large signal swings, an input pair is formed with only *p*-channel transistors due to their superior *1/f* noise properties. In other amplifiers, a *n*-channel input pair $T_{1\text{-}2}$ is placed in parallel with a *p*-channel input pair $T_{3\text{-}4}$ to process signals from rail to rail. To make the transconductance as a function of the common-mode input voltage constant a simple feed-forward method is applying current switches $T_{5\text{-}8}$ [15]. The current switches are divided into two transistors of which the drains are connected to the drains of the corresponding input-stage transistors. By adding the currents to the outputs of the input-stage transistors the output current of the input stage does not change as a function of the common-mode input voltage. Since relatively small current-switch transistors can be used, their noise contribution to the noise of the amplifier can be made relatively small. A common-mode feedback circuit consists of $T_{23\text{-}35}$ [16]. In this implementation, the resistor/capacitor network in balanced resistor/capacitor differential-difference amplifier common-mode feedback structure is replaced by a transistor network consisting of $T_{23\text{-}28}$, so that the output common mode level can be sensed without changing the impedance at the system output. The signal path from the opamp output to the gate of T_{32} is built exclusively by source-follower stages, so the gate voltage $V_{G(T32)}$ is a monotonically increasing function of the output common-mode level. Similarly, since $T_{23\text{-}28}$ are complementary types of transistors, the output common-mode level is guaranteed to be detected in full-swing range without pulling any transistors of $T_{31\text{-}35}$ away from the saturation region. Additionally, since all nodes in the network $T_{23\text{-}28}$ are low impedance nodes, no additional stability problems will occur.

2.4 Switched-Capacitor Filter

The major bottleneck of realizing a high-frequency CMOS SC filters is the requirement for high-gain and large-bandwidth op-amps, which provide virtual grounds for accurate charge transfer [17]. Although it is possible to realize CMOS op-amps that can provide the required gain and bandwidth values, the resultant high power consumption often hinders the practical realization [17]. Besides the large-gain-bandwidth approach, two techniques, which are meant to enhance a CMOS SC filter's ability to operate in the megahertz range, can be roughly classified into two groups: op-amp based and unity-gain-buffer based [18]-[19].

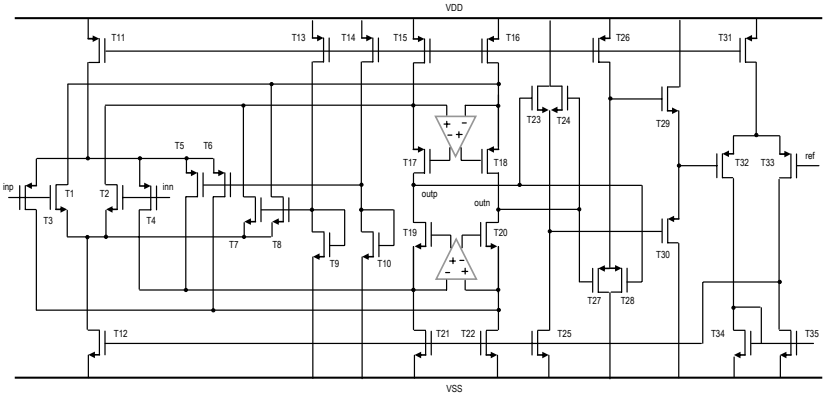

Figure 5: Opamp schematic

A typical unity-gain buffer is able to operate over a much wider signal bandwidth than the conventional op-amp. In addition, this buffer can be realized using simpler circuitry; as a result, it occupies less silicon area and consumes less power than a conventional large-gain-bandwidth op-amp does. However, unity-gain buffer -based SC filters suffer from parasitic capacitances, which are mainly caused by the source-gate diffusions in the unity-gain buffer's input transistors, whose values tend to vary with process and temperature. Similarly, the parasitic-insensitive techniques are not applicable on unity-gain buffer-based SC filters, due to its inherent low gain. On the other hand, the large-bandwidth or high-speed op-amps tend to have low *dc* gains due to the fundamental tradeoff between *RC* time constant and $g_m R_{out}$. A low op-amp *dc* gain tends to introduce nonlinearity errors to the SC integrator's output, hence compromising the filter's accuracy performance. As a response to this problem, op-amp-based techniques typically emphasize modifying the traditional op-amp structures so that the resultant new op-amps are capable of fulfilling both the speed and accuracy requirements of high-frequency SC filters, despite the fact that they typically have low *dc* gains. In this implementation, the gain regulating approach [20] is followed, where the low *dc* gain of each large-bandwidth op-amp in the high-frequency SC filter is precisely controlled and the regulated gain value is used as a reference to scale the capacitances in the circuit.

3. EXPERIMENTAL RESULTS

A prototype micrograph of the programmable waveform generator fabricated in standard single poly, 65-nm CMOS with the core area of 0.17 mm^2 is shown in Figure 6. The waveform generator has been laid out through a two-level matching process. In lower level, the internal transistors of every opamp have been laid out following a common centroid technique. Equally, in the higher level, opamp cell has been arranged in a common centroid structure as well. A similar rule has been applied for capacitors, which have been laid out in an array of unit capacitors with common centroid geometry.

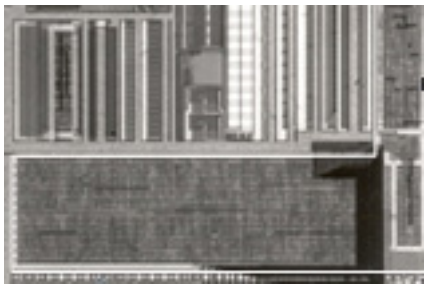

Figure 6: Prototype micrograph

The filter outputs were buffered using a simple source follower before connecting them to the pads. Power and ground lines with maximal allowed width are overall routed to reduce the voltage drop. Since the analog sections are susceptible to noise coupling from the digital sections, they are constantly kept separated. Critical clock lines have been provided with shielding. All analog paths were differential to increase the rejection of common mode noise, such as substrate noise and supply voltage fluctuations. To reduce switching noise on power supply lines on-chip decoupling capacitors are employed. Routing of the digital signals is placed between digital parts. Using this total arrangement there is a minimum of analog and digital signal lines crossings. The dense layout minimizes wire capacitances, so that most nodes are dominated by transistor parasitics and the performance of the waveform generator is primarily determined by the circuit design. The frequency response of the variable gain amplifier is shown in Figure 7 and in-band IIP3 interpolation point is given in Figure 8. In-band two-tone linearity test is illustrated in Figure 9. The performance parameters of the test chip as well as of the previous works in the literature are summarized in Table 1. The noise and power consumption are optimized with respect to the results of the required linearity. Table 2 gives a comparison between the presented generator and other reported approaches. It demonstrates that the proposed waveform generator based on switched-capacitor technique with the measured performance of 81 dB at 41 MHz while occupying only 0.17 mm^2 is currently the best reported and the only one available for testing of high-speed, high-resolution of up to 12 bit A/D converters.

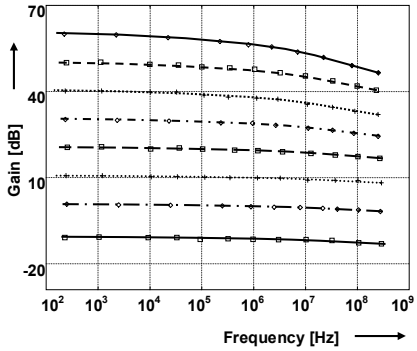

Figure 7: Measured gain response of the fabricated chip

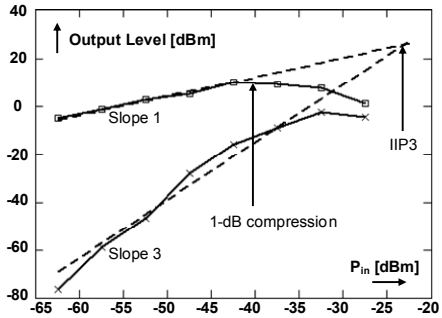

Figure 8: Measured IIP3 for maximum gain setting of 60 dB

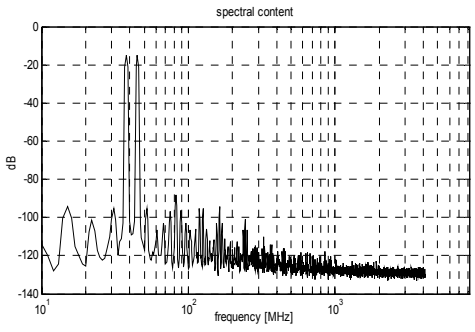

Figure 9: Measured frequency response

4. CONCLUSIONS

The analog circuits are usually evaluated using functional approaches, often requiring a large data volume processing, high accuracy and high speed ATEs. In addition, these analog cores are normally very sensitive to noise and loading effects, which limit the external monitoring. On-chip evaluation and generation of periodic signals are of undoubted interest from this point of view. They have wide application as most of the analog systems (filters, A/D converters, D/A converters, signal conditioners, etc.) can be characterized and tested (frequency domain specifications, linearity, etc.) using this kind of stimuli. The method for sine-wave signal generation proposed in this paper based on the switched-capacitor technique with performance of 81 dB at 41 MHz while occupying only 0.17 mm^2 is currently the best reported. Additionally, it has the attributes of control capability, robustness and low area overhead, which make it suitable for a whole range of BIST applications.

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Table 1. Variable Gain Amplifier Performance Summary and Comparison

Features	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[This work]
Bandwidth [MHz]	20	125	3	15	2.5	12.5	33	40
Tech. [CMOS]	0.18µm	0.35µm	0.13µm	0.8µm	0.35µm	0.5µm	0.35µm	0.065µm
Supply [V]	1.8	3.3	2.5	5	2.5	3	2.8	1.2
Power [mW]	2.43	21	16	25	11.25	173	40	11
Gain Range [dB]	-10 to 20	0 to 19	-10 to 36	-2 to 12	0 to 60	0 to 32	0 to 18	-10 to 60
IRN [nV/sqrtHz]	11.2	8.6	4.2	20	1.64	4	---	12

Table 2. On-Chip Signal Generator Performance Summary and Comparison

Features	Continous-Time Oscillator[9]	Analog ΣΔ Oscillator [10]	ROM based Generator[11]	Integrator based [14]	[This work]
Technology	0.8µm CMOS	FPGA+6^{th} order filter	0.8µm BiCMOS	0.35µm CMOS	0.065µm CMOS
Area [mm^2]	0.63	---	0.83 + 4^{th} order filter	0.1	0.17
THD [dB]	44dB @ 25MHz	84dB @ 5kHz	---	67dB @ 41MHz	81dB @ 41MHz
SFDR [dB]	49dB @25MHz	86dB @ 5kHz	65dB @ 10 MHz	67dB @ 41MHz	84 dB @ 41MHz