Crosstalk-Aware Statistical Interconnect Delay Calculation

Qin Tang, Amir Zjajo, Michel Berkelaar and Nick van der Meijs
*Circuits and Systems, Delft University of Technology
e-mail: q.tang@tudelft.nl

Abstract— As the device geometries are shrinking, the impact of crosstalk effects increases, which results in a stronger dependence of interconnect delay on the input arrival time difference between victim and aggressor inputs (input skew). The increasing process variations lead to statistical input skew which induces significant interconnect delay variations. Therefore, it is necessary to take input skew variation into account for interconnect delay calculation in the presence of process variations. Existing timing analysis tools evaluate gate and interconnect delays separately. In this paper, we focus on statistical interconnect delay calculation considering crosstalk effects. A piecewise linear delay-change-curve model enables closed-form analytical evaluation of the statistical interconnect delay caused by input skew (SK) variations. This method can handle arbitrarily distributed SK variations. The process-variation (PV)-induced interconnect delay variation is handled in a quadratic delay model which considers coupling effects. The SK- and PV-induced interconnect delay variations are combined together for crosstalk-aware statistical interconnect delay calculation. The experimental results indicate that the proposed method can predict the interconnect delay impacted by both input skew variation and process variations with average (maximum) absolute mean error 0.25% (0.75%) and standard deviation error 1.31% (3.53%) for different types of coupled wires in a 65nm technology.

I. Introduction

Gate delays have been considerably reduced thanks to the scaling of device dimensions. However, interconnect delay has reduced less compared to gate delay [1], becoming a dominant component of circuit delay for modern nanometer technologies. Interconnect delay is affected by the variations of critical process parameters (process variations) in a complex way and the ratio of process variations with respect to their corresponding nominal values is increasing. Therefore, the impact of process variations (PVs) on interconnect delay must be taken into account for accurate statistical static timing analysis (SSTA). In many SSTA methods, delay is modeled as a function of process variations. Since significant errors occur in linear delay models when process variations are larger than 10% of the nominal values, quadratic delay models have become popular, which are sufficiently accurate for process variations up to 30% [2].

Besides process variations, the effect of crosstalk on delay increases with each new technology generation. The accurate SSTA tools which can include crosstalk effects are required for high-performance circuits. Meanwhile, as the spacing between wires continues to shrink (e. g. typical spacing of intermediate wires is $0.35\mu m$ in a 180nm technology, but $0.14\mu m$ in a 65nm technology [3]), the value of the coupling capacitance starts to dominate the ground capacitance. Crosstalk may increase path delay up to 30%, making it the biggest variation component within a die [4]. Therefore, accurately estimating interconnect delay distribution with crosstalk effects is an absolute necessity for timing analysis.

Due to the crosstalk effects, interconnect delay is strongly sensitive to the arrival time difference between victim and aggressor inputs (input skew). Since process variations cause variability in the arrival time of gate outputs, the input arrival times of victim and aggressor are variable as well. Whether to consider crosstalk is determined by the overlap of victim and aggressor input switching windows. The switching window overlap can be estimated deterministically [5, 6] or using statistical switching windows [7]. If the input switching windows do not overlap, only process variations need to be considered. Otherwise, both input skew variation and process variations must be taken into account together.

The delay-change characteristics of coupled interconnects due to input skew variations are addressed in [1, 8] without considering process variations of wires. In contrast, the delay variation of coupled interconnects resulting from process variations is represented in [9] by a first-order closed-form expression, assuming independent random variables and a deterministic ramp input model. However, the signals are stochastic in SSTA, which can not be simply modeled by a ramp. How to include statistical input arrival times in [9] is unclear. Both random input skew variation and process variations are considered in [10, 11]. The interconnect delay is modeled as a piecewise quadratic delay-change curve (DCC) of input skew, and the probability density function (pdf) of the victim output arrival time is calculated using a closed form. The method requires Gaussian-distributed input arrival time but mostly generates non-Gaussian output arrival time which is the input for the next stage. How to obtain arrival time propagation and how to consider input skew for PV-induced interconnect delay are not explicitly explained. Our experiments show that a piecewise linear DCC is accurate enough for interconnect wires at 65nm node. Also, arrival times are not necessarily Gaussian distributed.

In this paper, a piecewise linear DCC for random input skew (SK)-induced interconnect delay is proposed. Based on the linear DCC, SK-induced delay moments are analytically calculated, enabling the handling of arbitrarily distributed random variations. To apply the method to existing SSTA tools, a worst/best delay calculation technique from statistical input skew windows is presented in this paper. Furthermore, we

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model the PV-induced interconnect delay as a quadratic delay model with respect to process variations considering the dependence on input skew. According to our experiments, for long wires (e.g. the $500\mu m$ global wires), the standard deviation of PV-induced interconnect delay depends on input skew weakly. As a consequence, the PV-induced delay can be calculated without coupling effect by setting input skew far away from 0. However, for shorter (and more common) interconnects in 65nm technology and below (e.g. local and intermediate wires), excluding coupling effects would result in delay standard deviation errors up to 80%. Additionally, the interconnect delay variation due to crosstalk is propagated without changing the delay model format in our method.

The rest of the paper is organized as follows. In Section II, we describe the problem we need to solve. In Section III, we present a method to compute delay moments caused by input skew variation based on a piecewise linear DCC, which is valid for arbitrarily distributed input skew. Using the method for worst/best delay calculation from input skew windows is also explained in this section. In Section IV, we demonstrate that the dependence of process-variation-induced interconnect delay distribution on input skew must be taken into account. In Section V, we show the high accuracy of our method using experimental results. In Section VI, we present the conclusion.

II. Problem description

The interconnect delay distribution in the presence of crosstalk effects in SSTA depends on many factors, such as arrival time difference and slew-time difference between the victim and aggressors. Additionally, an aggressor couples noise to a victim wire when its transition is in the crosstalk window $[-0.5T_r, 0.5T_r]$ [12], where T_r is the input transition time. Since input skew influences interconnect delay significantly, in this work, we model the variation sources in input skew in addition to the process variations (PV). Fig. 1 illustrates the crosstalk effects in the coupled wires. If the victim and aggressor inputs switch in the same direction, coupling effects can speedup the victim transition and reduce the interconnect delay of the victim wire, which changes the best-case delay. On the other hand, if victim and aggressor inputs switch in an opposite direction, victim transitions slow down thus affecting the worst-case victim delay[1]. Together with PVs in wires, the statistical interconnect delay calculation becomes more complex. Therefore, we define the **PROBLEM**: *How to calculate the delay of a coupled interconnect system in the presence of both input skew variation and process variations?*

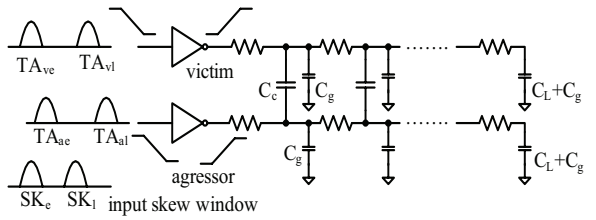

Fig. 1. Statistical interconnect delay calculation with crosstalk effects: calculate interconnect delay distribution given input switching window of victim and aggressors and process variations of wires.

[1]Since RLC interconnect is a linear system, a system of multiple aggressors can be analyzed by superposition for efficient timing and noise analysis [9]. This is also an accepted approximation in the case of nonlinear driver model. Therefore, we illustrate two coupled interconnects in this paper.

The following definitions will be used in this paper:

- s, μ_s, σ_s^2. input skew, mean and variance of input skew variation respectively.
- D_0, nominal delay, the interconnect delay calculated by setting input skew and process parameters to their mean values.
- delay variation, the difference between real delay and nominal delay D_0 .
- μ_{sk} and σ_{sk}^2, the mean and variance of random *input-skew-induced (SK-induced) interconnect delay* when each process parameter has its mean value.
- $\mu_{pv}(\mu_s)$ and $\sigma_{pv}^2(\mu_s)$, the mean and variance of *process-variation-induced (PV-induced) interconnect delay* when input skew has its mean value μ_s.
- μ_{total} and σ_{total}^2, the mean and variance of delay in the presence of both process and input skew variations.

According to [1, 10, 11], the process variations of wires and input skew can be considered independent without much loss of accuracy. Therefore, better efficiency can be achieved for delay calculation by superposition:

$$\mu_{total} = \mu_{sk} + \mu_{pv}(\mu_s) - D_0 \quad (1)$$

$$\sigma_{total}^2 = \sigma_{sk}^2 + \sigma_{pv}^2(\mu_s) \quad (2)$$

Based on (1)-(2), the **PROBLEM** is split into two parts: **PROBLEM 1.1**: *How to calculate the delay distribution caused by input skew variation only? (e.g. μ_{sk} and σ_{sk}^2)* and **PROBLEM 1.2**: *How to calculate the delay distribution caused by process variations only, considering coupling effects? (e.g. $\mu_{pv}(\mu_s)$ and $\sigma_{pv}^2(\mu_s)$).* According to our experiments, although the $\mu_{pv}(\mu_s)$ and $\sigma_{pv}^2(\mu_s)$ can be calculated without coupling effects for global wires to get higher efficiency, the dependence of PV-induced delay on input skew must be considered for local and intermediate wires in 65nm technology and below. The delay variations caused by crosstalk are lumped as a local variable χ in interconnect delay for propagation with mean $\mu_\chi = \mu_{total} - D_0$ and variance $\sigma_\chi^2 = \sigma_{total}^2$. Special cases are presented in Section III-A.

Whether to consider the crosstalk effects is determined by input switching window overlap. In SSTA, often the input arrival time information is not a single distribution but the earliest and latest arrival time distributions. Switching window overlap can be estimated deterministically or statistically and more accurate timing windows can be obtained using iterations [6, 7]. In this work, we emphasize accurate statistical interconnect delay calculation within a single iteration of the delay calculation.

III. Input-skew-induced delay

A. Delay calculation with input skew variation

Due to process variations, the arrival time at every node is statistical with some distribution. Arrival time and delay are

modeled using linear or quadratic models in many SSTA methods. Since input skew is calculated by subtracting aggressor arrival time from victim arrival time, input skew is also expressed as a linear or quadratic function of the process variations. Global variations are generally assumed as Gaussian distributed and independent [13]. Local variations are often managed by principal component analysis (PCA)-like methods and converted to a (smaller) number of uncorrelated normal distributed variables. Therefore, input skew is Gaussian distributed in linear SSTA, but non-Gaussian in quadratic SSTA. However, even though the skew is a quadratic model of process variations, its probability density function (*pdf*) and cumulative distribution function (*cdf*) can be directly calculated by using a characteristic function [2].

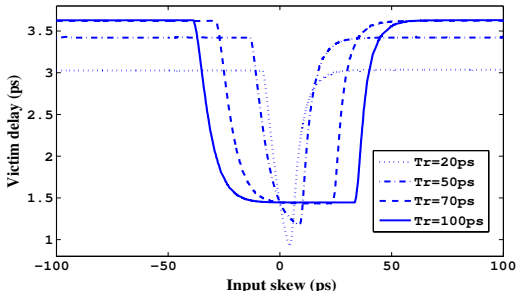

Fig. 2. Delay change curve (DCC) of a pair of $200\mu m$ coupled intermediate interconnects in PTM 65nm technology. Linear driver model with 50Ω driver resistance is used. The load capacitance (C_L in Fig. 1) of each wire is $3fF$.

Fig. 2 shows the dependence of the victim delay on the input skew of a pair of coupled $200\mu m$ intermediate wires. It is simulated in SPICE for different input transition times (T_r) of both inputs using the 65nm technology given by predictive technology model (PTM) [3]. It is clear that the interconnect delay decreases when the coupling effect occurs if two input signals switch in the same direction, and the coupling effects are apparent when the input skew is within approximately $[-0.6T_r, 0.6T_r]$. Additionally, the DCC appears closer to a piecewise linear function.

Based on the observations mentioned above, we compute the interconnect delay for different input skews. In contrast to [10, 11], we approximate it as a piecewise linear function of input skew as shown in Fig. 3(a) and formulated as follows:

$$D_{sk}(s) = \begin{cases} D_a & s \le s_0 \quad || \quad s \ge s_3 \\ a_0 s + a_1 & s_0 \le s \le s_1 \\ D_b & s_1 \le s \le s_2 \\ b_0 s + b_1 & s_2 \le s \le s_3 \end{cases} \tag{3}$$

where a_0, a_1, b_0 and b_1 are determined by D_a, D_b and break points $s_0 \sim s_3$ which can be derived easily. Based on this piecewise linear DCC, the mean (μ_{sk}) and variance (σ^2_{sk}) of the input-skew-induced interconnect delay[2] can be calculated as follows.

$$\begin{aligned} \mu_{sk} = & E\{D_{sk}(s)\} \\ = & \int_{-\infty}^{+\infty} D_{sk}(s) f_s(s) ds \\ = & \int_{-\infty}^{s_0} D_a f_s(s) ds \\ & + \int_{s_0}^{s_1} (a_0 + a_1 s) f_s(s) ds + \int_{s_1}^{s_2} D_b f_s(s) ds \\ & + \int_{s_2}^{s_3} (b_0 + b_1 s) f_s(s) ds + \int_{s_3}^{+\infty} D_a f_s(s) ds \\ = & (D_a - a_0) F_s(s_0) + (a_0 - D_b) F_s(s_1) \\ & + (D_b - b_0) F_s(s_2) + (b_0 - D_a) F_s(s_3) \\ & + D_a + a_1 G(s_0, s_1, f_s) + b_1 G(s_2, s_3, f_s) \end{aligned} \tag{4}$$

$$\begin{aligned} \sigma^2_{sk} = & E\{D^2_{sk}(s)\} - (E\{D_{sk}(s)\})^2 \\ = & \int_{-\infty}^{+\infty} D^2_{sk}(s) f_s(s) ds - \mu^2_{sk} \\ = & \int_{-\infty}^{s_0} D_a^2 f_s(s) ds + \int_{s_0}^{s_1} (a_0 + a_1 s)^2 f_s(s) ds \\ & + \int_{s_1}^{s_2} D_b^2 f_s(s) ds + \int_{s_2}^{s_3} (b_0 + b_1 s)^2 f_s(s) ds \\ & + \int_{s_3}^{+\infty} D_a^2 f_s(s) ds - \mu^2_{sk} \\ = & (D_a^2 - a_0^2) F_s(s_0) + (a_0^2 - D_b^2) F_s(s_1) \\ & + (D_b^2 - b_0^2) F_s(s_2) + (b_0^2 - D_a^2) F_s(s_3) + D_a^2 \\ & + 2a_0 a_1 G(s_0, s_1, f_s) + 2b_0 b_1 G(s_2, s_3, f_s) \\ & + a_1^2 H(s_0, s_1, f_s) + b_1^2 H(s_2, s_3, f_s) - \mu^2_{sk} \end{aligned} \tag{5}$$

where $F_s(\cdot)$ and $f_s(\cdot)$ are the *cdf* and *pdf* of input skew variation respectively. $G(x_0, x_1, f_s) = \int_{x_0}^{x_1} s f_s(s) ds$ and $H(x_0, x_1, f_s) = \int_{x_0}^{x_1} s^2 f_s(s) ds$, where x_0 and x_1 are symbols for parameters in the functions.

If the input skew distribution is non-Gaussian, G and H can be calculated by numerical integration given its *pdf* and *cdf* by using just a few samples to keep it efficient. On the other hand, if the input skew distribution is approximated as a mathematical distribution, such as Gaussian or uniform distribution, μ_{sk} and σ^2_{sk} can be computed analytically in closed form. In the case of Gaussian distribution, the following closed-form expressions (6)-(10) are substituted into (4)-(5).

$$\begin{aligned} G(x_0, x_1, f) = & \frac{\sigma}{\sqrt{2\pi}} \left(e^{-z_0^2/2} - e^{-z_1^2/2} \right) \\ & + \mu \left(\Phi(z_1) - \Phi(z_0) \right) \end{aligned} \tag{6}$$

$$\begin{aligned} H(x_0, x_1, f) = & \frac{\sigma^2}{\sqrt{2\pi}} \left(z_0 e^{-z_0^2/2} - z_1 e^{-z_1^2/2} \right) \\ & + (\mu^2 + \sigma^2) \left(\Phi(z_1) - \Phi(z_0) \right) \\ & + \frac{2\mu\sigma}{\sqrt{2\pi}} \left(e^{-z_0^2/2} - e^{-z_1^2/2} \right) \end{aligned} \tag{7}$$

$$z_0 = (x_0 - \mu)/\sigma \quad and \quad z_1 = (x_1 - \mu)/\sigma \tag{8}$$

$$F_s(s) = \frac{1}{2} \left[1 + erf \left(\frac{s - \mu_s}{\sqrt{2\sigma_s^2}} \right) \right] \tag{9}$$

$$f_s(s) = \frac{1}{\sqrt{2\pi\sigma_s^2}} e^{-\frac{(s-\mu_s)^2}{2\sigma_s^2}} \tag{10}$$

where $\Phi(x) = \frac{1}{2} \left[1 + erf \left(\frac{x}{\sqrt{2}} \right) \right]$ is the *cdf* of the standard normal distribution. Therefore, the mean and variance of the interconnect delay can be calculated through closed-form expressions in constant time.

A special case for SK-induced delay calculation and propagation occurs when the truncated input skew distribution is fully within $[s_0, s_1]$(or $[s_2, s_3]$), since we can express the delay as $a_0(TA_v - TA_a) + a_1$ (or $b_0(TA_v - TA_a) + b_1$). TA_v and TA_a are the victim and aggressor input arrival time distributions used to calculate the input skew distribution. In contrast to the quadratic model in [10, 11], the linear combination of input arrival times of victim and aggressor leads to

[2]Better accuracy can be obtained by more segments in the linear DCC if necessary, but the moment calculation is similar to (4) -(5).

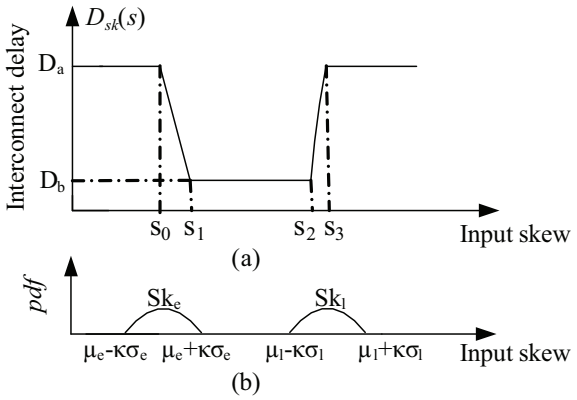

Fig. 3. (a) Delay change curve (DCC) model for SK-induced interconnect delay; (b) Input skew window.

the same model format for interconnect delay and input arrival times. This maintains the correlations between victim and aggressor inputs for accurate delay distribution calculation. For instance, if TA_v and TA_a have the same quadratic models like (11) with coefficients TA_{v0}, β_v, Γ_v and TA_{a0}, β_a, Γ_a respectively, $D_{sk} = D_{sk0} + \beta_{sk}\xi + \xi^T\Gamma_{sk}\xi$, where $D_{sk0} = a_0(TA_{v0} - TA_{a0}) + a_1$, $\beta_{sk} = a_0(\beta_v - \beta_a)$ and $\Gamma_{sk} = a_0(\Gamma_v - \Gamma_a)$. For this special case, SK-induced delay distribution can be calculated directly similar to (12)$\sim$(13).

The characterization of DCC takes $O(N)$ time, where N is the the number of sample points. In our implementation, $15 \sim 25$ points are selected within $[-1.5T_r, 1.5T_r]$ ($3 \sim 4$ points for $[-1.5T_r, -T_r]$, $[0, 0.1T_r]$ and $[T_r, 1.5T_r]$ respectively. The remaining points are assigned to $[-0.7T_r, -0.3T_r]$ and $[0.3T_r, 0.7T_r]$). Based on the DCC, SK-induced delay distribution can be calculated within a constant time using the closed-form formulas.

B. Delay calculation from input skew window

Given the earliest and latest arrival time distribution of victim and aggressor inputs (TA_{ve}, TA_{vl} and TA_{ae}, TA_{al} in Fig. 1), the earliest and latest input skew distributions (SK_e and SK_l in Fig. 1 and Fig. 3(b)) can be computed by subtracting TA_{ae} and TA_{al} from TA_{vl} (worst-case delay) or TA_{ve} (best-case delay) [1]. SK_e and SK_l are truncated within $[\mu_e - \kappa\sigma_e, \mu_e + \kappa\sigma_e]$ and $[\mu_l - \kappa\sigma_l, \mu_l + \kappa\sigma_l]$ respectively, where $\kappa = 3 \sim 6$.

After obtaining the input skew window, we need to calculate the worst/best SK-induced delay from it. As shown in Fig. 3, coupling effects do not occur if $\mu_l + \kappa\sigma_l \leq s_0$ or $\mu_e - \kappa\sigma_e \geq s_3$. In this situation, the SK-induced delay calculation can be skipped since worst/best delay is D_a. Other conditions can be divided into the following three types: i) $\mu_l + \kappa\sigma_l \geq s_0 \cap \mu_l - \kappa\sigma_l \leq s_1$. Since DCC is constant or decreasing along with s, SK_l determines the best delay (or worst delay if input switch in opposite directions). Therefore, SK_l is used for SK-induced delay calculation; ii) $\mu_e + \kappa\sigma_e \geq s_2 \cap \mu_e - \kappa\sigma_e \leq s_3$. DCC is an increasing function of s thus SK_e is used for delay calculation; iii) $\mu_l - \kappa\sigma_l \geq s_1$ or $\mu_e + \kappa\sigma_e \leq s_2$. The best/worst SK-induced delay is D_b. If SK_e and SK_l are overlapping, their statistical maximum or minimum is computed for i and ii situations respectively.

IV. Process-variation-induced delay

PV-induced delay distribution refers to the interconnect delay distribution under process variations with input skew at its mean value. Fig. 4 shows that the μ and σ of interconnect delay with width and thickness variations vary with the input skew. This effect should therefore be modeled for crosstalk-aware statistical delay calculation. For global wires, the σ change with respect to input skew is within 3% so the PV-induced delay can be calculated ignoring crosstalk effects (s is far away from 0). However, for local and intermediate interconnects, the delay σ change would be up to 80% which is clearly not negligible.

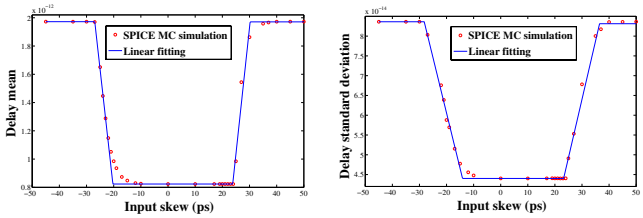

Fig. 4. The mean (left) and standard deviation (right) of a pair of coupled $200\mu m$ intermediate wires with width and thickness variations along with input skew change. Circles are results from SPICE Monte Carlo simulations.

In our implementation, after RC extraction, we model victim delay as a quadratic function of process variations at two conditions: without coupling effects ($s = 1.5T_r$) and with strong coupling effects ($s = 0$). The quadratic models are characterized by matching the first two moments, which achieves a maximum error of 0.02% and 0.64% for μ and σ of interconnect delay, respectively, for a $200\mu m$ intermediate wire in PTM 65nm technology. Based on the quadratic model, the delay can be expressed as (11) and its mean (μ_D) and variance (σ_D^2) can be calculated for arbitrarily-distributed process variations by using (12)-(13) under each condition.

$$D = D_0 + \beta^T\xi + \xi^T\Gamma\xi \tag{11}$$

$$\mu_D = D_0 + \sum_{i=1}^{n}\Gamma_{ii}\sigma_i^2 \tag{12}$$

$$\sigma_D^2 = \sum_{i=1}^{n}\left(\beta_i^2\sigma_i^2 + 2\beta_i\Gamma_{ii}m_{3,i} + \Gamma_{ii}^2 m_{4,i}\right) - \left(\sum_{i=1}^{n}\Gamma_{ii}\sigma_i^2\right)^2 + 2\sum_{i=1}^{n}\sum_{1\leq j\leq i\leq n}\sigma_i^2\sigma_j^2\left(\Gamma_{ii}\Gamma_{jj} + \Gamma_{ij}^2\right) \tag{13}$$

where ξ denotes the process variation vector and σ_i^2 is the variance of the i_{th} process variation (ξ_i). $m_{3,i}$ and $m_{4,i}$ are the third and forth moments of ξ_i. β and Γ are the first- and second-order sensitivities of delay with respect to ξ respectively.

When considering coupled interconnects as a black-box, delay calculation in the presence of crosstalk is similar to taking into account multiple input switching for gate delay calculation. An empirical model is used in [14] to predict the gate delay σ as a weighted sum of the σs of arrival times of multiple inputs. According to Fig. 4, the μ and σ of crosstalk-impacted interconnect delay can be fitted by a piecewise linear function. Exact break points are more accurate but takes long characterization time. According to our experiments, the break points are approximately a linear function of the input transition time,

which leads to more efficient characterization and calculation. Other methods, which calculates interconnect delay with relevant process variations considering crosstalk noise [9, 15], can also be used for PV-induced delay calculation with coupling effects.

In this paper, we show that *even though the influence of input skew and process variations on interconnect delay can be considered independent, the PV-induced interconnect delay calculation must take input skew (μ_s) into account in nanometer technologies*. More data for this are in σ_c errors in Table III.

V. Experimental Results

We evaluated our method on some typical coupled interconnect structures in PTM 65nm technology [3], which are listed in Table I. Geometries (length L, width W, spacing S, and thickness T) and RC parameters (total resistance R_w, total ground capacitance C_g, and total coupling capacitance C_c) are obtained from PTM with inter-layer dielectric (ILD) height $H_{ILD} = 0.20\mu m$ and $k_{ILD} = 2.2$. The local and intermediate (inter.) wires have a C_c which is approximately twice as large as C_g while global wires have an almost inverse C_c/C_g ratio. Therefore, local and intermediate wires have stronger coupling effects. The coupled $\pi \sim \pi 3$ models are used for interconencts in the Table I. The load capacitance (C_L+C_g in Fig. 1) is $3fF$ in wL, wI1 and wI2, and $10fF$ in wI5 and wG. The transition times (T_r) of victim and aggressor inputs vary from $10ps$ to $100ps$.

TABLE I
The typical coupled interconnect structures for experiments

65nm (Name// Type//model)	L	W	S	T	R_w	C_c	C_g
	μm				Ω	fF	
wL//Local//π	30	0.10	0.10	0.20	33.00	3.22	1.17
wI1//Inter.//π2	100	0.14	0.14	0.35	44.90	11.53	5.38
wI2//Inter.//π3	200	0.14	0.14	0.35	89.80	23.06	10.76
wI5//Inter.//π3	500	0.14	0.14	0.35	224.49	57.65	26.89
wG//Global//π3	500	0.45	0.45	1.20	20.37	33.00	69.98

The input-skew- (SK)-induced interconnect delay calculation method (Section III) was evaluated in all wires in Table I. The delay mean and standard deviation results of coupled wires wI2 with Gaussian-distributed and Uniform-distributed input skew variations can be found in Table II. The transition time of input signals is $50ps$. The Gaussian-distributed SK variation has $3\sigma_s = 20.4ps$ while the *pdf* of Uniform-distributed SK has value within $[\mu_s - 10ps, \mu_s + 10ps]$. Table II shows that the absolute difference between the results by using our linear-DCC(LDCC)-based method and from 2000 SPICE Monte Carlo (MC) simulations is quite small [3]. It should be noted that, when $\mu_s = 0$, the SPICE MC simulation does not converge even when the number of MC samples is 70,000 for Gaussian SK distribution (the delay σ_{sk} increases when the number of MC samples are 10k, 20k, 50k, 70k and 100k). This is caused by the small probability of samples being taken outside the $[s_1, s_2]$ range, but those values significantly contribute to the variance of interconnect delay. Therefore, using an analytical method is sometimes more reliable than MC simulations if the DCC is accurate enough. Table II shows that our method is able to accurately estimate SK-induced interconnect delay for both Gaussian- and non-Gaussian-distributed input skew variations.

[3] 100k SPICE MC is used for $\mu_s = 0$ of Gaussian-distributed input skew in Table II

TABLE II
SK-induced delay calculation with different input skew mean value μ_s for Gaussian- and Uniform-distributed SK variations

μ_s (ps)	$\mu_{sk}(ps)$ SPICE	$\mu_{sk}(ps)$ LDCC	$\sigma_{sk}(0.1ps)$ SPICE	$\sigma_{sk}(0.1ps)$ LDCC	%error of μ_{sk}	%error of σ_{sk}
Gaussian-distributed input skew variation						
-20	1.20	1.19	4.32	4.37	0.83%	-1.22%
-10	0.87	0.86	1.55	1.52	1.15%	1.74%
0	0.82	0.82	0.18	0.19	0.16%	-5.54%
10	0.83	0.83	0.79	0.82	-0.13%	-3.35%
20	1.01	1.01	3.66	3.64	-0.52%	0.61%
Uniform-distributed input skew variation						
-20	1.21	1.20	4.42	4.43	0.83%	-0.28%
0	0.82	0.82	0.00	0.00	0.06%	0%
20	1.00	1.00	3.40	3.32	0.28%	2.35%

The wire width and thickness are chosen as the source of process variations in wires. We use the capacitance and resistance model formulated in PTM [3] for SPICE MC simulations. Different wire types use different distributed RC model based on interconnect length. Fig. 5 shows the probability density function (*pdf*) comparison between our quadratic PV-induced delay model characterized based on statistical moment matching and 5k SPICE MC simulations for different width and thickness variances.

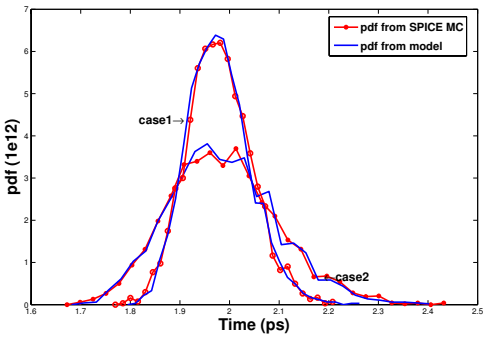

Fig. 5. *pdf* comparison between SPICE 5k MC and the proposed method for wI2 wires with different width variation ($3\sigma_W/\mu_W$) and thickness variation ($3\sigma_T/\mu_T$). case1: 9% and 18%; case2: 21% and 15%.

The interconnect delay in the presence of both input skew variation and process variations under different input skew means are calculated and compared to 5k SPICE MC results in Table III. The victim/aggressor input arrival time variation is extracted from an INV_X4 gate with transistor length variation $3\sigma_L = 10\%\mu_L$, resulting in the input skew with $3\sigma_s = 20.4ps$. We use a $3\sigma/\mu$ variability of 15% for both the width and thickness variations. In our method, we first use the methods proposed in Section III and IV to calculate the SK-induced and PV-induced delay distribution respectively, then the final delay distribution is computed based on (1)-(2). In Table III, $\mu(\%)$ and $\sigma(\%)$ are the %error of the delay mean and standard deviation of the proposed method compared to the SPICE MC simulations. $\sigma\_c(\%)$ is the delay standard deviation error by

TABLE III
%ERROR OF INTERCONNECT DELAY CALCULATION IN THE PRESENCE OF BOTH RANDOM INPUT SKEW AND PROCESS VARIATIONS

Name	wL ($T_r = 10ps$)			wI1 ($T_r = 20ps$)			wI2 ($T_r = 50ps$)			wI5 ($T_r = 50ps$)			wG($T_r = 100ps$)		
$\mu_s(ps)$	$\mu(\%)$	$\sigma(\%)$	σ_c (%)	$\mu(\%)$	$\sigma(\%)$	$\sigma\_c(\%)$	$\mu(\%)$	$\sigma(\%)$	$\sigma\_c(\%)$	$\mu(\%)$	$\sigma(\%)$	$\sigma\_c(\%)$	$\mu(\%)$	$\sigma(\%)$	$\sigma\_c(\%)$
-50	0.08	-1.81	-1.81	0.10	-2.39	-2.39	0.10	-2.37	-2.37	-0.75	-0.39	-0.39	-0.22	0.26	0.26
-10	-0.20	1.20	1.20	0.58	0.36	0.65	-0.38	-3.53	5.48	0.31	-1.68	20.75	0.09	-0.59	2.42
0	0.15	-1.42	-0.07	-0.57	-2.65	-1.01	0.13	-2.06	80.04	0.13	-1.49	36.68	0.09	-0.57	2.43
10	0.25	-0.62	-0.62	-0.70	-0.47	0.31	0.01	-0.19	24.06	-0.39	-1.82	49.28	0.09	-0.56	2.43
50	0.09	-1.84	-1.84	0.09	-2.43	-2.43	0.11	-1.45	-1.45	0.44	-0.49	2.74	0.30	0.19	0.31

using $\sigma^2\_c = \sigma^2_{sk}(MC) + \sigma^2_{pv}(1.5T_r)$, where $\sigma^2_{sk}(MC)$ is the SK-induced delay variance from SPICE MC simulations and $\sigma^2_{pv}(1.5T_r)$ is the PV-induced delay calculation without considering coupling effect by setting $s = 1.5T_r$.

We can observe that σ_c is slightly smaller than σ for wL and wI1 when $s = 0$. The reason is that the delay variances of wL and wI1 are dominated by SK-induced delay variances σ^2_{sk}. Therefore, *for short wires, accurate calculation for SK-induced delay distribution is critical for crosstalk-aware statistical interconnect delay calculation*. For medium-sized wires wI2 and wI5, the σ_c error is up to 80.04% which is unacceptable for modern SSTA tools (the nominal delay of wI2 and wI5 are $2.0ps$ and $10.1ps$ when μ_s=-50ps respectively). Thus *PV-induced delay distribution calculation should include coupling effects*. However, for global wire wG, as we mentioned in Section I, ignoring input skew for PV-induced delay calculation results in a delay σ error within 3%. The average (maximum) absolute μ and σ errors of interconnect delay calculation by using the proposed method are 0.25% (0.75%) and 1.31% (3.53%) respectively. For global wires, the proposed method achieves maximum errors of 0.22% and 0.59% for delay mean and standard deviation. Table III demonstrates that the method proposed in this paper can estimate crosstalk-aware statistical delay accurately, not only for local and intermediate wires but also for global wires. The results of wI2 driven by a weak driver (driver resistance is approximately 1500Ω) also indicate the high accuracy of our method. The delay μ error and σ error are -0.02% and 0.40% when μ_s=$-10p$, and 0.28% and -1.76% when μ_s=200ps respectively by using seven-segment DCC (two more segments than five-segment DCC in (3)).

The importance of considering crosstalk effects is checked by grounding coupling capacitors and using the same parameter settings as in Table III. *Experimental results show that without considering crosstalk effects for coupled interconnects affected by input skew variation and process variations causes up to* 139% *delay mean error and* 83% *delay standard deviation error in PTM 65nm technology*.

VI. CONCLUSION

Crosstalk-aware statistical interconnect delay calculation is significant for accurate SSTA tools. In this paper, interconnect delay is modeled as a piecewise linear delay change curve (DCC), based on which an analytical method is proposed to calculate the mean and variance of random input skew (SK)-induced interconnect delay. The analytical method is able to handle both Gaussian and non-Gaussian input skew distributions. Quadratic interconnect delay model is used to consider process variations (PV). The dependence of PV-induced delay mean and standard deviation on input skew is considered for delay calculation. The total interconnect delay distribution with both input skew variation and process variations is computed from SK-induced and PV-induced delays based on an independence assumption. Compared with SPICE Monte Carlo simulations, the proposed method can accurately estimate the statistical interconnect delay moments considering crosstalk effects for different interconnect structures.

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