Stimulus generation for RF MEMS switches test application

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Abstract: The sinewave generators based the switched-capacitor (SC) technologies are implemented in transistor level. This analogue sinewave generator consists of two parts: an approximate sinewave generator and a filter. The structure of this generator is robust and easily-controlled, in which an approximate sinewave is firstly generated based on SC circuits and then filter the harmonics. The main advantages of the approach are that both the amplitude and the frequency of the signal can be controlled by a DC input voltage and the clock frequency respectively. The amplitude of the sinewave is 400 mV with SNR of 42.2 dB at a supply voltage of 1.2 V. The settling time of the system is less than 0.5 u and the power is less than 5 mW.

Keywords: switched-capacitor circuit; built-in-self-test; stimulus generation.

Reference to this paper should be made as follows: Song, M., Yin, J., Cao, Z., Wu, T., Zhao, Y., Jin, Z. and Zjajo, A. 'Stimulus generation for RF MEMS switches test application', *Int. J. Simulation and Process Modelling*, Vol.7, No. 1/2, pp.107–114.

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This paper is a revised and expanded version of a paper entitled ‘Design of stimulus generation for RF MEMS testing’ presented at the 2012 International Conference on Information, Computing and Telecommunications (ICICT 2012), Harbin, China, 9–10 January 2012.

1 Introduction

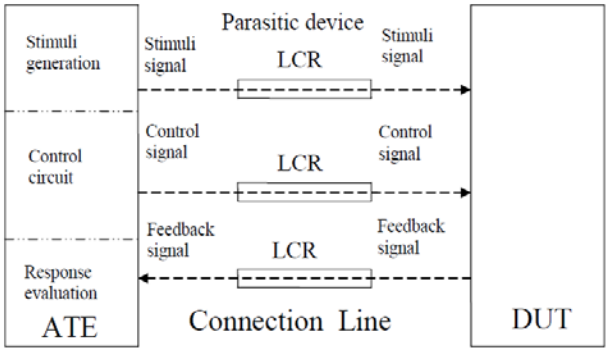
With the rapid development of CMOS technology, the function of a chip has becoming more and more complex. The transistors’ number and the frequency of integrate circuit (IC) develop as predicted by Moore’s law. It means conventional methods of testing become more and more difficult. As IC densities and operating speeds have continued to climb, proving Moore’s law again and again, the testing of a chip, especially analogue/mixed-signal (AMS) IC has became very difficult and very expensive. So it becomes the main bottleneck.

For AMS circuit, built-in self-test (BIST) is a very challenging problem compared to pure digital circuit. Many researchers include Barragan et al. (2006) and Roberts (1999) have paid the attention to them during the last year. A variety of solutions have proposed for analogue and mixed-signal circuit. Conventional sinewave signal generation methods mainly relay on the following three ways. According to Galan et al. (2005), the simple method is based on the analogue oscillator technology. But this structure has a poor precision and is not very power efficient. Both Chang et al. (1994), Dufort and Roberts (1999), Huang and Cheng (2000) and Lu et al. (1994) all focus on using by partly adapting digital techniques, which facilitates a digital interface for control and programming tasks. The method is unfit to generate a high pure sinewave for the area overhead. The third method is the direct digital frequency synthesis (DDS) technique described by Tierney et al. (1971). By which a very fine sine wave can be achieved. But it is not practical due to the area overhead.

For more than a decade, some researchers have endeavoured to perfect the development of microminiature relays using micromachining techniques. With the recent boom in wireless communications, research has intensified in the quest to develop low cost, ultra-low loss switches. Radio frequency Microelectromechanical systems (RF MEMS) switches have been demonstrated that superior RF characteristics can be achieved compared to field effect transistor (FET)-based switches and p-i-n diode-based switches. Now researchers have a lot of difficulty in testing RF MEMS switches.

BIST for AMS circuit is one of development directions of the IC and RF MEMS switches testing technology in the future. BIST circuit normally includes stimuli generation, control circuit and evaluation circuit. Because analogue stimulus generation (especially sinewave generation) has a wide potential applications in the field of mixed-signal testing as most of these systems (filters, ADCs, DACs, signal conditioners, etc.), it has being one of the research hotspot about the BIST technology at present. The methods and structure of sinewave generation have been presented during the past years. Due to the low precision, most of them are limited to use in low dynamic range applications. Some high precision sinewave generation-based DDS, are unfit to BIST application for taking into account the cost of chip area.

Figure 1 Conceptual diagram of the testing with ATE



2 Principle and structure of testing

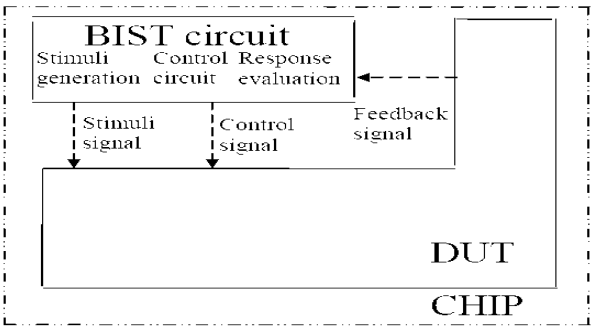
2.1 Principle and structure of ATE

The testing conceptual diagram with ATE is shown in Figure 1. The testing of AMS circuits asks for high accuracy and high speed automatic test equipment (ATE). But the operating frequency of ATEs is normally lower than the operating frequency of the chips. In addition, analogue circuits are normally very sensitive to noise and loading effects that exist connection parasitic capacitances and resistances from device under test (DUT) to ATE. These limitations make ATE unavailable for the high accuracy and high frequency application in AMS circuits testing.

2.2 Principle and structure of BIST

The BIST or built-in test (BIT) technology has been proved to an efficient method for complex chip testing. Because all the testing equipments (including test stimuli generation, response evaluation, test control circuit, etc) are moved from the ATE to the chip as shown as Figure 2, not only the expensive ATE but also the effect of parasitic device between DUT and ATE are eliminated. So it is fit for high frequency testing and makes the testing faster and less-expensive. Obviously, the accuracy of the testing is closely related to the precision of the stimuli signal generated by the stimuli generation. It is very important and necessary to design a low power and high precision stimuli generation for BIST Application in AMS circuits.

Figure 2 Conceptual diagram of the testing with BIST

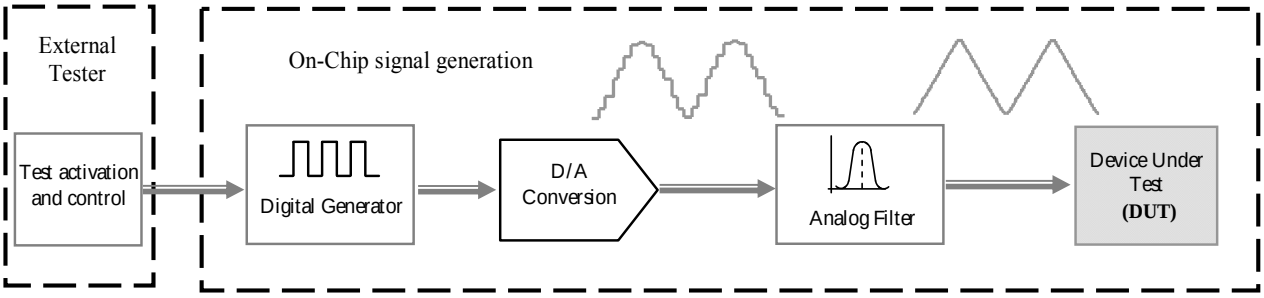


2.3 Principle and structure of digital-based analogue signal generator

A direct implementation using memory-based synthesisers is not practical because of the area overhead.

The works in Chang et al. (1994), Dufort and Roberts (1999), Huang and Cheng (2000) and Lu et al. (1994) avoid the use of the DAC by exploiting the noise shaping characteristics of $\sum\Delta$ encoding schemes. They consist on generating a 1-bit stream $\sum\Delta$ encoded version of an N-bit digital signal and match the shape of a filter with the noise shaping characteristics of the encoded bit stream.

Figure 3 Digital-based analogue signal generator



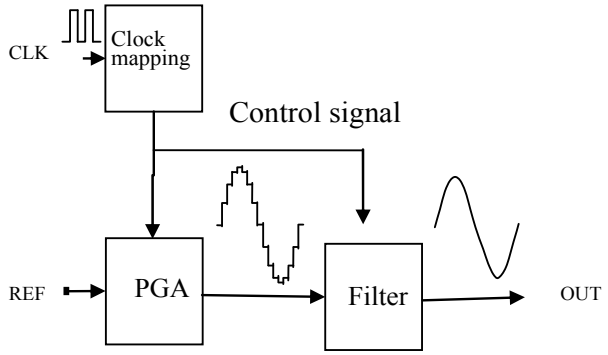
It is valid for single and multitone signals but requires large bit-stream lengths and a highly selective filter to remove the noise. In addition, the approach is frequency limited due to the need of very high oversampling ratios.

2.4 Principle and structure of the proposed signal generator

The block diagram of the proposed system for the on-chip generation is shown in Figure 4, in which the programmable gain amplifier (PGA) plays the role of the DAC of digital-based analogue signal generator in Figure 3.

The analogue sinewave generator shown Figure 4 in consists three parts: a clock mapping block, a programmable multi-gain amplifier (an approximate sinewave generator) and a filter.

Figure 4 Digital-based analogue signal generator



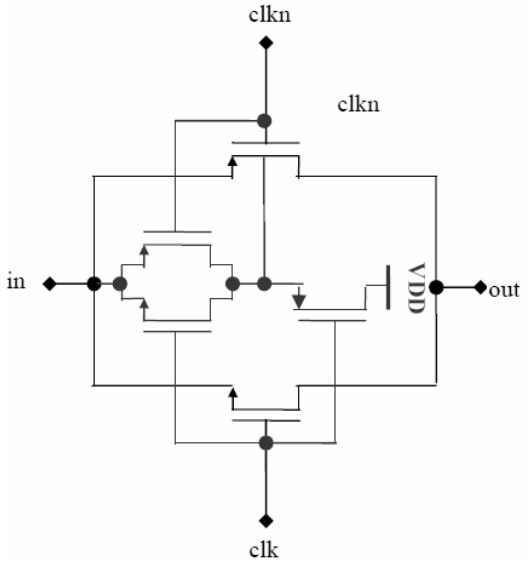
The proposed sinewave generators are based the SC circuit. The structure of the generator is robust and easily-controlled, in which an approximate sinewave is firstly generated based on switched-capacitor (SC) circuits and then filter the harmonics. The main advantages of the approach are that both the amplitude and the frequency of the signal can be controlled by a DC input voltage and the clock frequency respectively.

3 Auxiliary circuits

3.1 The proposed switches

One challenge of SC circuits in the low supply voltage is to drive the floating switch. The conventional structure of CMOS switch, which is called the CMOS transmission gate, is shown as the black part of Figure 5(a). For the low voltage application, a large switch on-resistance (R_{on}) will occur, due to the body effect. The structure of the CMOS switch according to Liu (2006) shown as Figure 5(a) is adopted. When CMOS switch is conducting, the body of the PMOS device is connected to its source [Figure 5(b)]. Because of the absence of body effect, the resistance of the switch is lowered, especially near the middle of voltage range, where the switch resistance is highest. When the switch is off, the body of the PMOS device is connected to the highest voltage present (V_{DD}) to ensure that the drain-to-bulk and source-to-bulk diodes for this device are always reverse biased for any voltage levels between ground and V_{DD} on either side of the switch [Figure 5(c)]. This arrangement lowers the peak resistance of the switch during conduction by about 50% compared to the case where the body of the PMOS transistor is permanently connected to V_{DD}. The reduction in resistance in turn allows a reduction in the size of the switches and their associated parasitic loading on the SC network that employs them. Since the capacitance of the n-well of the main PMOS transistor in the switch to the substate is small, the devices used to switch the body of the main PMOS transistor can be made much smaller (up to 16 times) than the PMOS transistor itself.

Figure 5 The proposed switch, (a) the circuit of the switches (b) switch conducting (c) switch off



(a)

Figure 5 The proposed switch, (a) the circuit of the switches (b) switch conducting (c) switch off (continued)

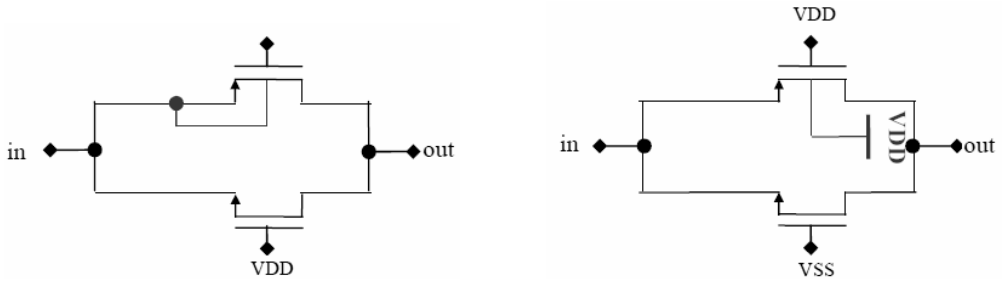
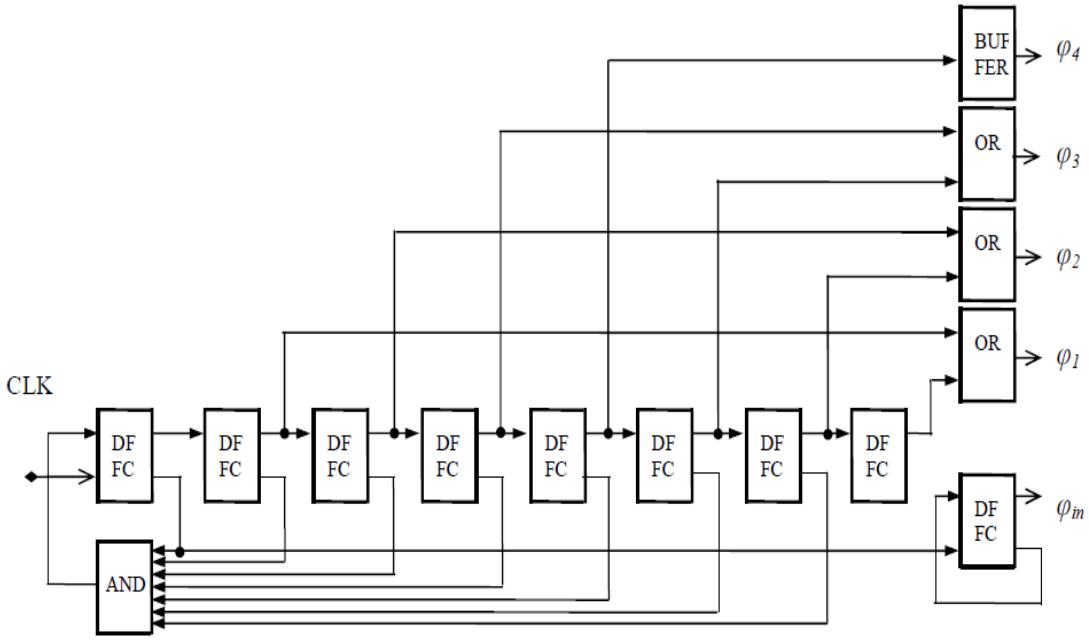


Figure 6 The circuit of the C-Q version



3.2 The clock mapping block

The C-Q architecture discussed in Mendez-Rivera et al. (2003) (Figure 6) has four different gain settings signals, which is applied to the PGA shown in Figure 9. Figure 7 shows the simulated results of the control signals. In any step, capacitor $E_{1...4}$ firstly clear and then absorbs a charge equal to $E_{1...4} \times V_{ref.}$ For the constant V_{ref} value, the output of the amplifier V_{SO} changes by $E_{1...4} \times V_{ref}/B$. The final value of V_{SO} after every step can be written as

$$V_{SO}\left(kT_{clk}\right) = V_{ref}\,\frac{E_{1...4}}{B}$$

In this case, the value of the capacitors $E_{1...4}$ and the capacitor B are 0.383 pF, 0.707 pF, 0.924 pF, 1 pF and 1 pF, respectively.

Figure 7 Timing diagram of the C-Q

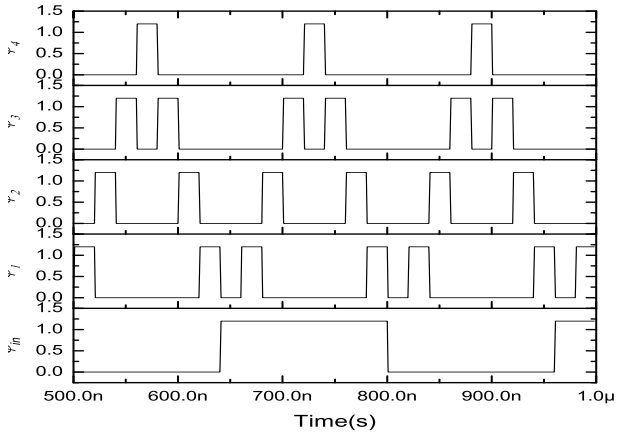
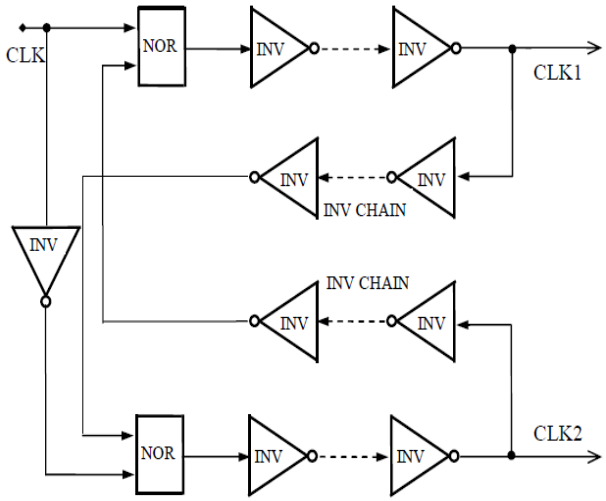


Figure 8 The circuit of the non-overlapping clock generator



3.3 Non-overlapping clock generator

A two-phase-clock generator (Figure 8) generates a first clock and a non-overlapping second clock. The non-overlap time can be adjusted by changing the length of the INV chains.

4 The approximate sinewave generator

Figure 9 illustrates the circuit of C-Q version of the generator. In this case, the value of the capacitors $E_{1..4}$ and the capacitor B are 0.383 pF, 0.707 pF, 0.924 pF, 1 pF and 1 pF, respectively. As shown in Figure 10, the outputs of the generators are the desired result. In Figure 11, the SNR of the output of the generators is observed.

Figure 10 shows output waveforms from the generator. The frequency of the signals is 3.125 MHz, one-sixteenth of the clock. The amplitude in each case is given by the reference voltages employed: ±300 mV under a supply voltage of 1.2 V. Figure 11 shows the output for a 3.125 MHz signal with SNR of 20.91 dB. The second and third order harmonic distortions are −31.37 dB at the frequency of the clock.

5 The filter

The clock mapping generator shown in Figure 6 generates the appropriate clock signals shown in Figure 7 for the signal generator and the programmable bandpass filter (SC filter) based on an external master clock. The SC structure can be used as the filter to improve SNR.

Figure 9 The circuit of C-Q version of the generator

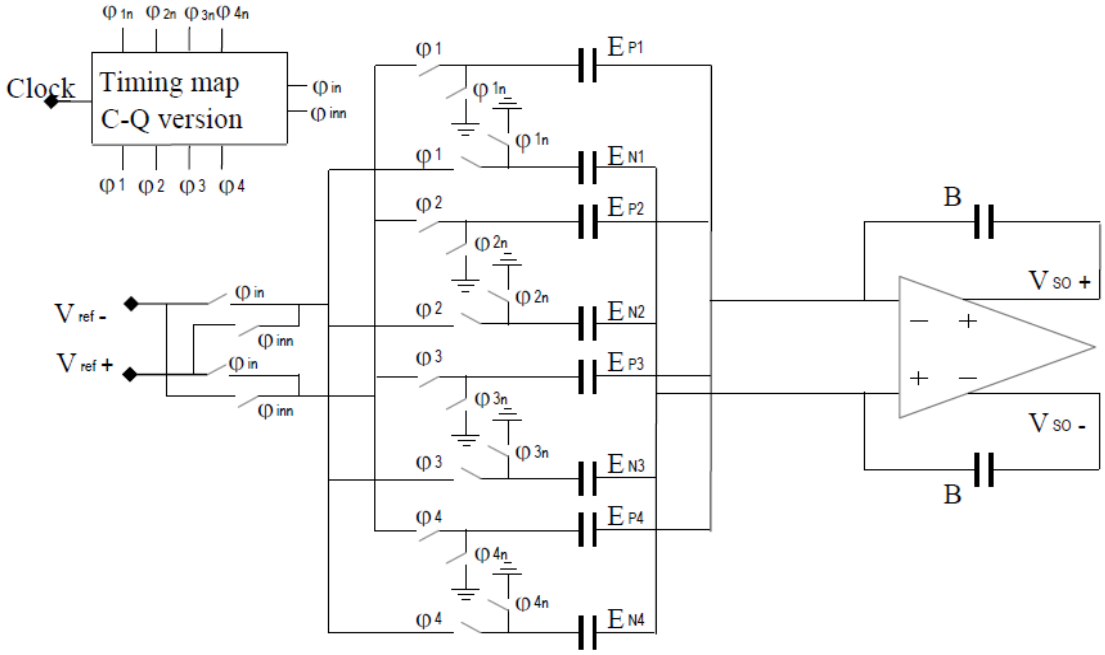


Figure 10 The outputs of the C-Q version generator

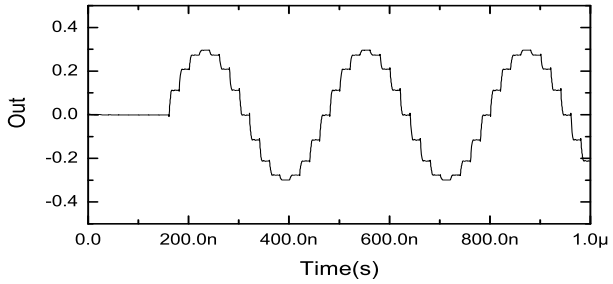
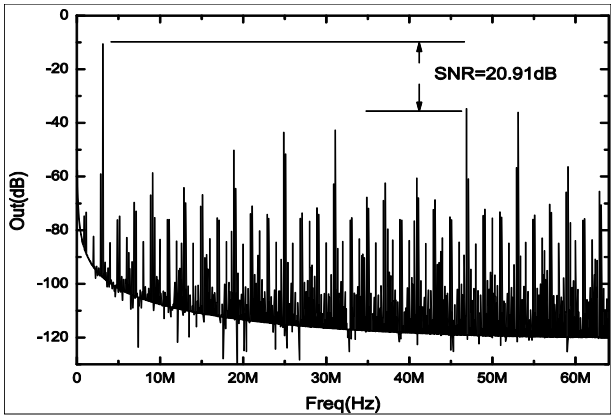


Figure11 The FFT of the output by the C-Q version generator



To illustrate the concept of the filter consider schematic based on SC techniques illustrated in Figure 12. The method is further improved by the use of a linear time-variant filter, where both operations signal generation and filtering is merged in the filter itself. The proposed approach maintains the attributes of digital control, programmability, and robustness, and reduces significantly the area overhead with respect to the other discussed approaches. Moreover, the proposed structures include the simplicity in design methodology, the digital process of test responses and the high speed in test execution.

An important advantage of this structure is that the amplitude of the sinusoidal generator output can be easily programmed by adjusting the reference voltages or using a bank of capacitors to adjust *B*. Simulation results shown in Figure 13 illustrates the feasibility of the proposed method.

Figure 13 shows output waveforms from the sinewave generator with the SC filter. The amplitude of the output is ±200 mV under a supply voltage of 1.2 V. The settling time of the system is less than 0.5 u. In order to achieve the sinewave with a high SNR, an initialising filter is employed behind the SC filter. Figure 14 shows the FFT of the output of the SC filter. The result shows the output for a 3.125 MHz signal with SNR of 42.2 dB.

Figure 12 The circuit of SC filter

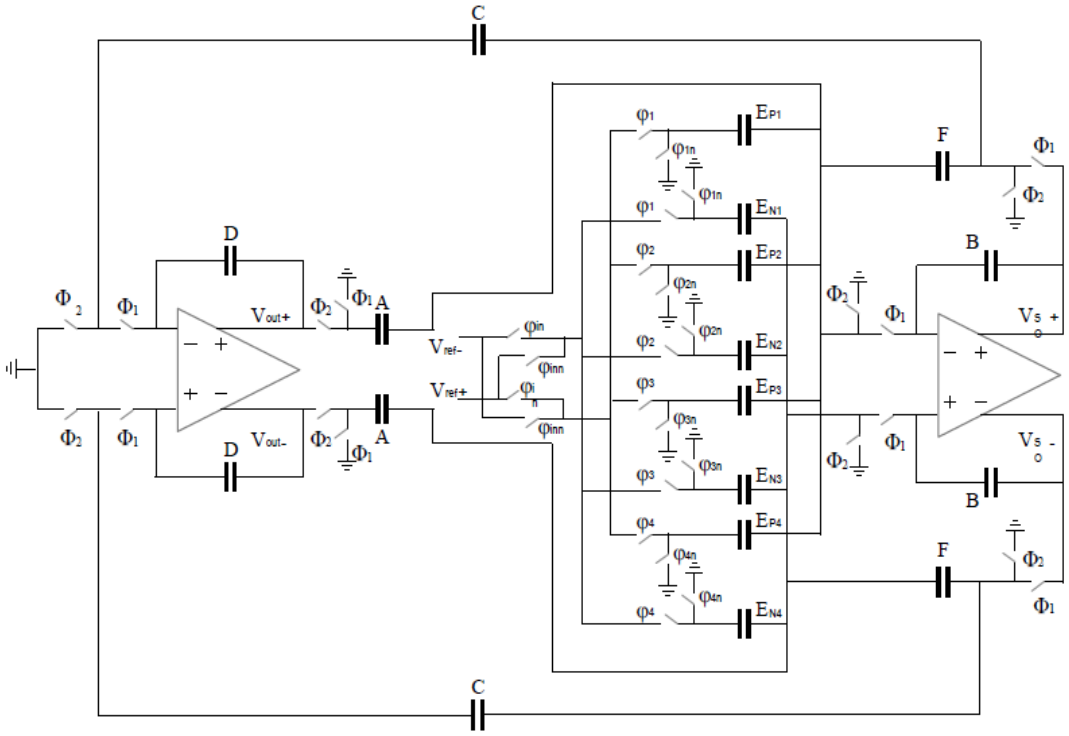


Figure13 The outputs of the SC filter

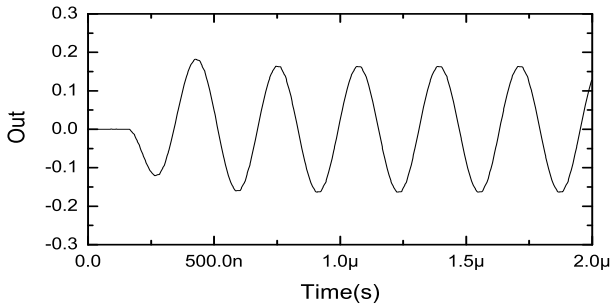
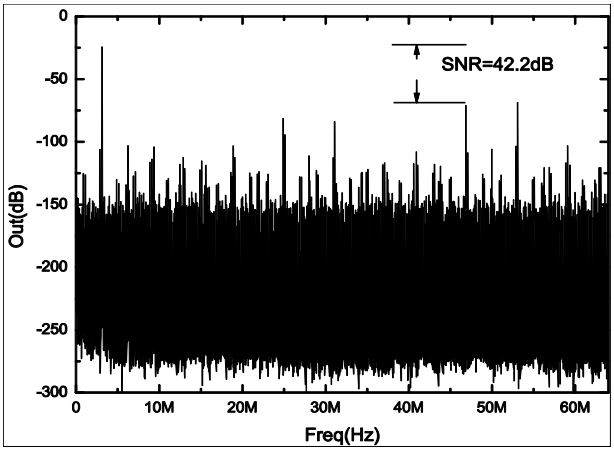


Figure14 The FFT of the output by the C-Q version generator



6 Conclusions

A practical BIST technique for analogue circuits has been presented. It allows the direct measurement of both the magnitude and harmonic distortion the magnitude and harmonic distortion characteristics of a DUT at various frequencies. The use of complex analogue instrumentation is avoided, potentially reducing the test time and cost. A CMOS implementation of the proposed system was design; to this end, a simple on-chip signal generator and a filter are developed. Circuit-level considerations and experimental results for the different building blocks were provided demonstrating the feasibility of a built-in spectrum analyser. The sinewave generators with the SC filter: The amplitude of the sinewave is 400 mV with SNR of 42.2 dB at a supply voltage of 1.2 V. The settling time of the system is less than 0.5 u and the power is less than 5 mW.

Acknowledgements

This work was supported by Natural Science Foundation of Heilongjiang Province (grant no. QC2011C087). The project work was also completed with the help and guidance of many colleagues of NXP Semiconductors, The Netherlands. It is my great pleasure to acknowledge their technical, organisational and social support.

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