A Wideband Linear Direct Digital RF Modulator using Harmonic Rejection and I/Q-Interleaving RF DACs

M. Mehrpoo, M. Hashemi, Y. Shen, R. van Leuken, M. S. Alavi, L. C. N. de Vreede
Delft University of Technology, Delft, The Netherlands

***Abstract*— This paper presents a wideband linear direct digital RF modulator (DDRM) in 40 nm CMOS technology. It features an advanced 2^{nd}-order-hold interpolation filter and I/Q-interleaving harmonic rejection RF DACs. The 2×9-bit DDRM core occupies 0.21 mm^2 and consumes only 110 mW at 1 GHz. Within the 0.9–3.1 GHz frequency range, the peak output power reaches +9.2 dBm and the $3^{rd}/5^{th}$ harmonic rejection, C-IMD3, and OIP3 are respectively better than 30 dB, −44 dBc, and +25 dBm. The EVM and ACPR at 3 GHz for a 57-MHz 64-QAM signal are better than −30 dB and −45 dB, respectively, and ACPR remains as low as −44 dBc up to a wide bandwidth of 110 MHz.**

***Index Terms*— RF DAC, direct digital RF modulator, harmonic rejection, 2^{nd}-order-hold, carrier aggregation, LTE**

I. Introduction

Digital-intensive transmitters (DTX) have become popular as they can offer higher integration, architecture simplicity, frequency agility, and compatibility with nanoscale CMOS compared to their analog counterparts [1]–[4]. For PAs, however, non-CMOS technologies are still preferred due to their superior linearity performance at high powers.

A key requirement of a modern cellular (e.g. LTE-Advanced) TX is to handle various frequency bands as well as carrier aggregation, which allows up to 5×20 MHz channels to be dynamically allocated. To accomplish such multi-band, high-bandwidth communication, a wideband reconfigurable DTX directly driving an external PA (Fig. 1) is a more efficient solution for an RF TX chain, compared to a fully CMOS approach.

II. Direct Digital RF Modulators

Among the existing DTX architectures, a digital Cartesian (I/Q) approach is potentially the best candidate because of its scalability to large bandwidths. Over the past decade, a number of DTX architectures capable of direct upconversion of the digital I/Q baseband signal to the desired RF carrier have been investigated [1]–[4]. These so-called direct-digital RF modulators (DDRM) [1] integrate the functionalities of baseband I/Q DACs and mixers into two parallel-connected I/Q RF DACs. There are three challenges commonly related to I/Q RF DAC approaches when dealing with carrier aggregation.

First, the traditional way of using two separate I/Q RF DACs and combining them at the output is prone to mismatch and excessive output parasitics, limiting the TX intrinsic image rejection and RF power, respectively [3].

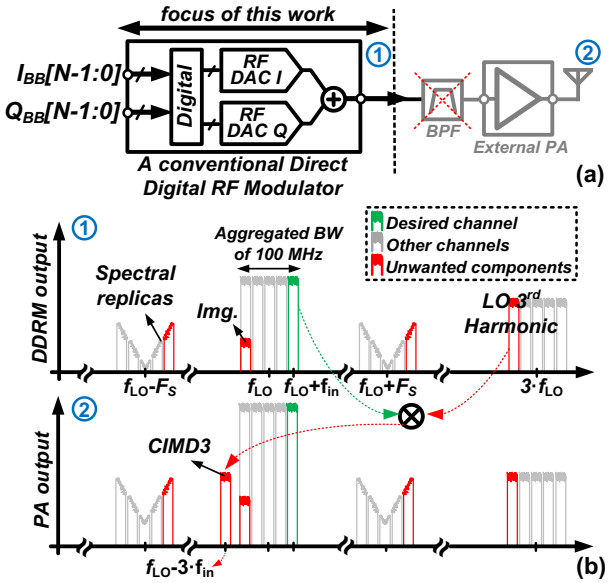

Fig. 1. DDRM (a) application context, (b) associated challenges.

Second, in the absence of baseband and RF filters, the sampling spectral replicas can produce relatively large spurious emissions, demanding a relatively high baseband sample-rate to suppress the replicas for wideband signals.

Third, an RF DAC which utilizes (hard-)switching mixers produces LO harmonics at the output that are detrimental in two ways. The harmonics lead to out-of-band spurious emission, imposing additional filtering requirements at RF. Moreover, the LO 3^{rd} harmonic at the DDRM output tend to yield counter-intermodulation distortion (C-IMD3) at the PA output [5], [6]. This is due to intermodulation of the RF signal components at around f_{LO} and $3\times f_{LO}$ through the nonlinear PA. As demonstrated in Fig. 1(b), C-IMD3 falls at f_{LO}-$3\times f_{in}$, which is difficult to filter. For the LTE carrier aggregation scheme, where carriers can be allocated up to ±50 MHz away from f_{LO}, C-IMD3 may fall into the restricted bands with tough spurious emission limit requirements.

III. Proposed Architecture and Key Features

All the aforementioned challenges are addressed by the DDRM architecture proposed in Fig. 2. To circumvent the

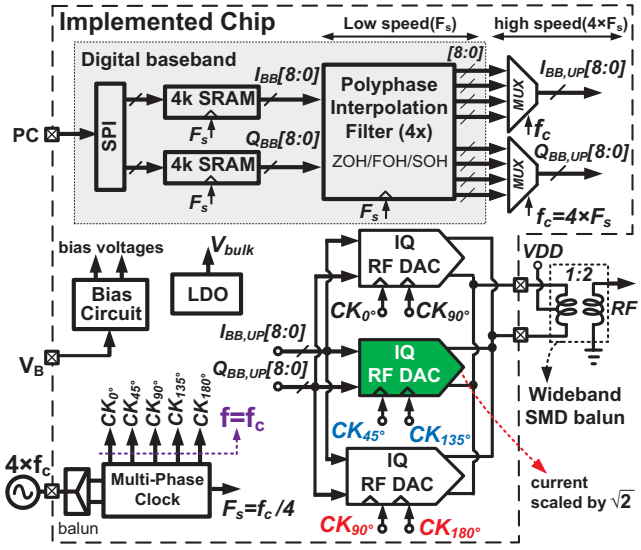

Fig. 2. Proposed direct-digital RF modulator block digram.

problems associated with using two separate I/Q banks, an innovative I/Q-interleaving technique based on 50% LO is proposed, and its operation is conceptually demonstrated in Fig. 3. Thanks to the employed bitwise XOR/OR logic, each unit-cell can generate a non-overlapping 25% duty-cycle output signal (V_{out}) covering all four quadrants of the I/Q-plane. Digital I/Q combining has also been recently deployed by [3] based on time-multiplexing with AND/OR logic for 50% LO. However, it relies on clipping the complex signal (|I|+|Q|≤N) to avoid I/Q overlap. This causes distortion and makes the use of digital pre-distortion (DPD) inevitable, thereby limiting the linearity, especially for large signal bandwidths. Here, unlike [3], no constraint is required for |I| and |Q| values due to the non-overlapping output waveforms.

Additionally, an advanced 2^{nd}-order-hold (SOH) interpolation filter with a $sinc^3$ transfer function is proposed to suppress the replicas, located F_S away from the carrier, below the modulator noise level. The filter is deployed to upsample the digital baseband I/Q signals, sampled at F_S, by 4× up to the carrier frequency. The I/Q signals are in a 9-bit unsigned format and stored on two on-chip SRAMs. The selection of F_S and the upsampling factor balances the replicas separation, data path power consumption, and the filter complexity. The SOH filter is realized based on a polyphase FIR filter structure consisting of four parallel sub-filters operating at the lower sample-rate of F_S. Only the filter output multiplexer operates at $4\times F_S$. Programmable powers-of-two coefficients are adopted to reduce the digital hardware complexity.

Moreover, the proposed DDRM also incorporates a multi-phase LO harmonic cancellation technique to reject $3^{rd}/5^{th}$ harmonics. For this purpose, three parallel-

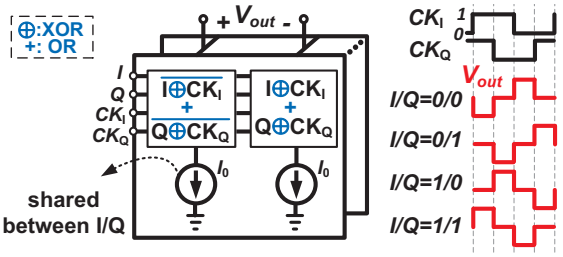

Fig. 3. I/Q-interleaving RF DAC concept.

connected IQ RF DACs are exploited, which are driven by the same baseband I/Q signals but different LO phases of $(0°, 45°, 90°)$ and current scaling factors of $(1, \sqrt{2}, 1)$ [5]. The multi-phase LO approach has been first demonstrated in [5] using conventional (Gilbert Cell) mixers. In this work, the multi-phase LO harmonic rejection is for the first time combined with RF DACs, providing a wideband LO $3^{rd}/5^{th}$ harmonics attenuation.

IV. Circuit Implementation Details

The I/Q-interleaving RF DACs are based on the current-steering principle, which are well-known for their superior linearity at high speeds [7]. A segmented structure is adopted with 3-bit binary-coded LSB and 6-bit thermometer-coded MSB cells. The binary-to-thermometer decoder logic is implemented in a distributed fashion, locally per each unit-cell, and the oversampled digital I/Q bit-stream is retimed at each unit-cell. As shown in Fig. 4, the unit-cells' current is set by a current mirror consisting of M_1/M_2, which is shared for the I/Q path. M_1/M_2 sizes are determined as a trade-off between the mismatch, total area, and speed. To implement the $\sqrt{2}$ current scaling factor required for harmonic rejection, the I_{REF} of the RF DAC with 45° LO is scaled. The octave-phase LO is generated by making use of an off-chip $4\times f_{LO}$ clock applied to on-chip cascaded divide-by-two stages.

The XOR/OR for the I/Q-interleaving operation is implemented as a current-mode logic by stacking it on top of current sources, as indicated in gray in Fig. 4. This allows a faster switching operation and reduction in power consumption via reusing the current I_0. M_3 sufficiently

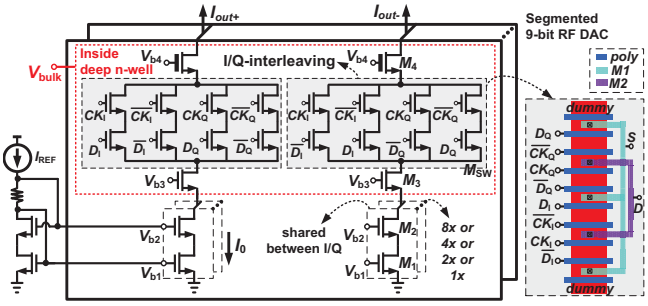

Fig. 4. I/Q RF DAC unit-cell circuit implementation details.

shields the source of switching transistors (M_{SW}) from the excessive parasitic capacitance on M_2 drain, hence improving the linearity performance at high frequencies. A customized compact layout for the switching devices, illustrated in Fig. 4, helps to further minimize the parasitics. Sufficient voltage headroom over all the cascode devices is provided by choosing V_{DD} of 2 V. To withstand large voltage swings at the output nodes and alleviate interaction between DAC branches, thick-oxide cascode devices (M_4) are locally used per each cell. Excessive V_{th} for the cascode devices is prevented by placing M_3, M_4 and M_{SW} inside deep n-well and elevating their bulk voltage using an on-chip LDO.

V. Measurement Results

The DDRM was fabricated in an LP 40 nm CMOS process, and the core circuit occupies 0.21 mm^2 as illustrated in Fig. 5. The RF output is implemented differentially, and due to area constraints, the output balun was placed off-chip. The low-speed part of the interpolation filter occupies only an extremely small portion of the whole digital front-end. The multi-phase clock circuit, the digital front-end, and SRAMs are shared with other front-ends implemented on the same die. Consequently, their area and power consumption are not optimized specifically for the DDRM. The clock circuitry power consumption varies from 17 to 29 mW at 1 to 3 GHz and the output draws 35 to 29 mA at 1 to 3 GHz from a 2 V supply. The LO and data buffers, decoders, and the high-speed part of the interpolation filter draw 36 to 80 mA at 1 to 3 GHz from a 1.1 V supply. The peak drain efficiency is 13% and occurs at around 1.5 GHz.

Fig. 6(a) shows the measured peak P_{out} and LO harmonics level over a broad f_{LO} of 0.9–3.125 GHz. The peak P_{out} reaches +9.2 dBm at 1.5 GHz after deembedding, and its variation over the entire frequency range is <5 dB due to the output parasitics and the off-chip balun. Thanks to the harmonic rejection technique, the uncalibrated $3^{rd}/5^{th}$ harmonic rejection remains better than 30 dBc [1]. The measured output phase noise floor at 2 GHz with unmodulated (static) and CW modulated carrier are −145 and −143 dBc/Hz, respectively.

The I/Q image of a single-tone signal is −49 dBc (f_{LO} = 3 GHz), which reduces to < −67 dBc after a simple I/Q gain correction. Fig. 6(b) demonstrates the output spectrum of two-tone signal at 1.5 GHz. Fig. 6(c) and 6(d) show the measured uncalibrated C-IMD and IMD levels across f_{LO} for single- and two-tone signals, respectively. Up to 3 GHz, the C-IMD3 and IMD3 remain below −44 and −41 dBc,

[1]Considering the cascaded DDRM/PA system, this is sufficient to meet the basestation spurious emission limit of −30 dBm/MHz (e.g. external PA condition P_{out} = 1 W and OIP3 = +30 dBm).

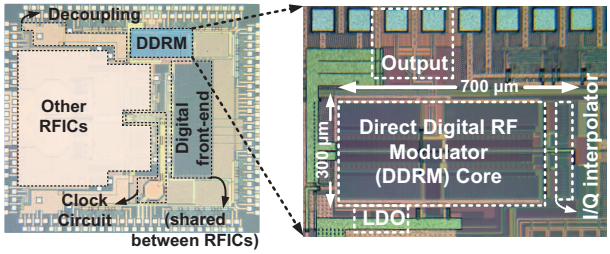

Fig. 5. Die microphotograph of the implemented DDRM.

respectively. Based on the measured P_{out} and IMD3 at 3 GHz, the corresponding OIP3 is around +25 dBm.

As indicated in Fig. 7(a), the SOH filter achieves a suppression of more than 30 dB compared to a ZOH, for BW = 100 MHz and F_s = 400 MHz. Fig. 7(b) shows the measured spectrum and EVM for a single-carrier (SC) 57 MHz QAM signal. Without employing DPD, EVM and ACPR1 are −30 dB and −44 dBc, respectively. ACPR and P_{out} vs. f_{LO}, for a relatively narrowband QAM signal, are shown in Fig. 7(c). Across f_{LO} of 1 to 3 GHz, ACPR remains between −52 to −46 dBc, and up to BW of 110 MHz at 3 GHz ACPR is as low as −44 dBc (Fig. 7(d)).

Constrained by the on-chip SRAMs size, the performance could not be measured with an actual LTE signal. However, the spectrum for a multi-tone signal with a PAR of 7 dB and BW of 18 MHz (resembling LTE signal with 100 resource blocks) was measured as shown in Fig. 8. For a single 18 MHz channel, located 40 MHz away from f_{LO}, APCR and C-IMD3 of < −48 dBc is achieved, meeting the most stringent basestation requirement of −45 dBc.

Table I summarizes the performance and compares it

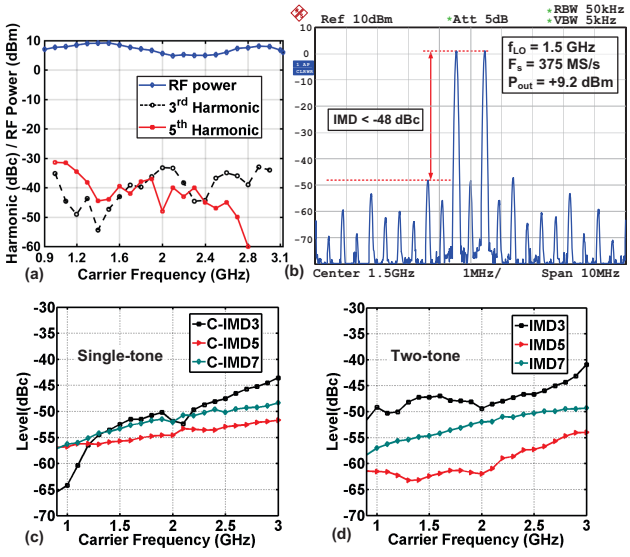

Fig. 6. Measured (a) peak RF output power and (uncalibrated) harmonic rejection vs. f_{LO}, (b) two-tone signal RF spectrum, (c) C-IMD3 and (d) IMD3 vs. f_{LO}.

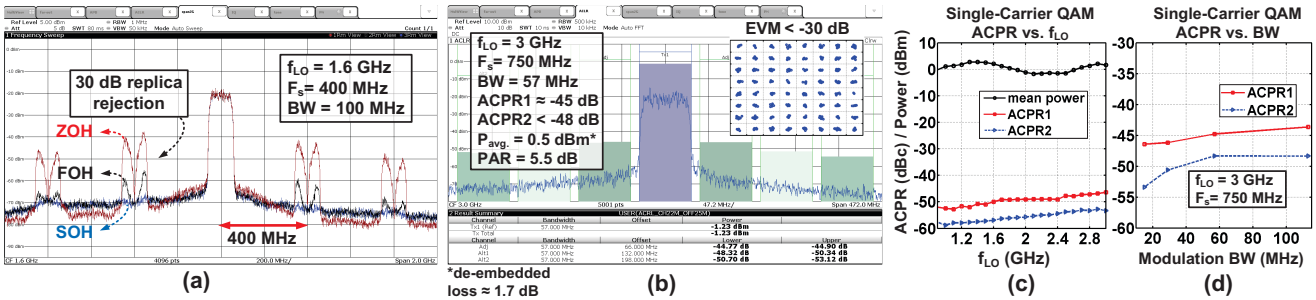

Fig. 7. Measured single-carrier 64-QAM (a) replicas for wide BW, (b) ACPR and EVM, (c) ACPR vs. f_{LO}, (d) ACPR vs. BW.

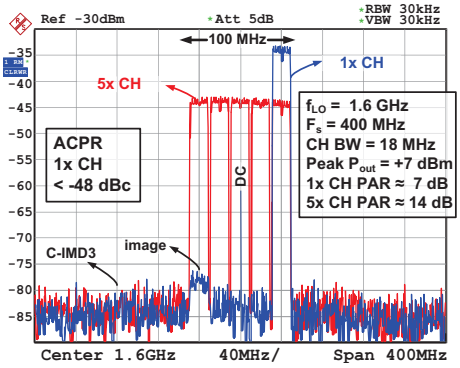

Fig. 8. Measured spectrum with multi-carrier aggregation.

to the prior art. This is the first reported DDRM that implements the LO harmonic cancellation and suppresses replicas for large bandwidths. The mixing-DAC in [7] has a better linearity, but it uses calibration and has a significantly lower RF output power and larger area and power consumption. Compared to [4], our DDRM achieves superior linearity and a larger bandwidth over a broader frequency range, at the cost of lower efficiency. The reported linearity of [2] is notably less, with a comparable efficiency and RF output power.

TABLE I
PERFORMANCE SUMMARY & COMPARISON WITH PRIOR ART

Parameter	This work		[4] JSSC'15	[2] RFIC'14	[7] JSSC'16	[6]* ISSCC'13	[1] JSSC'07
Architecture	DDRM		DDRM	DDRM	RFDAC	analog	DDRM
Process (nm)	40		28	65	65	40	130
Core area (mm^2)	0.21		0.25	0.18	1.6	1.4	0.7
Peak P_{RF} (dBm)	+9.2		+8	+11.9	-8	+12.1	N/A
P_{DC} (mW)	110/146[b][e]		41.3	227	380	142	157
Peak $\eta_{sys.}$(%)[a]	7		15.3	6.8	0.04	≈8.9	N/A
I/Q image (dBc)	-45/-49[b]		-44	-42	N/A	N/A	-43
C-IMD (dBc)	-56/-44[b]		-50	N/A	N/A	-60	-55
LO Harmonic Rej.	>30 dB		N/A	N/A	N/A	N/A	N/A
Frequency (GHz)	1.9	3	1	1.98	1.9/4.1	1.95	1.92
CH BW (MHz)	18	57	20	20	20	20	5
Modulation	SC 64QAM		M-T[c]	LTE	LTE	LTE	WCDMA
$P_{Avg.}$ (dBm)	-0.3	+1	+1	+2.5	≈-13.8	+3.2	-2
ACPR1 (dB)	-50	-44	-42[d]	-33.4	-69/-73	-41	-58
EVM (dB)	<-30		N/A	-28	N/A	-33.5	-34

* [6] does not include the baseband DACs
(a) $\eta_{sys.} = P_{RFout}/P_{DCtot}$, (b) value at f_{LO} of 0.9/3 GHz, (c) multi-tone signal, (d) measured in 5 MHz adjacent CH BW at 12.5 MHz offset, (e) not including the clock generation circuit power consumption (29 mW at 3 GHz)

VI. Conclusion

In this work, a DDRM incorporating an advanced 2^{nd}-order-hold interpolation filter, I/Q-interleaving and harmonic rejection RF DACs was proposed and implemented in 40 nm CMOS process. The DDRM simultaneously enables sufficient suppression of replicas and LO harmonics over 0.9–3.1 GHz frequency range while consuming only 110 mW at 1 GHz. With +9.2 dBm peak output power and <-48 dBc ACPR, the realized DDRM can act as an energy-efficient pre-driver for the next generation multi-band basestation PAs employing carrier aggregation.

Acknowledgment

This research was supported by STW project, SEED-Com and Catrene project, EAST. The authors would like to thank Ampleon and NXP and acknowledge contribution of A. Akhnoukh for his support and Prof. Masoud Babaie for helpful technical discussions.

References

[1] P. Eloranta et. al., "A Multimode Transmitter in 0.13 μm CMOS using Direct-Digital RF Modulator," *IEEE JSSC*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.
[2] B. Mohr et al., "A Digital Centric CMOS RF Transmitter for Multistandard Multiband Applications," *IEEE RFIC Symposium*, pp. 221–224, June 2014.
[3] Z. Deng et al., "A Dual-Band Digital-WiFi 802.11a/b/g/n TX SoC with Digital I/Q Combining and Diamond Profile Mapping for Compact Die Area and Improved Efficiency in 40nm CMOS," *IEEE ISSCC*, pp. 172–173, Jan. 2016.
[4] P. E. Paro Filho et al., "An Incremental-Charge-Based Digital Transmitter with Built-in Filtering," *IEEE JSSC*, vol. 50, no. 12, pp. 3065–3076, Dec. 2015.
[5] J. A. Weldon et al., "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," *IEEE JSSC*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.
[6] M. Ingels et al., "A Multiband 40nm CMOS LTE SAW-Less Modulator with -60dBc C-IM3," *IEEE ISSCC*, Feb. 2013.
[7] E. Bechthum et al., "A Wideband RF Mixing-DAC Achieving IMD < -82 dBc Up to 1.9 GHz," *IEEE JSSC*, vol. 51, no. 6, pp. 1374–1384, June 2016.