Interconnect and Thermal Aware 3D Design Space Exploration

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1 Abstract

Three-dimensional *Multiprocessor Systems-on-Chip (MPSoC)* are gaining in popularity due to their ability to integrate a wide range of devices such as *processing elements (PE)* and memories within the die stack. Vertical interconnections between layers of the stack are achieved using short *Through Silicon Vias (TSV)* with small propagation delays. The design of the vertical interconnect is non-trivial since the placement of TSVs influences both electrical performance, as well as thermal conduction in the die stack. The prevalence of thermal hotspots, and gradients between tiers of the stack limits the performance of 3D MPSoCs, and impacts dependability as well.

In this poster, we present an integrated flow for high-level design space exploration of 3D MPSoC architectures. The first step of the flow consists of a TSV topology exploration methodology that evaluates various user-specified design options for the vertical interconnect based on their electrical performance, and placement viability. Topologies that achieve performance requirements within area and signal integrity constraints are incorporated into the system floorplan. In the second step of the flow, the resulting system floorplans are evaluated in terms of their thermal performance using a Temperature-Power Simulator. This step uses a thermal model to estimate temperatures at different points in the die stack using instantaneous power dissipation corresponding to utilization rates from execution of the workload on PEs. A novel feature of our flow is its ability to include an active power management scheme to emulate the behaviour of runtime *Dynamic Voltage-Frequency Scaling (DVFS)*, and thus provide a more realistic estimate of thermal performance.

The insight gained from this exploration can be used to evaluate design choices in terms of performance, as well as their thermal implications, and guide optimization of the architecture. In this poster, we illustrate our presented flow in the context of a network-on-chip based 3D MPSoC.

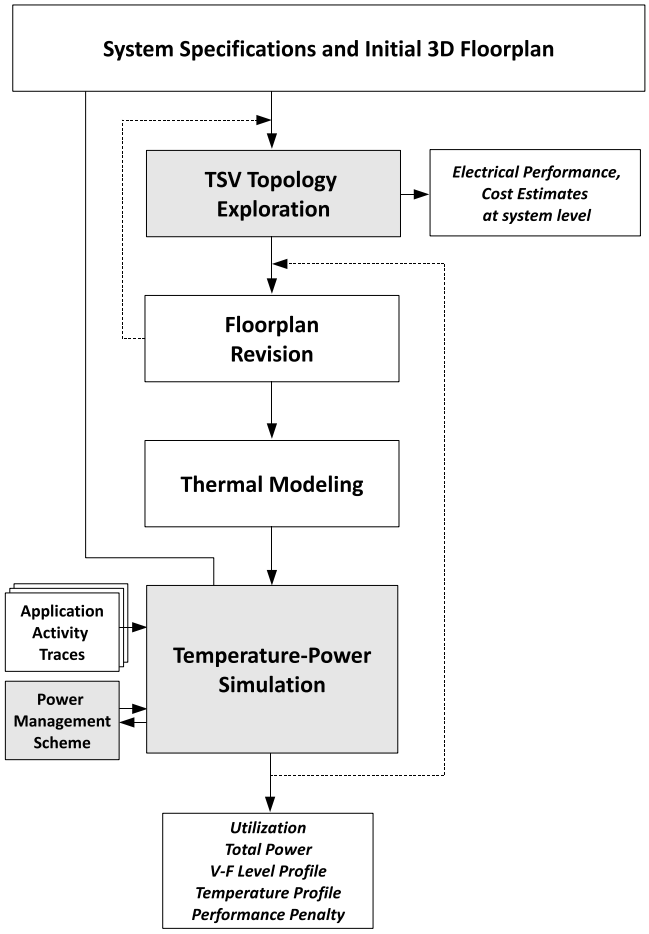

Figure 1: Illustration of the integrated flow consisting of TSV Topology Exploration followed by Temperature-Power Simulation based on a thermal model of the die stack.