An Advanced Cache Power Model for an Embedded Processor using SLEEP Methodology

Jia Chen
TU Delft
EEMCS/MECE/CAS
Mekelweg 4,
2628 CD Delft
The Netherlands

Yijun(Sue) Xu
Philips Research
ED&T
Prof. Holstlaan 4,
5656 AA Eindhoven
The Netherlands

Rene van Leuken
TU Delft
EEMCS/MECE/CAS
Mekelweg 4,
2628 CD Delft
The Netherlands

***Abstract*—Low power design of the digital SoC (system on a chip) is a hot research area recently. The power estimation techniques can be implemented at all abstraction levels in the low power design flow, of which system level is on the top. The power estimation in this level can greatly save the designer's effort and time of going to the lower design levels. However, in system level, the detailed information about the circuit of the system cannot be extracted. How to guarantee the accuracy is critical for system level power estimation.**

***Index Terms*— Digital SoC, Power estimation, power model, processor, cache power model.**

I. INTRODUCTION

The system level power estimation methodology (SLEEP) developed in Philips Research aims at a higher simulation speed than RTL/gate-level simulation and to be accurate. It is based on SystemC Transaction Level Modeling (TLM) for system simulation and gate-level power values for accuracy. Seven different types of on chip components are distinguished for power estimation. The processor core is one of the most important components in a digital SoC. Therefore; accurate power estimation of the processor is of great importance to that of the whole system.

II. SYSTEM LEVEL DESIGN

System level design is the first step of realization of a complex electronic system. Power estimation at this level has the advantage of relatively short simulation time as compared to circuit level power estimation. However, since the real circuit feature has not been determined at the system level, it is difficult to realize sufficient accuracy of the power usage.

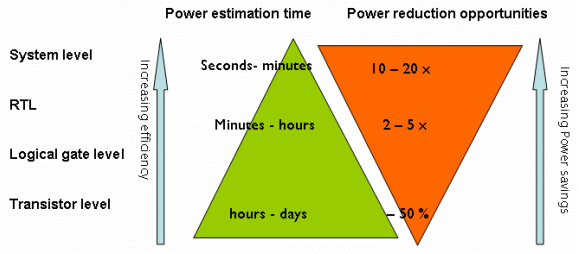

Figure 1. Power estimation in different design levels.

III. THE SLEEP METHODOLOGY

SLEEP is a SystemC simulation environment based on a high-level power estimation methodology for System-on-Chip (SoC) design. Its goals are:

- System level power estimation,
- Enable trade-off between performance (i.e. speed) and power consumption,
- Generate early feedback on power consumption of application software.

SLEEP aims to be

- As accurate as possible,
- Faster than RT/gate level simulation.

IV. THE SLEEP ESTIMATION FLOW

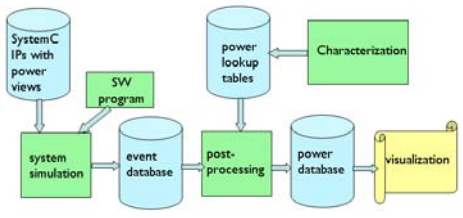

Figure 2. The SLEEP power estimation flow.

During system simulation, power related transactions are recorded and stored in a power event database. The power event database is annotated with power look up tables in the post-processing step and its result is used to visualize power figures. The power look up tables numbers are obtained by level power simulations using a program called Diesel.

V. THE SLEEP PROCESSOR POWER MODEL

In SLEEP, 7 different components are distinguished for power estimation:

$$P_{system} = P_{processor} + P_{bus} + P_{memory} + P_{dedicated-ip} + P_{I/O} + P_{clock-tree} + P_{clock-generator}$$

Generally, a processor has a major impact on the power consumption of the whole system. Hence, an accurate estimation of the processor power consumption is needed.

SLEEP uses a mode based processor power model, which distinguishes several power modes of the processor (such as active mode and standby mode).
The average power consumption of a processor in a power mode can be described as:

$$P_{processor\_avg} = P_{core} + P_{cache}$$

P_{core} : the average power value of the core.

P_{cache} : the average power value of the cache.

We distinguish between a cache hit and a cache miss:

$$P_{processor\_avg} = P_{core} + \frac{nP_{cache\_hit}}{N} + \frac{mP_{cache\_miss}}{N}$$

N : total cycle time.
n : the total cache hit time during the execution of the software.
P_{cache_hit} : the average power value of each cache hit.
m : the total cache miss time during the execution of the software.
P_{cache_miss} : the average power value of each cache miss.

VI. SIMULATION OF AN ARM1176 SUBSYSTEM

We show the SLEEP power estimation results of an ARM1176 processor in Figure 3***b)*** and in 3***a)*** a gate level estimation result of Diesel. In both simulations the processor is executing an MP4 decoding algorithm.

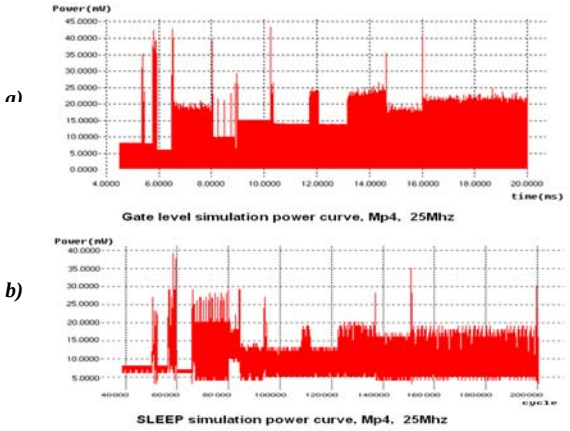

Figure 3. Simulation result of an MP4 decoder. We can observe a similar power profile between Diesel and the SLEEP simulation with a cache power model.

VII. ACCURACY ANALYSIS

f= 25 (MHz) SLEEP simulation	Pavg(mW)	Avg.Error	Ppeak(mW)	Peak.Error
Mp3 without cache power model	5.22	15.7%	N	N
Mp3 with cache power model	4.09	9.3%	38.46	14.7%
Mp4 without cache power model	5.22	53.1%	N	N
Mp4 with cache power model	3.50	43.0%	38.46	13.9%

Table 1. Accuracy analysis of the SLEEP power estimation for the ARM processor

Table 1 shows the deviations between SLEEP and Diesel for a number of simulation results. The cache power model has improved the power estimation accuracy by about 8% for average power values, leaving about 15% inaccuracy in peak power value for active mode.

VIII. CONCLUSION

In this paper, accuracy of the SLEEP processor power model is improved by adding the cache behavior. The simulation results on an ARM based SoC show that cache power modeling improves average power estimation by 8% comparing to the existing SLEEP processor power model and has an inaccuracy of peak power estimation about 15%. A design space exploration in terms of power with SLEEP using cache power modeling shows that this model can help with quickly and accurately capturing the power behavior of software programs on a SoC.

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