# A 19.6 ps, FPGA-Based TDC With Multiple Channels for Open Source Applications

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*Abstract*—This work presents a multi-channel, time-to-digital converter (TDC) based on a field-programmable gate array (FPGA). A thorough characterization of the TDC, based on a Xilinx Virtex-6 FPGA, is presented and several performance parameters are described, including distortions due to the FPGA architecture, temperature effects, intra-chip position variation, and chip-to-chip variation. An optimized TDC exhibits 10 ps LSB duration, an integral non-linearity range of 3.86 LSB, and an input range longer than 100 $\mu$s. Total time uncertainty (single-shot jitter) is measured to be 19.6 ps at a time difference of 40 ns, and less than 400 ps at a time difference larger than 100 $\mu$s.

*Index Terms*—Field-programmable gate array (FPGA)-based time-to-digital converter (TDC), multi-channel time-to-digital converter (TDCs), positron emission tomography (PET).

## I. INTRODUCTION

TIME interval measurements are required in many applications. In the field of positron emission tomography (PET), time interval measurements are indirectly used to narrow down the location of positron emission, thus improving SNR. Especially in time-of-flight PET, the accuracy of the time measurement is critical for data reconstruction. Throughput and the number of channels are also important, as they effect the measurement speed and the system complexity. For PET, it is desirable to have physical constraints, such as scintillator coupling or sensor response, be the limiting factor, rather than the timing measurement. High demands are therefore placed on the time measurement devices, and sub-100 ps systems with high accuracy and throughput are desired. For PET systems, effective implementations in ASICs have been shown [1], [2]. The downside of CMOS implementations is the custom development process. It is time consuming, and difficult to adapt to a slightly different system.

Recent developments show that there is a growing interest in time measurement circuits implemented in FPGAs [3]–[5]. FPGAs are integrated circuits, which consist of blocks with predefined logic; digital logic can be easily created using a hardware description language. The description language makes it possible to implement, efficiently, the same hardware on

different FPGA platforms—implemented systems are portable. Compared to full-custom chips, FPGAs have advantages in flexibility and development time. FPGAs are designed for parallelism, which makes them applicable for multi-channel and high throughput systems. However, FPGA-based TDCs are limited by the FPGA's pre-defined structure.

An open source initiative to apply FPGA-based systems in PET was recently launched [3]. The advantage of an open source approach in PET is the flexibility of new designs and the significant reduction of development time. In addition, performance can improve more quickly by taking advantage of the continuous evolution of FPGA technology. An example of open source TDC can be found in [6].

Recent PET scanner prototypes made a case for open-source, reconfigurable time measurement systems [3]. In this work we describe the architecture and characterization of an FPGA-based, 10 ps LSB duration TDC targeting PET applications. The TDCs with the best DNL and INL show a differential non-linearity (DNL) better than $\pm 2.0$ LSB, and an integral non-linearity (INL) better than $\pm 2.5$ LSB. In the present work, variations in TDC performance are characterized as a function of intra-FPGA location, two different FPGAs, and temperature. Also presented are issues from using multiple TDCs on the same FPGA.

## II. ARCHITECTURE

There are different ways of building a TDC on a FPGA. The major architectures are based on simple delay lines and Vernier delay lines [3], [4], [7]–[10]. Also, other structures have been invented to take advantage of the properties of the FPGA logic [5], [11], [12]. Great care must be taken in the design phase, which includes trade-offs in resource utilization, stability, and calibration difficulty, amongst other concerns.

An FPGA has a pre-defined structure based on look-up tables (LUTs), additional selection, and carry logic. The LUTs are used to define logic functions, and the selection and carry logic can be used to implement branches, multipliers, or adders. The present work is a port to the Virtex 6 of the Nutt architecture used in [10] which uses the carry logic of slices to build delay lines. The two-stage architecture, which consists of a coarse counter for the TDC's most significant bits and a fine interpolator implemented using a delay line for the least significant bits, has also been used on previous generations of FPGAs [13], and will likely be useful for future generations as well.

A schematic view of this two-stage architecture is shown in Fig. 1. The delay line is implemented by using the carry logic of the slices, with the multiplexers acting as delay elements. The complete carry chain must have a delay longer than one

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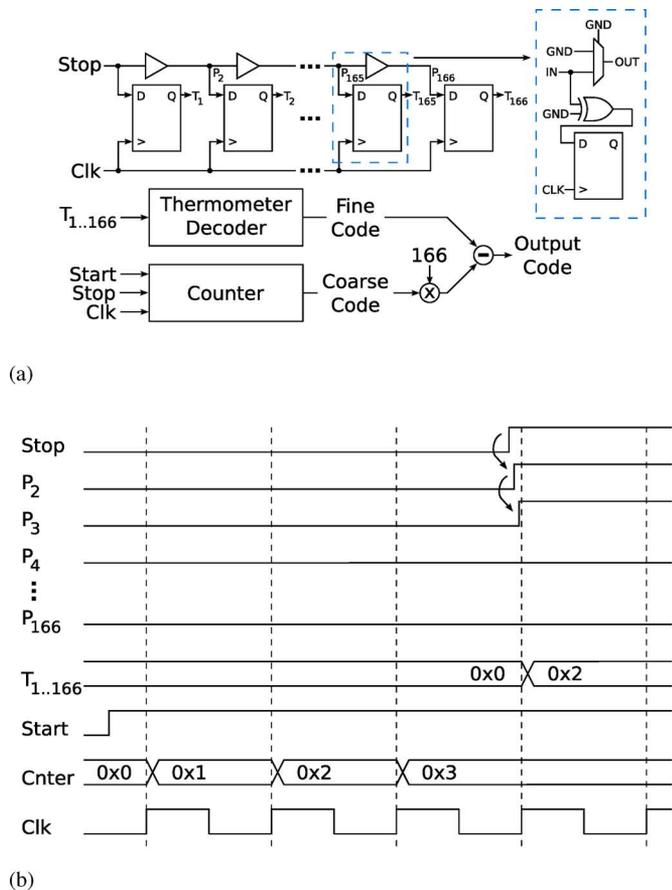


Fig. 1. TDC architecture. (a) Block diagram and a (b) timing diagram, with the delay line for the LSB portion and the coarse counter for the MSB portion of the measured time interval.

clock cycle. The number of delay elements, multiplexers, and the period of the clock will determine the LSB duration of the TDC.

When the global start signal is raised, a coarse counter starts. When an individual's stop signal is raised, the TDC's delay line begins to propagate, and on the following clock cycle the status of the delay line, $P_{1...166}$ in this case, is saved along with the value of the coarse counter. The exact length necessary for the fine code will vary with environmental conditions. Any metastability issues arising when saving the delay line value will be removed by the thermometer decoder. The value of the coarse counter minus the time measured by the delay line gives an absolute time. Two such TDCs can be combined to measure the differences between times, as described in Section III.E. To save bandwidth, the thermometer code of the delay line needs to be encoded to a binary value first before it can be used to determine the time interval by combining it with the coarse counter value. The mapping of the thermometer code from the registers to the binary value is affected by measurement variations and non-linearity, which must be trimmed for voltage and temperature variations. The origin of non-linearity is dealt with in more detail later. Here, calibration is defined as the compensation for non-linearity using previously acquired data.

Due to restrictions on operation of the thermometer decoder and its associated logic, the reset period is one clock cycle.
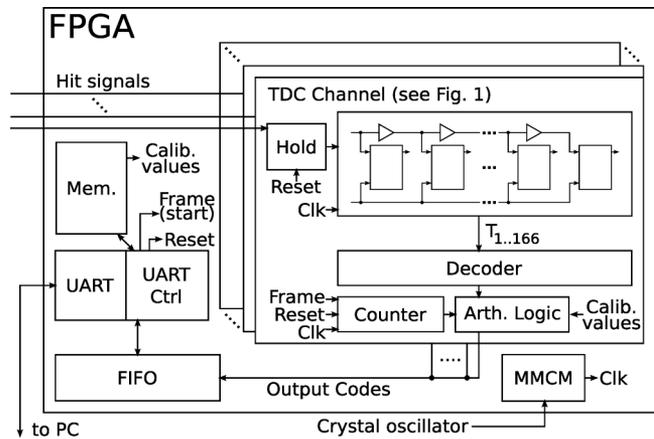


Fig. 2. System architecture.

So the first clock cycle of the measurement period is used for storing the measurement and the second one for resetting the delay line. A clock frequency of roughly 600 MHz is used on the Virtex-6 (XC6VLX240T) FPGA, giving a reset time of 1.67 ns. The clock is generated by an on-FPGA clock manager using an external 66 MHz crystal oscillator as a reference. The LSB duration of this architecture is limited by the delay of the multiplexers in the carry chain, with the clock period determining the size of the delay line. For a clock period of 1.67 ns, this architecture's delay line length is 165 elements, with an LSB duration of 10 ps and a throughput less than 300 MS/s.

Many other elements must be implemented in order to make a usable TDC with on-line encoding and external communication possibilities. All of these elements are shown in Fig. 2. A system monitor is used to measure the temperature and voltage on-chip, before the results stream through the USB connection to an external computer. A mixed-mode clock manager is used to achieve a low jitter 600 MHz clock [14]. The ROMs attached to the encoder are used to compensate the fine delay line result for non-linearity. One ROM is for static non-linearity while another ROM is for dynamic non-linearity, requiring updates whenever the temperature or local voltage shifts.

## III. CHARACTERIZATION

### A. Experimental Setup

The performance of the TDC was characterized using two types of tests: (1) a density test [15] and (2) inputting pulses of precise duration.

For a density test, a random time interval generator is needed. This is realized using a single-photon avalanche diode (SPAD) placed in the dark with a count rate below 10 kHz, giving a sufficiently uniform, random time distribution [16]. The SPAD is attached to the FPGA using an SMA-cable. The FPGA is placed inside a temperature chamber to control the environment temperature. Temperature and voltage data are sent to a computer as well as all encoded TDC values. The encoded values are analyzed offline to calculate the non-linearity. The FPGA-based TDC has the delay line shielded by one ring of blank slices, which have no implemented logic, to reduce the influence of the switching logic on the FPGA. All density tests were run until

there was an average of 1 000 counts per fine code. Based on the statistics of density tests, the measurement error (sigma) of DNL values will be less than 0.04 LSB, and in INL values this error will be less than 0.4 LSB [17].

The second method of characterization, inputting pulses of precise duration, will be described in detail later.

### B. Non-Linearity

Previous TDCs based on the proposed architecture used a Virtex-5 [10]. Porting the architecture from the Virtex-5 to the Virtex-6, used in this work, gave an improvement in LSB duration from 17 ps to 10 ps at room temperature, with an improvement in the measured loopback jitter from 20 ps to less than 14.2 ps, as will be presented in Section III.E. The variation in the realized duration of a single bin, called the DNL, will be expressed in least significant bits (LSBs); one LSB will indicate a variation that is exactly the chosen LSB duration. The accumulated error until a certain bin is the integral non-linearity (INL).

### C. Sources of Static Non-Linearity

Some non-linearity is static, which can be measured at system start-up and stored. This static non-linearity is caused by the chip structure, clock distribution, and the local transistor properties. Exploring this structure and other factors presents information about the sources of non-linearity. For example, the interconnect between elements of different slices creates a larger delay than intra-slice connections. Every fourth element is therefore expected to have a slightly larger DNL. Additionally, regular non-uniformity in the structure of the slices themselves may cause regular distortions in the TDC's measured DNL. For example, Fig. 7 shows that the DNL seems to fluctuate between 1 and −1; this is likely caused by structural differences in each stage's carry propagation or coupled logic, such as transistors facing opposite directions between different stages within the carry element. Other work has shown it is possible to address this issue [18].

Virtex-6 FPGAs are divided into different clock regions. Skew is minimal between slices in the same region, with the intra-region variation between different slices roughly 2–4 ps. However, inter-region skew can be hundreds of picoseconds. A visualization of clock delay is given in Fig. 3. The clock skew will directly influence the result, as the registers are driven by the clock. Fig. 4 shows the clock skew through the clock distribution network. Poorly placed delay lines will have codes with poor DNL, though the LSB duration will show little change. For this reason, clock region crossings need to be avoided in the placement of the delay line. Therefore, a high frequency clock is required, as high frequency reduces the size of the delay line required to fit in one balanced clock region. A clock of 600 MHz and an LSB duration of 10 ps results in no codes with DNL larger than 2.5 LSB.

*1) Position Effects on Non-Linearity:* Process variations cause the properties of fabricated transistors to differ from transistor to transistor. The effect of the intra-chip position on the TDC non-linearity is observed by measuring the TDC performance at different locations. 161 TDCs were placed and tested one by one; Fig. 6 show the resulting DNL and INL. The optimal TDC location is determined in the y-direction
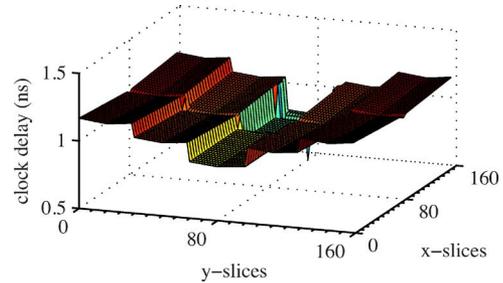


Fig. 3. Visualization of on-chip clock regions.
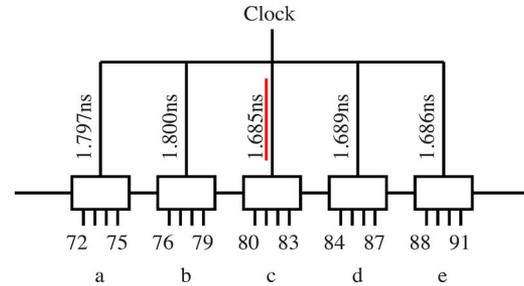


Fig. 4. Clock distribution to the different slices of the FPGA, with clock delays displayed at the interconnect. From b to c, large clock skew will lead to large and unwanted non-linearity.
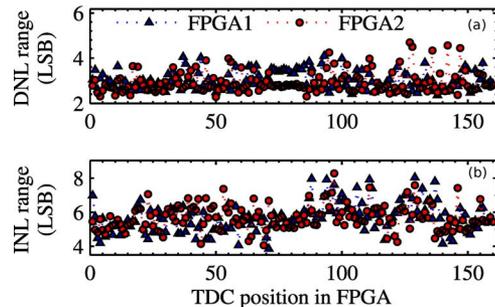


Fig. 5. Non-linearity: (a) DNL and (b) INL ranges versus intra-FPGA position.

by finding the clock regions with the least clock skew. The x-placement of the TDC was varied to observe the positioning effect. The first clock region crossing causing a large DNL can be observed around y = 80. The second crossing at y = 160 has a smaller effect on the DNL, but is also present for temperatures below 60°C. Fig. 5 shows the INL swing as a function of position. The INL swing varies from around 8 LSB to less than 4 LSB, with a mean of 5.7 LSB. There is also more variability in the first half of the positions, caused by the fact that the clock regions are not symmetric, previously shown in Fig. 3.

From these results it is clear that the position of the delay line is important. An implementation of the TDC at the position with the lowest INL swing was tested, and the results are shown in Fig. 7. This plot shows that an INL range of 3.86 LSB can be obtained with a LSB duration of 9.8 ps.

Two different FPGAs were tested for their performance and position dependence, in order to see if the result is applicable for other boards as well. The TDCs were placed in the exact same way on a second FPGA, and the resulting non-linearity was measured. The results of both boards are subtracted from

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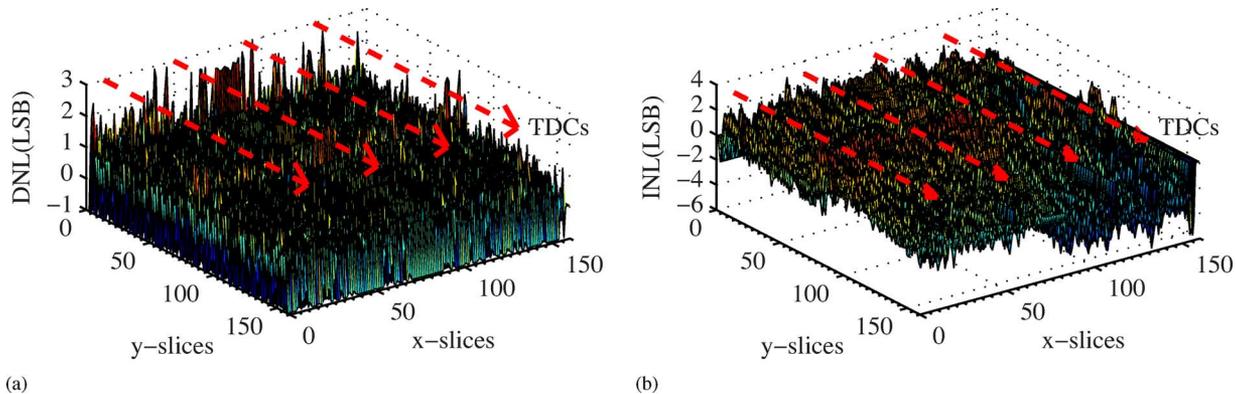


Fig. 6.   Position-dependence of non-linearity for 161 TDCs, each with 165 elements, from a single FPGA. The propagation of the start signal along the delay line is indicated by the arrows; the TDC position changes orthogonally to this propagation.
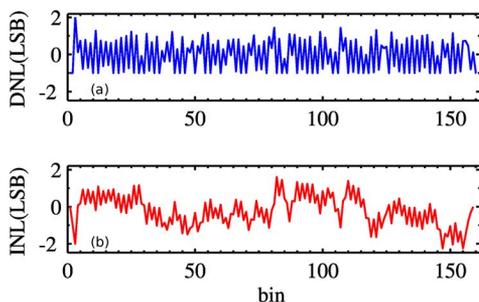


Fig. 7.   Non-linearity for the best TDC. (a) DNL and (b) INL for the TDC with the lowest INL range.
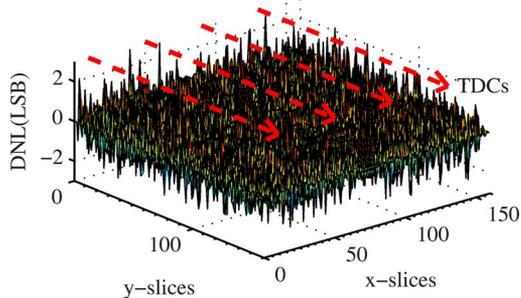


Fig. 8.   DNL differences between two FPGAs are plotted as a function of position, with 161 TDCs compared. The start signal propagation along is indicated by the arrows.

each other and presented in Fig. 8. The mean DNL variation between the two chips is only 0.02 LSB, implies that similar results can be obtained using different chips, though the large variation in some specific DNL values, reaching nearly $-2$ or $>2$, means that compensation for DNL values will be chip-specific.

### D. Dynamic Origins of Non-Linearity

While measuring time intervals, the environment conditions may change. Dynamic influences include shifts from both voltage and temperature. A standard deviation in voltage was observed to be at most 3 mV during one test, implying that voltage fluctuations cannot be measured without modification to the motherboard. Temperature variations across the chip were measured by changing the external temperature. For an arbitrary position, Fig. 10 show the resulting non-linearity as a

function of temperature. The changes in temperature will affect the propagation speed of the delay line, and therefore the LSB duration; higher temperatures will imply a worse LSB duration. At $10°C$ the LSB duration is 9.8 ps and at $60°C$ the LSB duration will be slightly above 10.8 ps. Another phenomenon besides the LSB duration shift can be observed in the figure as well; there is a switch in the order of the plotted lines around bin 120. This appears to be caused by the clock distribution's temperature dependence, as this bin's associated logic occurs next to a clock region crossing.

For applications with high throughput or multiple channels, the effect of multiple TDCs on the same chip must be characterized. Delay lines close to each other might have some effect on the performance and non-linearity. To test this, an the implementation with just a single TDC and one ring of logic-free slices around the delay line was implemented. A second implementation without such a guard ring was also tested; this implementation consisted of three consecutive TDCs with the same start signal. The result of a standalone TDC and parallel TDCs without separation is shown in Fig. 9. During this test the temperature was kept constant using a temperature chamber, with three different test runs made per implementation. The required length of the delay line can be estimated by dividing the clock period by the LSB duration, with the length ranging from 171 elements at $10°C$ to 160 elements at $60°C$. The consecutive delay lines show average DNL shifts of more than 0.2 LSB across several consecutive codes. Since the density test sigma is less than 0.04 LSB, this implies a statistically significant shift in the measured time. The distortions do not appear in the tests for the single TDC. The measurement to measurement variation is shown in Fig. 9. When a guard ring of one slice is included, the effect is reduced. Guard rings solve the problem of surrounding logic influences, though at the cost of missing area.

### E. Measurements of Known Time Differences

To characterize the uncertainty and uniformity with known time differences, a two-channel TDC implemented on an ML605 board at room temperature measures the rising and falling edge of pulses ranging from 40 ns to 1.28 $\mu$s. These pulses are generated with a 200 MHz oscillator from a different ML605 board. Samples of the pulses with a LeCroy WaveMaster oscilloscope showed sub-10 ps jitter and a fixed

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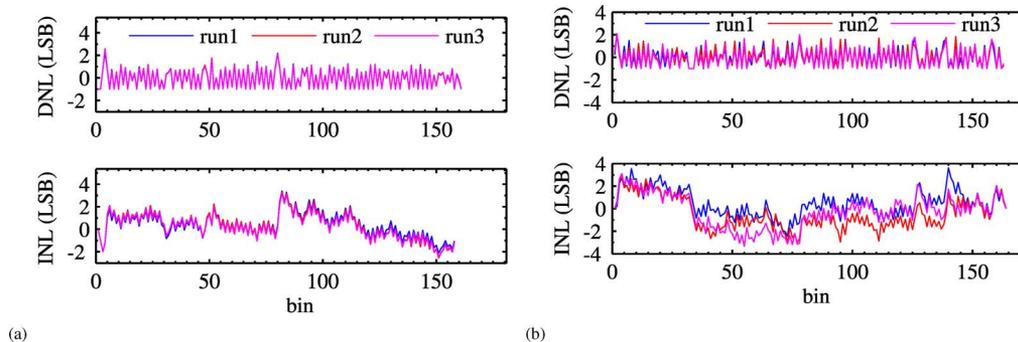


Fig. 9. Characterization results of multiple on-chip TDCs with (a) stand alone TDC and (b) a parallel placed TDC with guard slices.
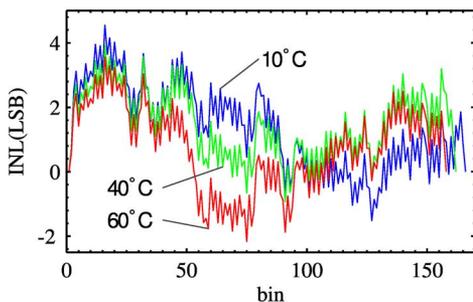


Fig. 10. Temperature behavior of the best TDC, and the corresponding variation in LSB duration, temperature, and voltage.
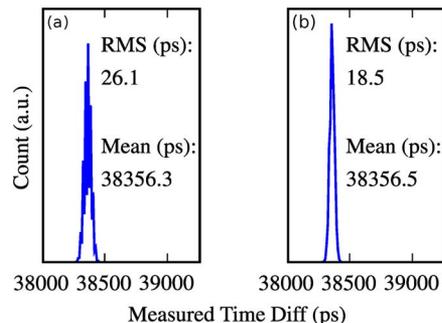


Fig. 11. Measurement histograms of input time differences of 40 ns for (a) raw and (b) DNL-compensated data.



Fig. 12. Single-shot jitter versus. input time difference.

offset of 185 ps. Fig. 11 shows the measured durations of 40 ns pulses for both the raw output times and the output times following compensation for the TDC's DNL. At an input of 40 ns, the standard deviation of the measured delay is 26.1 ps for the raw data and 18.5 ps when compensated for the DNL for acquisitions below one second. For ten 2-second acquisition occurring over the course of several minutes, the standard deviation increased slightly to 19.6 ps at 40 ns, with similiarly small increases at the other time differences. Fig. 12 shows the final measured RMS values from these 10 experimental runs occurring over several minutes. The standard deviation of the measured delay increases with the input time difference, being roughly 320 ps for input pulses of duration 327.7 $\mu$s. The increase in jitter appears to follow three regions—below 1 $\mu$s the on-FPGA clock generator's jitter is expected to dominate, between 1 $\mu$s and 1 ms the jitter will be a mix of the on-FPGA clock generator and the reference oscillator, and above 1 ms the jitter is expected to follow that of the reference oscillator. All measured input time differences exhibit a 423 ps offset from expectations, which is presumably due to routing difference between the start and stop signals, with a 9 ppm dependence on the input time difference. The 9 ppm dependence may be caused by the crystal oscillators used in both the generating and the measuring systems; such oscillators often age with a shift of a few ppm per year.

By routing the coarse clock through external cables to be the stop signal, in other words in a loopback configuration, an upper bound can be placed on the clock-free jitter, which is the jitter accumulated as the signal propagates along the delay line. By changing the length of the external cables, this measurement can occur early and late in the delay line. The jitter (sigma) that the delay line introduces at room temperature is measured to be at most 7.38 ps (0.74 LSB) for the initial codes, and 14.24 ps (1.42 LSB) for the final codes. Ignoring any differences from cable length, and assuming i.i.d. normal distributions for each element, the standard deviations of the elements will add in quadrature. The combined std. dev. $\sigma_{\mathrm{element}}$ of the 166 elements will be roughly $\sqrt{160\sigma_{\mathrm{element}}^2 + (7.4\,\mathrm{ps})^2} \approx 14.24$ ps, implying an element std. dev. of, at most, roughly 0.96 ps. It is not clear how much of this single element jitter accrues from propagation along the delay line compared to the increase in cable length; while such jitter might be a factor in the total jitter for input time differences below 60 ns, it is inconsequential compared to the clock jitter for measurements of durations larger than 100 ns.
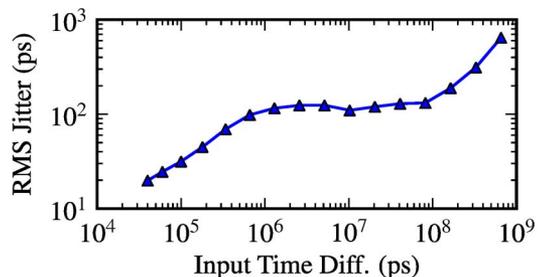
### F. Code Availability

A modified version of this two-channel TDC for Xilinx's ML605 board, along with the source code for the read-out system but not the TDC itself, is available upon request. The

modified version of the TDC is coupled to a soft-core processor which provides a TCP/IP interface for communication.

## IV. Conclusion

Results show that sub-20 ps RMS time uncertainty, sub-40 ns range TDCs can be implemented in a Virtex-6 FPGA with high reliability and uniformity. The input range can be increased beyond 100 $\mu$s, with an increase in RMS time uncertainty below 400 ps. The static and dynamic non-linearities of both single- and multi-channel versions of the TDC were characterized. Static non-linearity dependencies due to architecture, clock distribution, and chip position were investigated and optimized. Dynamic non-linearity dependencies due to temperature, voltage, and environmental influences were presented. The final results show a FPGA-based TDC with sub-11 ps LSB duration, 300 MS/s expected throughput, $[-1, 1.5]$ LSB DNL and $[-2.25, 1.61]$ LSB INL can be realized. Initial tests show that there is high uniformity between two tested FPGAs, though further results are required to see if this trend holds across all devices. A single-channel TDC is fully implemented and a multiple-channel TDC is freely available for download. The proposed TDC can be applied in a wide range of applications, besides PET, where high throughput, sub-100 ps accuracy and fast processing speed are required.

## Acknowledgment

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