Reverse Biasing and Breakdown Behavior of PureB Diodes

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1. Introduction

In PureB technology, a layer of pure boron is deposited on Si using a commercial single-wafer Si/SiGe epitaxial CVD reactor, forming ideal nm-deep ultrashallow junctions with low saturation currents [1]. As another attractive feature, the PureB layer itself has proven to be a robust front-entrance window for photodiode detectors for low penetration-depth beams such as DUV [2], VUV [2] and EUV [3] light, and low-energy electrons [4]. For all these applications, PureB detectors have been commercialized, mainly in the form of small clusters of millimeter-large photodiodes operated at moderate reverse biasing. Under these conditions the performance of these photodiodes surpasses that of other existing technologies on points such as internal/external quantum efficiency, dark current and degradation of responsivity. Both the optical and electrical degradation is related to the properties of the oxide interface at the perimeter of the diodes [3]. The depleted region at the interface should be kept as small as possible. This is commonly achieved by implementing implanted p-type guard rings and n-type channel stops [5]. The p-guard is also used to reduce the surface curvature in the doping near the device edge that otherwise can cause premature edge breakdown.

In this paper, the reverse biasing and breakdown properties of the PureB diodes are investigated for different methods of processing the PureB anode window and the metal contacting. In particular, micron-sized devices are examined in order to assess their suitability for use in dense imaging arrays that may require operation as avalanche photodiodes to obtain the necessary photosensitivity [6]. For such small devices implanted guard rings cannot be implemented without paying a penalty in fill-factor. At the same time it is also desirable to position the photosensitive area away from the oxide perimeter where permanent damage can be inflicted by high reverse currents. Therefore, a "virtual" guard, using an n-enhancement implantation in the central region of the diode is applied here.

2. Device Fabrication

The basic process flow is shown in Fig. 1. All experiments are performed on n-type Czochralski (100) 1-10 Ω·cm Si substrates both with and without an intrinsically-grown epitaxial layer. A thermal oxide is grown, either 30-nm or 300-nm thick, though which heavily-doped p^+ guard rings, n^+ channel-stops or n-enhancement regions are optionally implanted and annealed at 950 ℃ for 20 min. The wafers with 30-nm oxide are then covered with 300-nm LPCVD TEOS oxide.

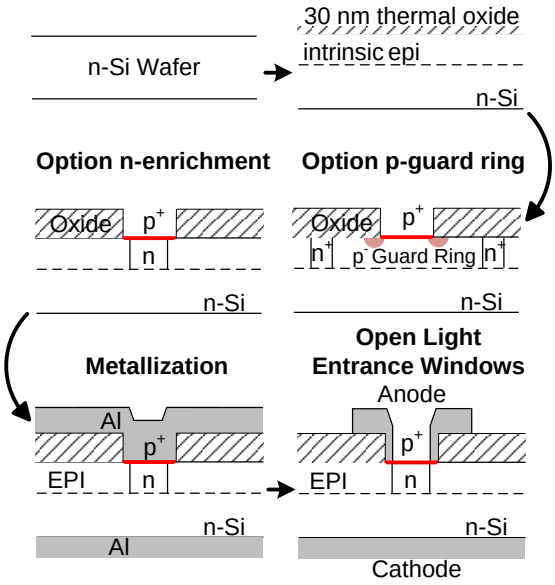

Fig. 1. Schematic process flow for fabrication of PureB diodes showing two options: one a virtual guard ring using an n-enhancement implant, and the other a p-type guard ring and n^+ channel-stop, both in an intrinsic epi-layer.

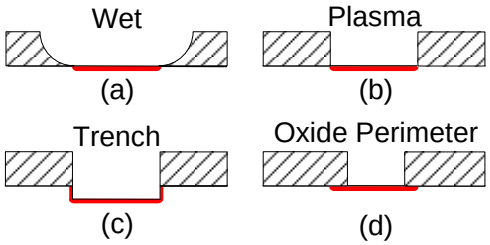

Fig. 2. Schematic of 4 different methods of etching and filling the PureB anode windows.

Four different methods of processing the PureB anode windows are illustrated in Fig. 2. The windows to the silicon are etched through the oxide either entirely wet, by plasma etching with soft- or wet-landing, or by plasma etching about 1 μm into the Si. The native oxide is removed by dip etching in 0.55% HF and Marangoni drying, followed by the deposition of a 2.5-nm-thick PureB layer in the ASM Epsilon 2000 reactor at 700 ℃. The PureB is thereby self-aligned to the anode window. On some wafers the anode window is covered by 100 nm oxide and after this contact, windows to the PureB, a few micron from the anode perimeter, are etched in 0.55% HF. For contacting the anode, a 675-nm pure Al is sputtered at 350 ℃ and the back of the wafer is also sputtered with Al to form the cathode contact. After anode interconnect patterning, the entrance windows to the photosensitive areas are opened

first by plasma etching the Al back to 100 – 200 nm. This thin Al layer is then removed by wet etching in HF 0.55% for 3 to 5 min, selectively to the PureB layer. Lastly, a 400 ℃ alloy step in forming gas is performed to improve the contact between the metal and the PureB layer and to passivate the oxide interface. An overview of the fabricated diodes is given in Table I.

The electrical I-V diode characteristics are measured at room temperature. The current compliance is set at 10 μA for the breakdown measurement.

Table I. List of the measured PureB diodes indicating the different process variations

Device	Epi	Geometry	Guard ring	Anode window etch
Dg(intr,pl)	10 μm intr	diameter = 3.6 mm	p- + n^+ ch-stop 2.5 μm apart	plasma
D(intr,wet)	10 μm intr		no	wet
D(oxide)	no		no	wet + oxide perimeter
D(pl+wet)	no	300×315 μm^2	no	plasma + wet
D(trench)	no		no	trench
Dn(intr,pl)	1 μm intr	various diameters	n-enrichment	plasma
Dn(1e16,pl)	1 μm 10^{16} cm^{-2}	various diameters	n-enrichment	plasma

2. Large diodes with/without implanted guard rings.

To meet the speed requirements for detector read-out, a low capacitance and series resistance are often achieved by growing a lightly-doped epitaxial Si layer on a more heavily-doped substrate. For large PureB photodiodes the studies up until now have been devoted to the design of guard rings to optimize the trade-off between capacitance and leakage current [7]. It has been shown that the depleted region at the oxide interface is the source of both leakage and degradation during exposure to radiation [3].

In Fig. 3 the I-V characteristics of 3 large diodes, Dg(intr,pl), D(intr,wet) and D(oxide), are compared. All three have high breakdown, which for the Dg(intr,pl) is lowest due to the small distance between the n- and p-guard. For the device D(intr,wet), with the anode window entirely wet-etched and no p-guard, the saturation current is almost 2 decades higher than for the plasma etched windows. This difference is reproducible over the wafer and from run to run. Since the Gummel number of the substrate, which governs the hole injection current, is the same in all cases, it must be concluded that electron injection from the substrate to the p^+-region at the diode perimeter is responsible for this behavior. This could be explained in terms of the very thin tapered oxide that surrounds the PureB region: this could give a very small distance between the metal and the doped Si, reducing the edge Gummel number of the p^+ region and increasing electron injection into the metal. Otherwise, a very high effective Gummel number corresponding to a p^+-doping of about $10^{15}/cm^2$ is created at the PureB-to-Si interface [8].

In Fig. 4 I-V characteristics are compared for the devices D(pl+wet) and D(trench). For the latter the breakdown voltage is decreased, presumably because the trench in which the PureB is deposited has corners where the electric field will be higher than for the flat structure. Nevertheless, the breakdown is high and reproducible over the wafer and from wafer to wafer.

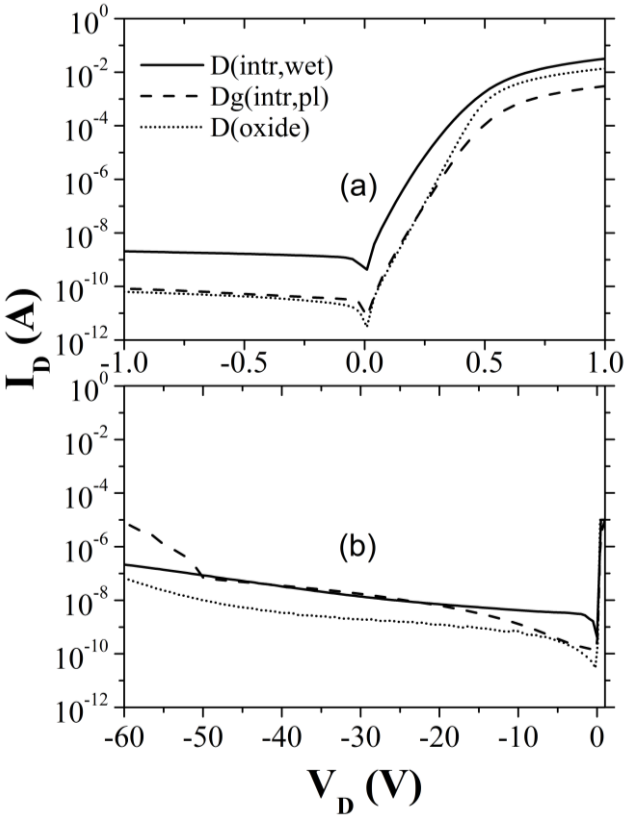

Fig. 3. I-V characteristics of 3 large diodes fabricated in different ways, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diameter of the diodes is 3.6 mm.

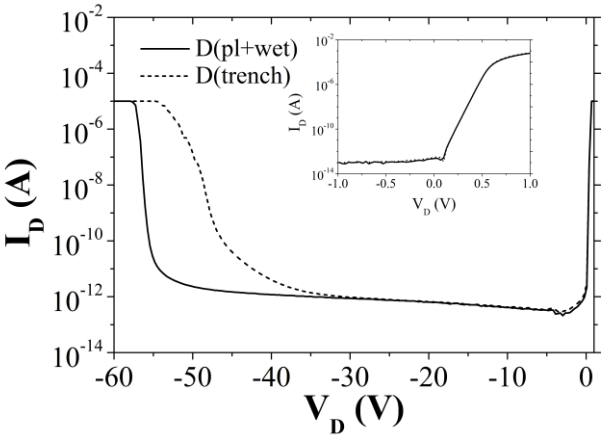

Fig. 4. I-V characteristics of diodes with where the anode window is opened in two different ways, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diodes have an area of 300×315 μm^2.

3. Small diodes with n-enhancement implantation

From the results presented in the previous section it is clear that the PureB diodes have reliable reverse biasing/breakdown behavior for a variety of anode window configurations, independent of whether there is a p-guard

ring or not. For micron small photodiodes to be used in avalanche mode, it is therefore possible to apply a virtual guard to move the breakdown point away from the perimeter in order to acquire a large active region in the center of the diode. This is achieved here by a phosphorus n-enrichment implantation placed in a lightly-doped epi-layer 1.5 µm away from the edge of the anode. Round diodes are used to avoid the high electrical field at the junction corners.

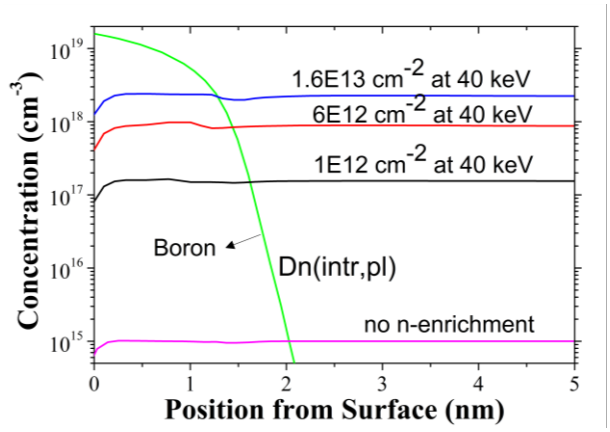

Fig. 5. Simulated doping profiles in the Si as a result of a 6-min PureB deposition at 700 ℃ on an n-epi layer with doping 10^{15} cm^{-3}, and 3 different phosphorus implantations at 40 keV added to an implantation at 300 keV to a dose of 5×10^{-12} cm^{-2}. The situation with no n-enrichment is also shown for comparison. The boron is diffused from a constant surface concentration of 2×10^{-19} cm^{-3}.

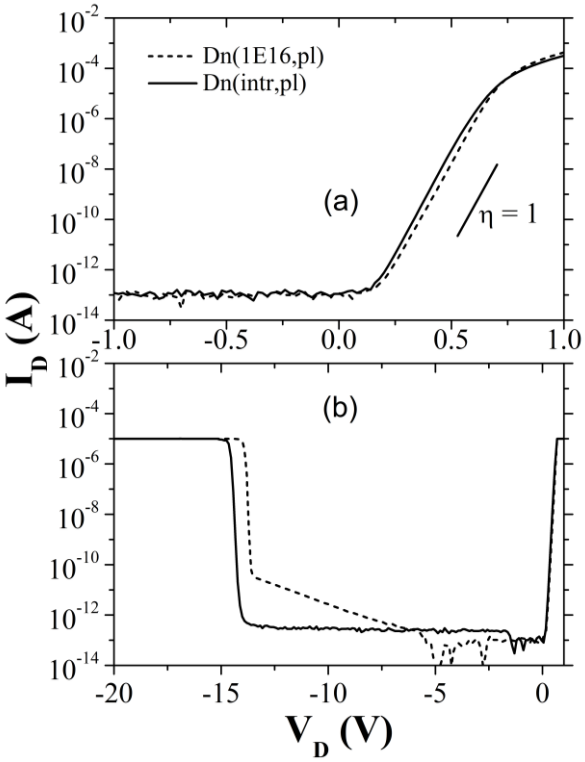

Fig. 6. I-V characteristics of two diodes with different epi-layer doping concentrations and an n-enrichment implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diameter of the diodes is 8 µm.

For the n-enrichment several implant doses are used, the simulated doping profile of which are shown in Fig. 5. Since the PureB is diffused into the Si at only 700 ℃, the boron doping profile only extends about 2 nm into the Si.

In Fig. 6 the influence of the epi-doping on the I-V characteristics is compared for the devices D(intr,pl) and D(1e16,pl) with 1 µm intrinsic or n-doped epi (10^{16} cm^{-2}) and a light n-enhancement implant. In the former case, due to phosphorus up-diffusion from the n-Si substrate and the background doping of the epi-reactor, the epi-layer will also be n-doped to an estimated concentration of around 10^{15} cm^{-3}. Both diodes have very good forward characteristics and the reverse I-V characteristics display abrupt breakdown in both cases. For the diode with the intrinsic epi-layer, the reverse current is below the noise floor until the onset of avalanche breakdown, while for the diode with the 10^{16} cm^{-3} epi-layer, the reverse current is higher and increases with increasing bias voltage. With the higher electrical field in this case, trap-assisted tunneling at the oxide interface is more likely to occur and this leads to a steady increase of the leakage current. To minimize the peripheral electrical field, a low-doped epi-layer is preferable.

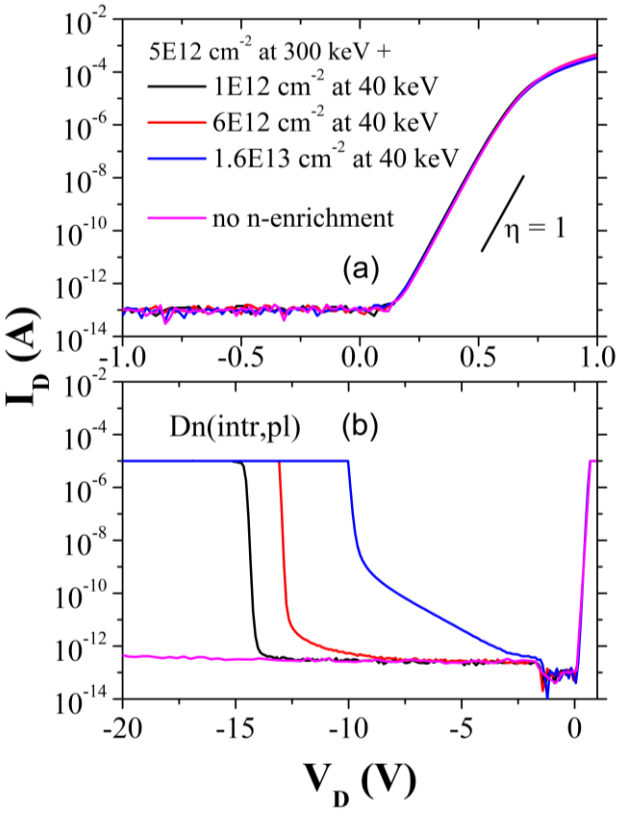

Fig. 7. I-V characteristics of a set of Dn(intr,pl) diodes with different n-enrichment implantations, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diameter of the diodes is 8 µm.

As seen in Fig. 7, where the influence of the n-enhancement implantation dose is displayed, the forward I-V characteristics of diodes with a diameter of 8 µm are all very good while the reverse characteristics show an increasing leakage current and decreasing breakdown

voltage with increasing implantation dose, suggesting the breakdown is taking place between the junction and the n-enrichment region. With no n-enrichment, the reverse current stays below the noise floor. The sharpest breakdown is observed for the lightest implantation dose of 10^{-12} cm^{-2} at 40 keV added to a deeper implant of 5×10^{-12} cm^{-2} at 300 keV. This is the type of abrupt breakdown desired for detecting single avalanche events.

In Fig. 8 the I-V characteristics are shown for diodes with diameters from 8 µm to 20 µm. The leakage increases with the area, rising above the noise floor and the breakdown becomes less abrupt but still occurs at the same voltage. It is probable that the increase in leakage is related to the increase in the length of the perimeter and depends on the oxide interface quality and the exact epi-doping.

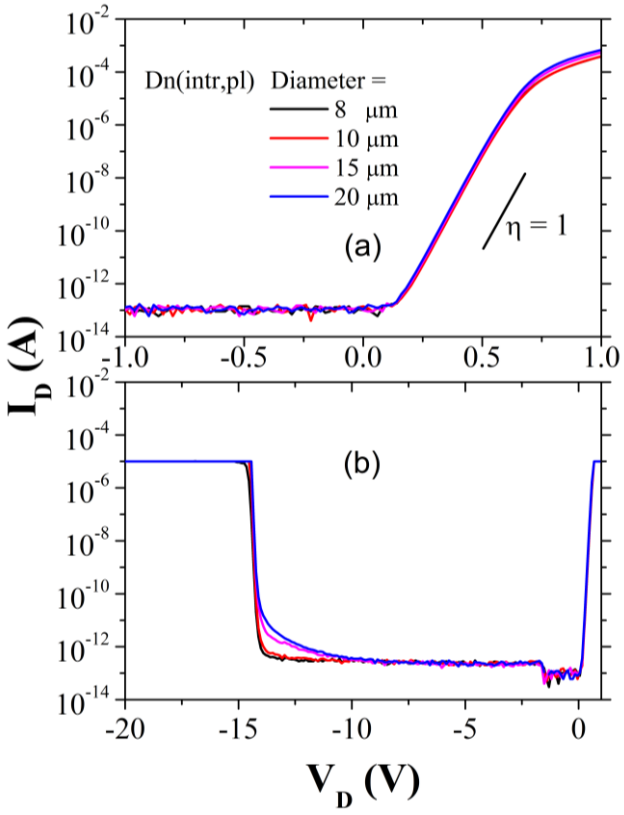

Fig. 8. I-V characteristics of a set of Dn(intr,pl) diodes with different diameters (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The n-enrichment implantation is 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV.

4. Conclusions

The reverse current measurement of the large number of PureB diodes studied here with different anode window geometries and different configurations of guard rings or n-enhancement implantations show that although the PureB anode forms a p-doping of the Si that is only about 2 nm deep, the leakage currents and breakdown voltage are determined by the doping of n-Si and/or the depletion of the oxide interface at the diode perimeter. Even in the cases without guard rings or trench-etched anode windows, the PureB perimeter coverage is complete and allows high breakdown voltages. For the small round diodes with a diameter of 8 µm made with intrinsic epi and an n-enrichment implantation in the central region, a very abrupt breakdown is achieved of the type that is suitable for photodiode operation in avalanche mode. All in all, these small diodes are promising for fabrication of imaging arrays with high fill-factor, nm-thin front-entrance windows and associated high sensitivity to beams that only can penetrate a few nm into the Si. The demonstrated abrupt breakdown behavior also holds promise for applications requiring diodes that work close to or beyond the avalanche breakdown voltage as, for example, Single-Photon Avalanche Diodes (SPAD) [9].

Acknowledgments

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