An Optical Punch-Through Diode and Gate Biasing 1-T Pixel for Binary Pixels in Fully Digital CMOS Image Sensors

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Abstract–*An optical punch-through diode and 1-T pixel CMOS image sensor are presented as a potential candidate for binary pixels and multi-bit digital pixels in a fully digital image sensor, such as the gigavision camera or the digital film concept. The optical punch-through diode was tested varying the depletion width in the n/p-/n structure. The prototype chip with 4×4 pixel array was implemented in a 65nm CMOS standard technology. Another prototype chip with 300×90 1-T pixel array and 300×90 typical 3-T pixel array was implemented in 180nm CMOS image sensor technology. Both the prototype chips were tested with high-speed laser illumination and halogen lamp respectively. In the optical punch-through diode, a time uncertainty of 332psec FWHM (Full Width at Half Maximum) was measured with 1.2V operating voltage. The 1-T pixel CMOS image sensor had 2.8797×10^{-3}V/(lux•sec) light sensitivity with 3.26msec accumulation time, which is 8 times higher than that of a typical 3-T pixel sensor.*

In the digital film concept [1, 2], it is desirable that pixels have high photon conversion gain. To enable high spatial oversampling ratios, the pixels should have nanometric dimensions, while a fast response is necessary to enable high temporal oversampling ratios. These are contradicting requirements, even though, in principle, conventional p-n photodiodes could achieve some of them individually. In this paper we propose two potential candidates for the digital film concept pixel. One is an optical punch-through diode that could potentially fulfill nanometric pitch, high conversion gain, and high-speed constraints, simultaneously. The structure is based on the punch-through breakdown mechanism [3, 4], which causes the drain current to increase rapidly with only a small increase in drain voltage. The other candidate is a gate biasing 1-T pixel designed for use in the digital film concept. The 3 state operations – accumulation, readout, and reset – are controlled by the gate biasing voltages and the gate biasing in the readout state makes it possible to increase the light sensitivity in the high speed operations.

Optical Punch-Through Diode

Fig. 1 shows a space charge in the transition region of the proposed punch-through diode for an optical device. The basic idea of the proposed optical punch-through diode is that the electrons generated by light illumination makes flat the potential barrier in between p-n junction and the photo-electrons become a trigger to generate punch-through breakdown like as MSM (Metal-Semiconductor-Metal) photodiode [5]. There are two necessary conditions to create the optical punch-through diode: a very narrow and lightly doped p-type region between two n-type regions, as shown in Fig. 1. A reference bias is applied to the punch-through diode structure with the conditions to generate a fully depleted p-type region for a drifting operation.

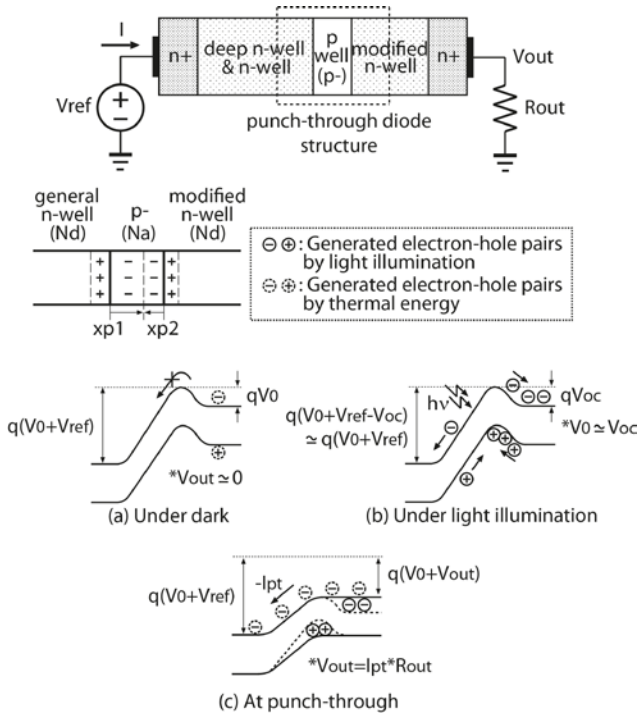


Fig. 1. Space charge in the transition region of the proposed punch-through diode with n/p-/n structure for optical device. Energy band diagrams for each step, (a) under dark, (b) under light illumination, (c) occurring punch-through breakdown with readout resister.

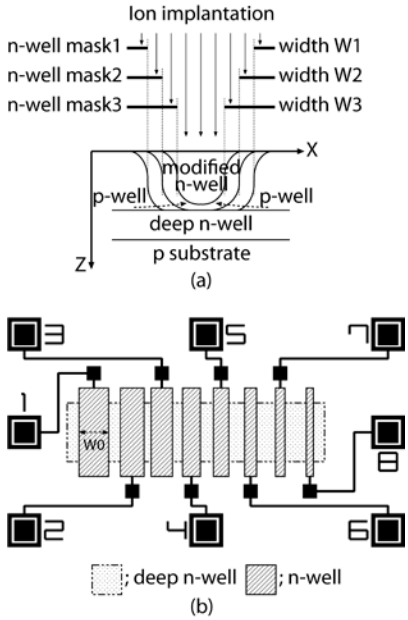


Fig. 2. (a) A cross-sectional profile of n-well implantation and (b) a schematic of the test pattern.

Fig. 2 shows a cross-sectional profile of n-well implantations and a schematic of the test patterns to find the best condition to generate the narrow and low-doped p-type region for the optical punch-through diode in a CMOS standard process. W_0 is the minimum width of n- well in the design rule of a 65nm standard CMOS process.

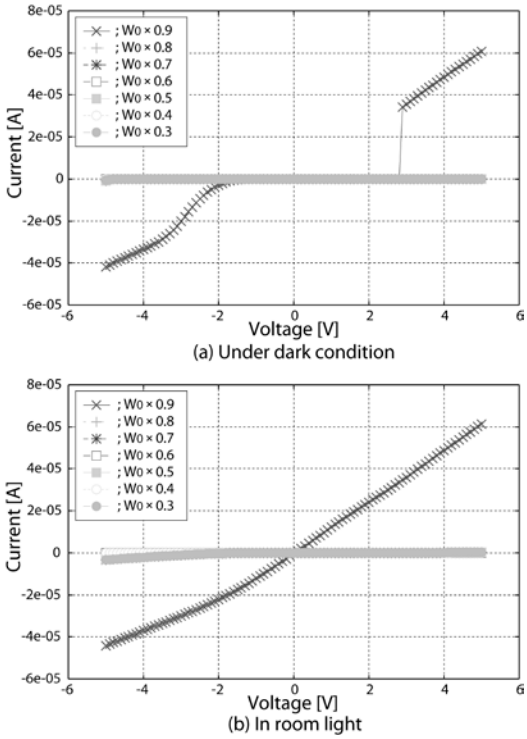


Fig. 3. I-V characteristic of the test pattern (a) under dark condition and (b) in room light.

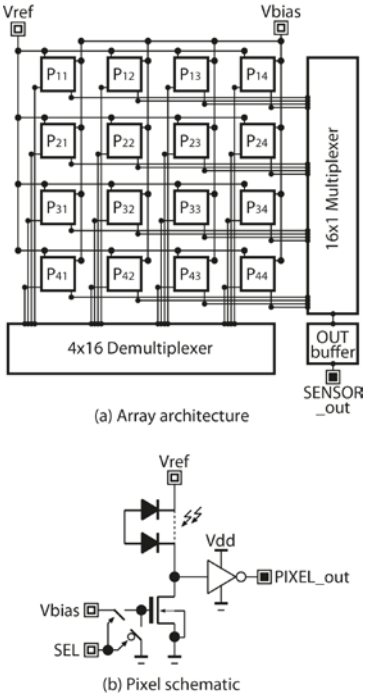


Fig. 4. (a) An array architecture and (b) a schematic of the unit pixel of the prototype fully digital image sensor array with the optical punch-through diode.

Fig. 3 shows the I-V characteristics of the test pattern under dark condition and in room light. As shown in Fig. 2, the currents between pad no. 1 and other pads were measured with varying voltage. Because of the risk of design rule violation, the modified n-well under the minimum width of the design rule was apparently allowed to shrink 10 percent of the minimum width; W_0. The optical punch-through diode is working as a photo-resistor in light illumination whereas the optical punch-through diode is working as a normal punch-through diode in dark.

Fig. 4 is a block diagram of the prototype digital CMOS image sensor array with 16 different structures of the punch-through diode with a schematic of the unit pixel. 1.2V was used for operating voltage for both pixel and circuits.

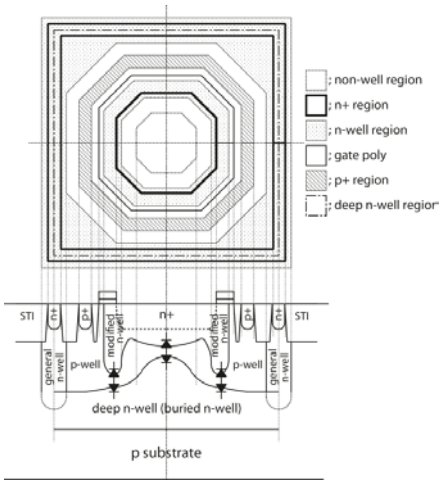


Fig. 5. A cross-sectional view of the succeed pixel in the prototype fully digital CMOS image sensor.

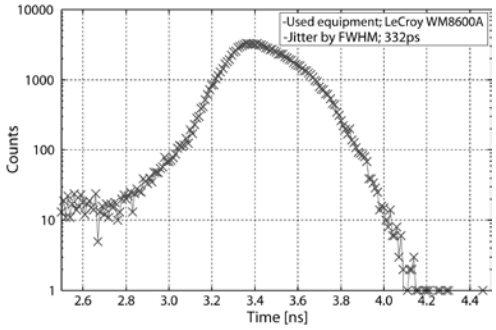


Fig. 6. Histogram of the timing jitter between the laser output trigger and the optical sensor output with the punch-through diodes receiving digital pulse in log scale.

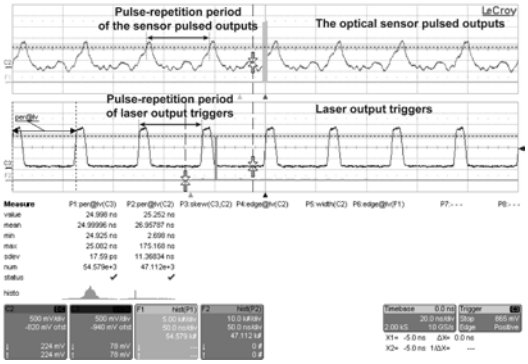


Fig. 7. Waveforms of the pulsed output of laser trigger and the optical sensor. The pulse-repetition period of laser output triggers was set to 25nsec with 40MHz repetition rate and the output waveforms of laser output triggers were well matched with the set-up.

Fig. 5 shows the best pixel structure among the 16 different pixel structures. For the modified n-well, W_0×0.9 was chosen and non-well region was added in the center of the active region.

To check the transition speed, the prototype sensor was employed to a timing jitter test with a 40MHz laser sources at 637nm wavelength. Fig. 6 shows a histogram of the timing jitter between the laser output trigger and the optical sensor output with the pixel structure in Fig. 5. The jitter by FWHM was 332pses in the measurement. A pulse-repetition period is the time it takes for a pulse to recur. The pulse-repetition period of the trigger input for the laser of 40MHz were measured at 25nsec in Fig. 7.

Gate Biasing 1-T Pixel CMOS Image Sensor

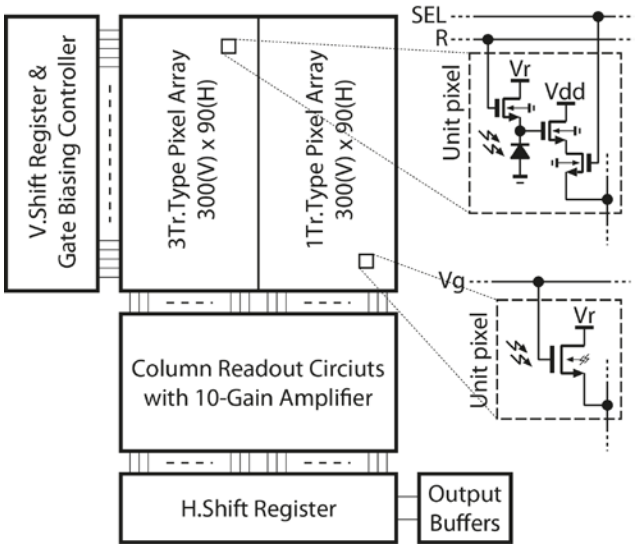


Fig. 8. Block diagram of the 1-T pixel CMOS image sensor. To compare the functions of the 1-T pixel sensor, a typical 3-T type pixel array was also desinged together with the 1-T pixel on the same readout and selecting circuitries. Both 1-T pixel and 3-T pixel array have 300(V) × 90 (H).

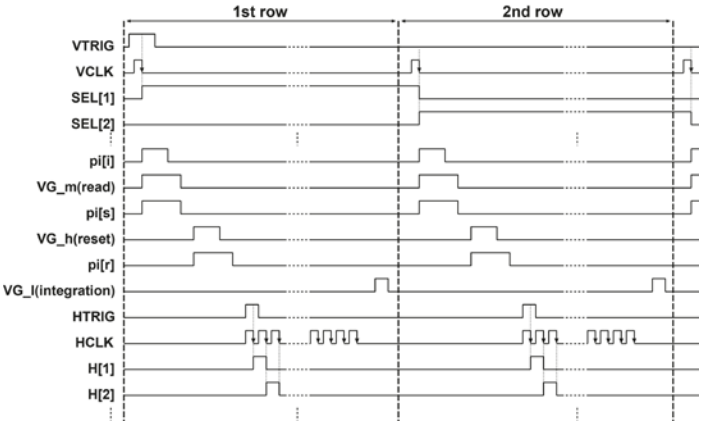


Fig. 9. Timing diagram for the 1-T pixel CMOS image sensor operation. The 1-T pixel has three operating states such as accumulation stage with VG_l, readout state with VG_m, and reset state with VG_h achieved by proper biasing of the gate using a vertical shift register with the gate biasing controller.

Fig. 8 and Fig. 9 show the block diagram of the prototype CMOS image sensor and timing diagram for the 1-T pixel operation. To compare the functions of the 1-T pixel sensor, a typical 3-T pixel with p-n jucntion diode based photodetector was included in the prototype sensor design. Both the pixel types have 300(V) × 90 (H) pixel array and the outputs of each row are sequentially fed to a column noise canceling amplifier with 10 internal gain and the signal is read out through horizontal scanning.

The 1-T pixel operation referred in the previous result [6] has three different states for the accumulation, readout, and reset operations as shown in Fig. 9. In special, the midium gate biasing voltage in the readout state is able to increase the sensitivity of the light illuminaiton by a boosting mechanism.

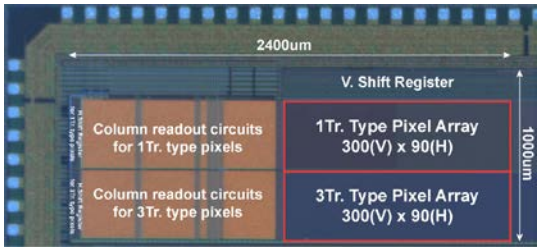


Fig. 10. Chip microphotograph. The size of both the pixels was 3.5µm×3.5µm; the active pixel size of 1-T pixel was 2µm×2µm whereas the active pixel size of 3-T pixel was 3.5µm×3.5µm. 0.18µm CMOS image sensor technology used for the chip implementation.

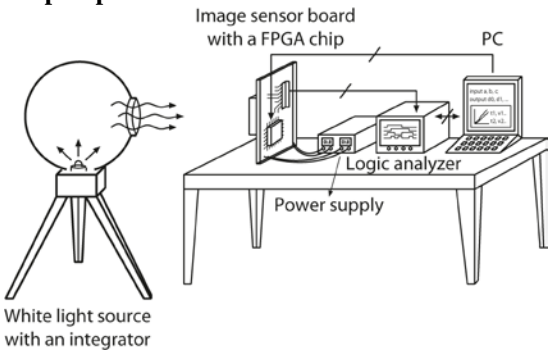


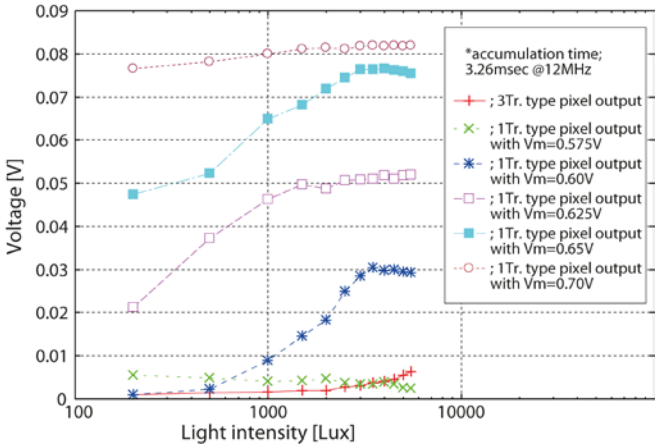
Fig. 11. Measurement system. A halogen lamp with light integrator was used for the light source.

Fig. 10 shows a microphotograph of the prototype CMOS image sensor chip with 1-T and 3-T pixel and it was implemented in a four-metal and one-poly 0.18µm CMOS image sensor technology. Both the pixel sizes were 3.5µm×3.5µm; the active pixel size of the 1-T pixel was 2µm × 2µm whereas that of the 3-T pixel was 3.5µm×3.5µm. A microlens array and color filters were not generated on the pixel array.

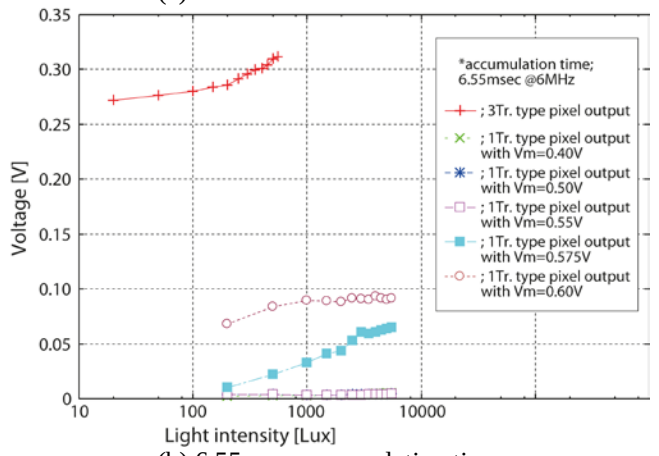
A measurement system for the imaging sensor is shown in Fig. 11. For the light source, a halogen lamp with light integrator was used for both the CMOS image sensor measurement. All control pulses were generated by an FPGA. The signal output was digitized with 14-bit analog-to-digital converter, and the output data were stored in a logic analyzer with a large size memory. The digitized output was also fed to a desktop personal computer for data and image processing.

Fig. 12 shows the measured photo-conversion characteristics of both the CMOS image sensor with 1-T and 3-T type pixel. For the 1-T pixel test, the gate biasing voltage in the readout state was varied to increase the light sensitivity. As shown in Fig. 12, the accumulation time was set to 3.26msec, 6.55msec, and 27.29msec by the clock speed.

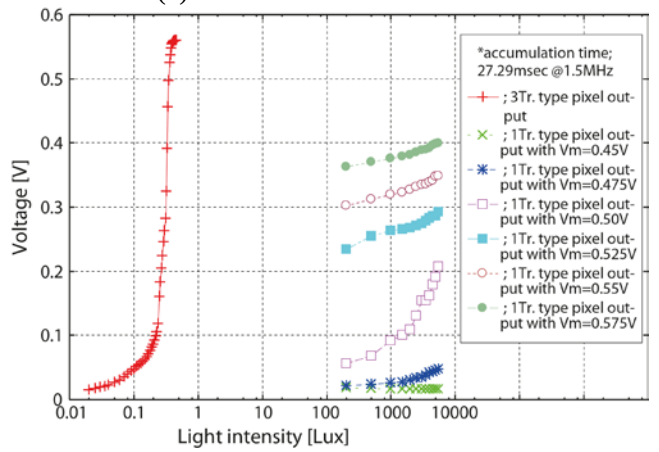
In the 1-T pixel, the 1-T has the photo-detector function as well as select and reset functions. For the photo-detector function, the



(a) 3.26msec accumulation time



(b) 6.55msec accumulation time



(c) 27.29msec accumulation time

Fig. 12. Linearity and sensitivity of both the CMOS image sensor with 1-T and 3-T pixel. For the 1-T pixel measurement, the gate biasing voltage in the readout state was varied to increase the light sensitivity. The sensitivities with different accumulation time by clock speed were measured with (a) 3.26msec accumulation time, (b) 6.55msec accumulation time, and (c) 27.29msec accumulation time respectively.

illumination area is defined as the gate region and it may cause the reason of much less light sensitivity of the 1-T pixel than 3-T pixel with 27.29msec accumulation time for the video rate speed like as Fig. 12(c). Even though a salicide blocking layer was deposited on the gate region to reduce the light reflection, the metal gate itself may become the most reflective source by the light. However, it is interesting note that the light sensitivity of the 1-T type pixel overcomes that of 3-T type pixel in shorter accumulation time like as Fig. 12(a). Moreover, the increase of gate biasing voltage in the readout state, Vm, causes the light sensitivity to increase in the measured results of Fig. 12. The chip summary is presented in Table. 1.

Table. 1. Summary of functions of the chip.

Parameter	1-T pixel	3-T pixel	Comments
Sensitivity	2.8797×10^{-3} [V/(lux·sec)] @Vm=0.625V	0.353×10^{-3} V/(lux·sec)	@3.26msec accumulation time
Sensitivity	1.38×10^{-3} [V/(lux·sec)] @Vm=0.5V	44.519 V/(lux·sec)	@27.29msec accumulation time
SNR	13.72 [V/V] @Vm=0.5V	3.31 [V/V]	@27.29msec accumulation time, @min. light intensity
Conversion gain	3.49×10^{-5} [V/e-]	4.12×10^{-5} [V/e-]	@27.29msec accumulation time, @min. light intensity

Conclusion

Two different pixels for the binary pixels and multi-bit digital pixels in a fully digital image sensor are proposed in this works. Both the chip summaries are represented in Table. 2. By light tests, both the pixel structures are able to be a digital film concept binary pixel and more detail analysis and imaging test will be going on in near future.

Table. 2. Summary of specifications of both the chip.

Parameter	Optical punch-through diode	1-T pixel
Process	65nm standard CMOS process	180nm CMOS image sensor process
Supply voltage	1.2V	1.8V
Remarkable results	Time uncertainty of 332psec FWHM	Light sensitivity of 2.8797×10^{-3}[V/(lux·sec)] ;8.15 times higher than that of typical 3-T pixel @3.26msec accumulation time

References

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