# Stabilizing sensitivity in large single-photon image sensors with an integrated 3.3-to-25V all-digital charge pump

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## Abstract

This paper presents a digitally controlled charge pump (DCP) to supply high voltages, while ensuring temperature and load current independence of excess bias in cameras based on avalanche photodiodes. This is achieved through a single-photon avalanche diode (SPAD) based monitoring mechanism that continuously reconfigures the DCP using a feedback loop to compensate breakdown voltage variations by temperature and load current in real time. The sensitivity of the SPADs, or photon detection probability, is maintained to within 1.9% when the temperature shifts from 28 °C to 65 °C and the load current changes from 0 µA to 100µA.


## Introduction

Single-photon avalanche diodes (SPADs) are used as imaging devices in various fields, including 3-D vision, space exploration and biomedical diagnostics. SPADs need to be reverse-biased several volts above breakdown; these voltages are far beyond the transistor's operation conditions in low voltage CMOS technologies. Charge pumps based on the Dickson architecture are widely used to supply a high voltage proportional to the number of stages [1], [2]; these circuits are ideally suited for a SPAD biasing for bill-of-materials and cost reduction [3], [4]. Fig. 1 shows the concept of a sensor based on a SPAD array with charge pump. The cathode of the SPAD is biased to $V_{op}, = V_{bd}+V_e$, where $V_{bd}$ is the breakdown voltage and $V_e$ the excess bias. During the detection cycle, the anode, $V_{pix}$, reaches $V_e$ in less than 1 ns and returns to ground absorbing a current pulse $I_{source}$(t), upon a photon or thermal event. The width of the pulse is proportional to $V_e$ and the sum of all impulsive currents, $I_{sum}$, is proportional to the illumination brightness; it must thus be guaranteed by the voltage generator under all specified lighting conditions. In addition, the generator must also adjust $V_{op}$ to maintain a constant excess bias when the breakdown voltage changes, due to process and temperature variations, and to account for current absorption variations at $V_{op}$ due to increase of brightness [3], [4]. Maintaining the excess bias irrespective of process, voltage, temperature, and brightness (PVT-B) variations is essential to ensure constant and reliable sensitivity levels of SPAD arrays over long periods of time, as demanded by today's applications.

## Architecture and implementation

Fig. 2 shows the schematic of the DCP; it is clocked by a 6-bit digital controlled oscillator (DCO). The DCP resembles a 11-stage Dickson architecture, except for a parasitic capacitance, $C_{parasitic}$, in each stage that can be digitally modulated via NMOS switches. The voltage gain in each stage is $(V_{dd} - V_t)C/(C_{parasitic} + C)$, where $V_{dd}$ is the power supply, $V_t$ the threshold voltage of the stage's diode, and C the main capacitance. The input voltage of the DCP is 3.3 V, the nominal power supply voltage, and C is 1.64 pF. The DCP output voltage modulation step is approximately 80 mV and it depends on the DCP frequency and $I_{sum}$. This voltage step was chosen as 1% of the detector sensitivity. Fig. 3 shows a schematic of the environment monitor. The monitor acquires the dark counts and computes the dark count rate (DCR) of a reference SPAD that was shielded from light; it also measures the width of the avalanche pulses of the SPAD. The width of the avalanche pulse is proportional to the excess bias and the SPAD capacitance. The avalanche pulse is converted onto a square wave, EN, by a comparator and digitized to a digital code with the pulse-width-to-digital converter (PWDC). The PWDC consists of a 4-stage differential inverter chain with a 10-bit counter; the inverter chain oscillates when EN in on. The frequency of oscillation is the inverse of the timing resolution, which in turn is dynamically checked by the replica PWDC that is fed a reference pulse generated by a temperature independent PLL on a FPGA. The DCR and avalanche pulse width will be used to estimate the temperature and the excess bias of the SPAD. There are three identical environment monitors operating in parallel to increase the estimation speed and to cope with low DCR.

## DCP and Environmental monitor Characterization

The DCP and the environment monitor have been designed and fabricated using a 2P4M high voltage 0.35 µm CMOS process. A photomicrograph of the chip is shown in Fig. 4. The DCP was characterized first in open-loop and subsequently in closed-loop, with a controlled load current and temperature. Fig. 5 (a) shows the DCP output voltage plotted as a function of DCO clock frequency and control coding in an open-loop operation mode. Fig. 5 (b) shows the DCP output voltage as a function of clock frequency for selected codes. Fig. 5 (c) shows that the optimal frequency shifts up by increasing loading for a given control code, while Fig. 5 (d) shows how the DCP output voltage varies with different control codes by changing the loading. when the DCP is operated at the optimal clock frequency for that loading level. The resolution of PWDC is 204 ps at 20 °C , and has a INL of +0.5 / -1.6 LSB in a 1.24 µs input range; note that the typical single-shot jitter is 1.6 LSB (FWHM). The resolution improves by 4.1 ps and 4.3 ps by cooling the device to 10 °C and by increasing the power supply voltage by 0.1 V, respectively. Fig. 6 (a) and (b) plot the pulse width histogram of SPAD avalanche pulses occurred and measured by the PWDC at several excess bias values from 1.5 V to 3.5 V with a 0.5 V step, spanning a temperature range from 0 °C to 70 °C with a 10 °C step. The average FWHM of the pulse width is 13.8 ns, corresponding to 115 mV of excess bias and 21.6 °C temperature resolution. By averaging the results over 200 iterations, the FWHM can be improved to 3.47 ns, corresponding to 28.9 mV of excess bias and 5.4 °C temperature resolution. The estimation time is limited by DCR, the DCR being less than 10 Hz at lower temperatures. Fig. 6 (b) summarizes the relation between DCR and pulse width at various temperature and excess bias combinations. Fig. 6 (c) summarizes the relations between pulse width, DCR, temperature, and excess bias.

## Interpolation method for excess bias and temperature information

Fig. 7 shows the excess bias and temperature information estimation based on a look-up table (LUT) that was acquired

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beforehand. To acquire excess bias and temperature information based on an interpolation method, the parameter, $\alpha$ and $\beta$ should be solved using measured vector $\vec{x}$, and temperature direction, $\vec{a}$, and excess bias direction vector, $\vec{b}$, from the equations shown below,

$$\vec{x} = \alpha\vec{a} + \beta\vec{b}.$$

By assuming that $\vec{a} = (\Delta PW_a, \Delta DCR_a)$, $\vec{b} = (\Delta PW_b, \Delta DCR_b)$ and $\vec{x} = (\Delta PW_x, \Delta DCR_x)$ van be measured, then, $\alpha$ and $\beta$ are calculated as below,

$$\alpha = \frac{DCR_b PW_x - PW_b DCR_x}{PW_a DCR_b - PW_b DCR_a} \quad (1)$$

$$\beta = \frac{DCR_a PW_x - PW_a DCR_x}{PW_b DCR_a - PW_a DCR_b} \quad (2)$$

Then current excess bias, $V_{ex}$, and temperature, $T_x$, are calculated using excess bias step $\Delta V_e$, and temperature step $\Delta T$, based on the course calibration beforehand (Fig. 6 (c) and Fig. 7), as below

$$V_{ex} = V_e + \alpha \times \Delta V_e \quad (3)$$

$$T_x = T + \beta \times \Delta T \quad (4)$$

## System characterization

The DCP was tested in closed-loop configuration, whereas the environment monitor is used in the feedback. Fig. 8 (a) shows the block diagram for the feedback loop. The SPAD array is emulated by a variable current source. The DCP output is provided to three SPAD cathodes. All SPAD outputs are read out and monitored by FPGA, simultaneously, the SPAD outputs are rectified and converted to digital codes by a bank of PWDCs. The DCR calculator counts the count rate and the Pulse width calculator takes averages of the pulse width. The PWDC is dynamically calibrated using a replica pulse from a temperature-insensitive PLL in the FPGA. FPGA and host PC estimate the excess bias of the SPADs using a LUT which has been pre-calculated during a calibration phase. Based on the estimation, the proper digital code for DCP and DCO is generated and available from the FPGA. Fig. 8 (b) shows the timing diagram of the system. The system clock frequency is 20 MHz. After reset, the replica pulse is generated. Once one of the SPADs fires, the FPGA starts to read out the latched data of all PWDCs in 26 clock cycles. Then, the system again waits until the next dark count occurs in an event driven scheme.

Fig. 9 (a) and (b) show the measured excess bias with and without feedback. The excess bias is reconfigured in real time when temperature or load current are dynamically changed with the feedback loop described above. The resulting estimated excess bias derived from the LUT is also drawn in the same graph. The average excess bias difference between measurement and estimation is 78 mV and 60 mV for the temperature and the load current sweep, respectively. Voltage variations of 5.7 % and 3.7% were measured with the feedback when the temperature ranged from 28 °C to 65 °C and the load current from 0 A to 100 µA, respectively. The same voltage variation increased to 10.3 % and 68 %, respectively, without feedback. With feedback, the variation in sensitivity was only 1.9 % at a wavelength of 450 nm in the entire temperature range. Fig. 9 (c) summarizes the features of the proposed high-voltage generator and compares it with the literature [2], [3], [6].

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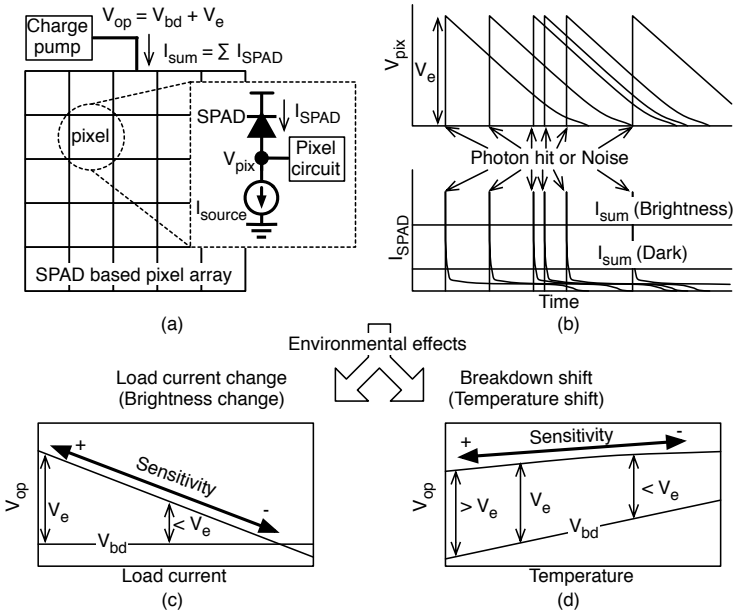



Fig. 1. (a) Concept of a SPAD array with excess bias voltage stabilization via charge pump. (b) Superimposed oscilloscope traces of pixel responses. (c),(d) Typical response of a conventional charge pump supplied $V_{op}$ as a function of load current and temperature with respect to breakdown voltage $V_{bd}$. Sensitivity varies with excess bias and thus it will degrade with an increase temperature and load current.

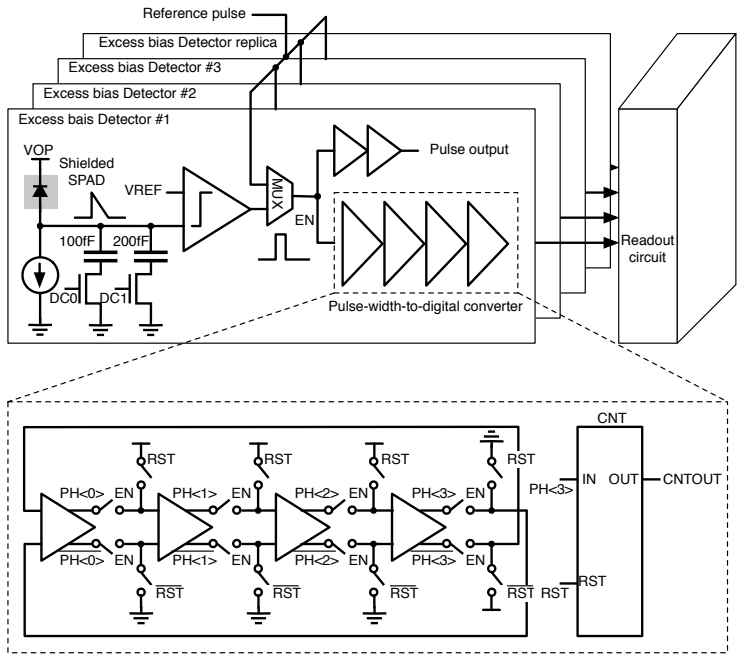



Fig. 3. Schematic of the environment monitor, comprising an array of shielded SPADs, a comparator, the pulse-width-to-digital converter, and readout circuitry.

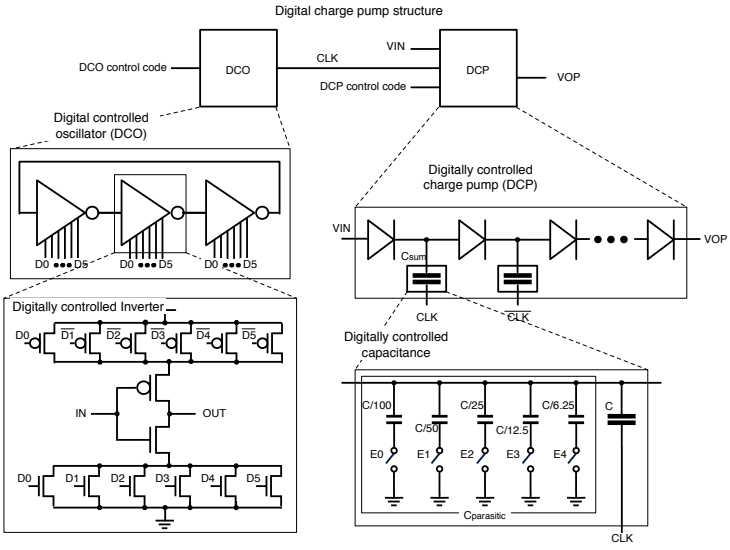



Fig. 2. Block diagram of the digitally controlled charge pump and schematics of its components. The DCO is a three-stage digitally controlled ring oscillator; the frequency of oscillation can be swept from 43.7 MHz to 1.2 GHz. The DCP is also digitally controlled; the output voltage is determined by the value of $C_{sum}$ in each stage.

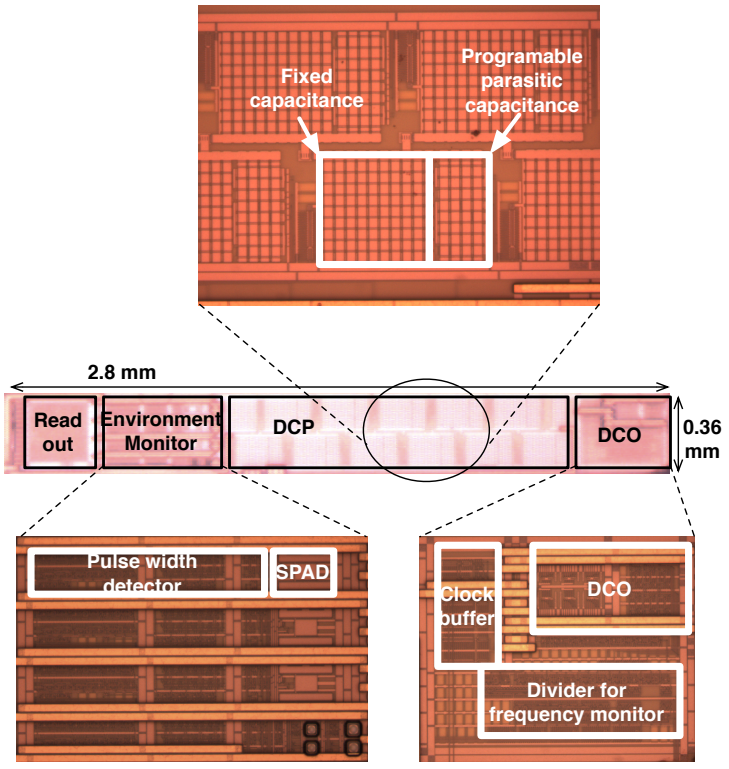



Fig. 4. Chip microphotograph. Details of the circuit are shown in the insets. It was fabricated in a standard 0.35 µm CMOS process. The die size is 0.36 × 2.7 $mm^2$. The 6 µm diameter SPAD comprises a p+ / deep n-well junction with a p-well guard ring [5]. The breakdown voltage at 20 °C is 19.6 V. The quenching current source generates 15 µA.

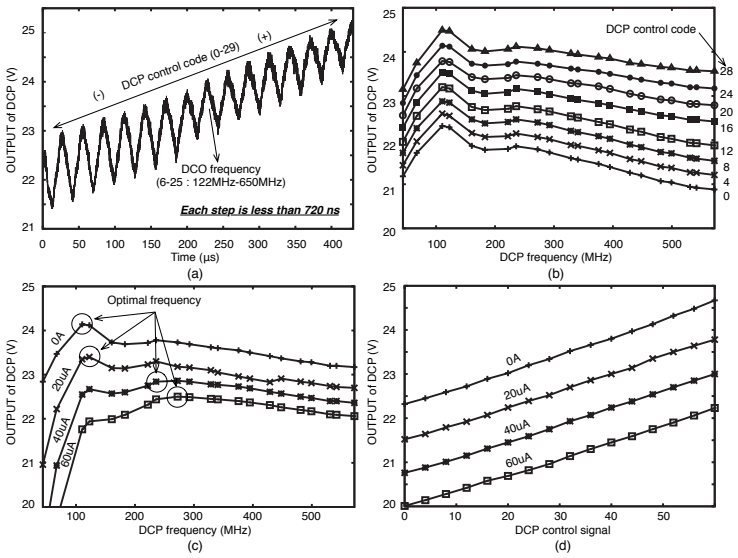



Fig. 5. Measurement results of the DCP. (a) Transient sweeping of the DCO clock frequency and DCP control code. (b) DCP output voltage as a function of DCO frequency and DCP control code. (c), (d) DCP output voltage as a function of DCO frequency for a given DCP code at various loading levels.

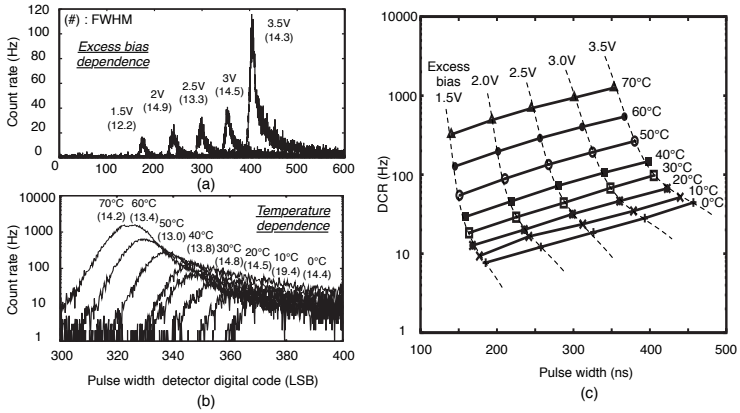



Fig. 6. Estimation of avalanche pulse width and excess bias in various environmental conditions. (a), (b) Pulse width histograms as a function of excess biases and temperature; in parentheses the FWHM jitter of the measurement is reported. (c) Pulse width estimation vs. DCR for various combinations of excess bias and temperature.

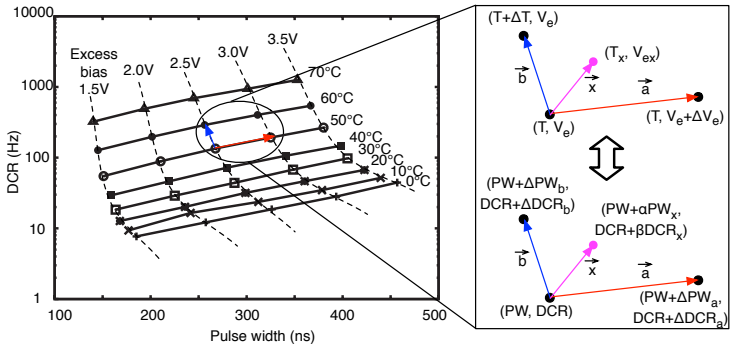



Fig. 7. Interpolation method to acquire excess bias and temperature information using coarse calibration data.

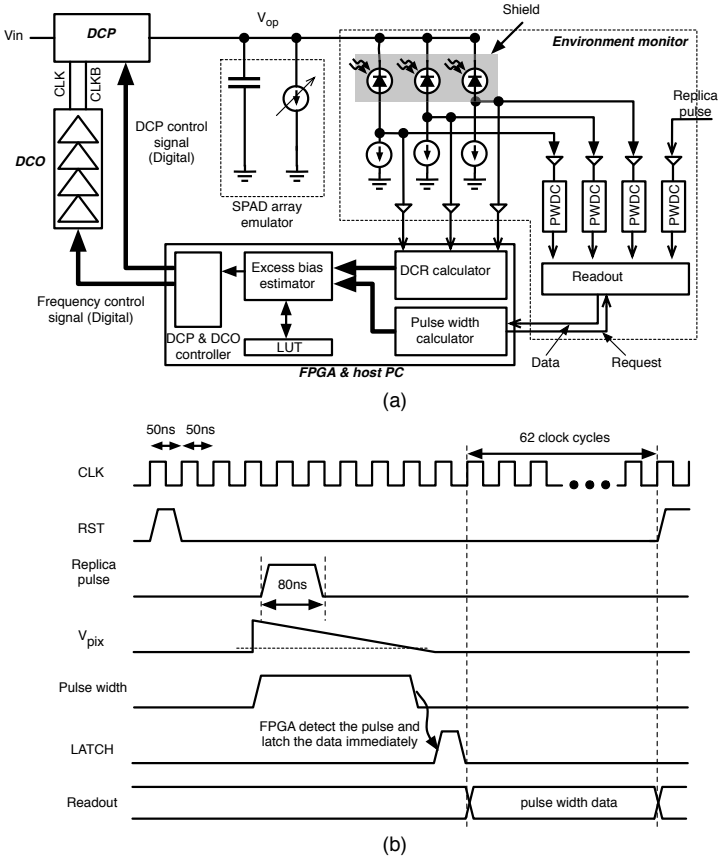
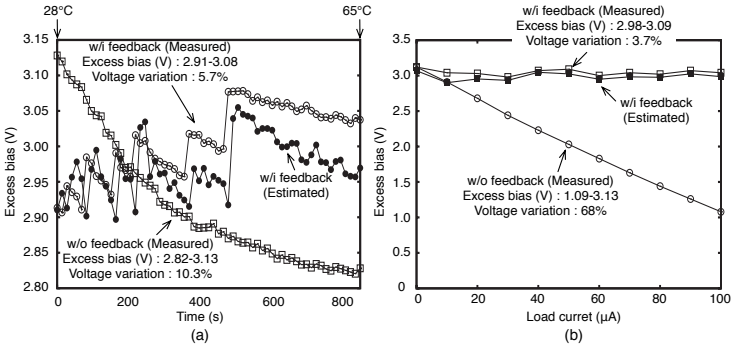



Fig. 8. (a) Block diagram for the feedback loop. (b) Timing diagram. The readout circuit starts to read out as soon as the FPGA detects the DCR pulse. The minimum number of clock cycles to read out the data from three PWDCs and the replica PWDC is 62.




| Features | This work | [2] | [3] | [6] |
|---|---|---|---|---|
| Technology | 350 nm | 130nm | 90nm | 180nm |
| Area | 0.36 mm x 2.8 mm | 0.3 mm x 0.1 mm | 0.12 mm x 0.16 mm | 2.05 mm x 1.95 mm |
| Output voltage | 21.4 V - 25 V | 1.2 V to 8V | 10.9 V | 1.2 V - 6 V |
| Application | SPAD based camera | Non-volatile memory | SPAD based camera | Earphone |
| Current change | **Insensitive** | Sensitive | Sensitive | **Insensitive** |
| Temperature shift | **Insensitive** | Sensitive | Sensitive | Sensitive |

(c)

Fig. 9. Excess bias voltage control results with and without feedback as a function of (a) temperature and (b) load current. (c) Specification summary and comparison with literature.