A Geiger Mode APD Fabricated in Standard 65nm CMOS Technology

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Abstract

We present the first avalanche photodiode (APD) successfully fabricated in standard 65nm CMOS technology. The APD operates both in proportional and Geiger mode at -60C to +60C temperature range. The device comprises an octagonal n+p-well junction surrounded by an n-tub guard-ring; its photon detection probability peaks at 450nm with 200mV excess bias and it is above 1% between 350 and 750nm. The dark count rate is 1.5kHz/μm^2 at 200mV excess bias, while afterpulsing is less than 1% for a dead time longer than 5μs and timing jitter is better than 235ps. Applications include low-power, ultra-high-speed quantum number generators, time-of-flight 3D image sensors, LIDAR detectors, and time-resolved spectroscopy.

Introduction

Photon counting is useful in many applications where single-photon sensitivity and time-of-arrival detection is critical. Photon counting can be achieved in CMOS since 2003, thanks to the creation of Geiger mode APDs or single-photon avalanche diodes (SPADs) in 0.8μm [1], however more advanced CMOS technologies have later emerged due to the flexibility of ultra miniature pixels enabling advanced functionality. Thus, a continuous trend towards low pitch pixels has continued over the years, fueled by the need for multi-megapixel photon counting cameras for scientific and biomedical applications and gigabit-per-second quantum random number generators for embedded security and gaming applications [2],[3].

State-of-the-art SPAD technology has reached the 90nm CMOS technology node [4],[5]. In this paper, we propose a new APD fully characterized and modeled in a standard 65nm CMOS process that operates in Geiger and proportional mode. The design is not a simple shrink of an older node but it has required extensive redesign. For this reason, significant modeling efforts were devised before and after fabrication.

Structure and Modeling

The APD, shown in Fig. 1, has an octagonal n+p-well junction under which the multiplication region is confined.

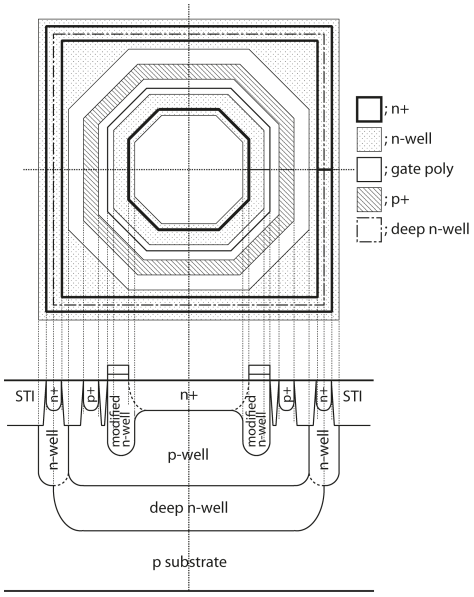

Fig. 1. Top-view and cross-section of the proposed SPAD.

An n-tub guard-ring is used to prevent edge breakdown due to high electric fields at the edges of typical planar junctions.

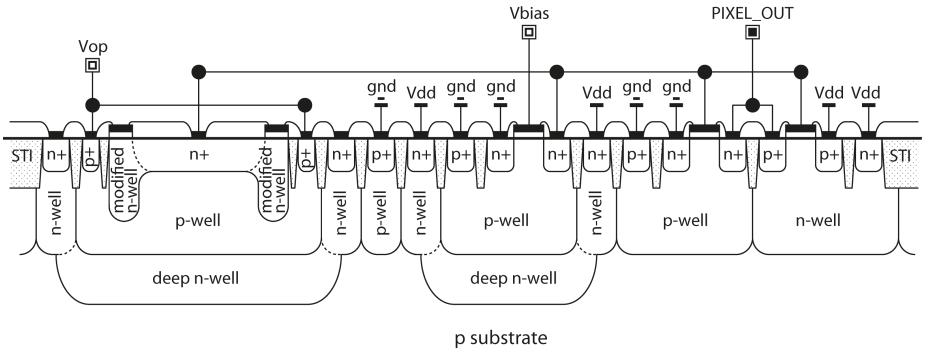

Fig. 2. Integration of the SPAD with CMOS compatible digital electronics; the electronics can also implemented inside the guard rings as proposed in [6].

Fig. 2 shows the cross-section of a pixel that includes the APD and functional circuitry lying side-by-side in a possible monolithic implementation of an array. The circuitry can also be placed on the guard-ring itself, as demonstrated for other CMOS processes in [6]. The potential across the junction was simulated in depth for several values of operating voltage V_{OP} ($V_{OP}=V_e+|V_{bd}|$, where V_e is the excess bias and V_{bd} the breakdown voltage). The results of Fig. 3, show the collapse of the potential when a breakdown voltage of 9.1V is reached; this result was confirmed by measurements.

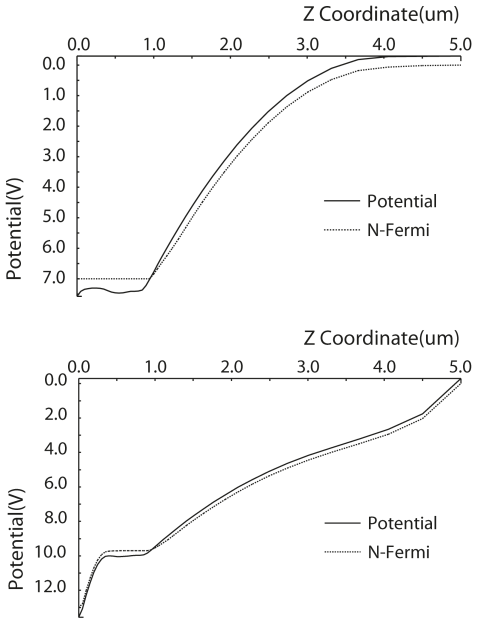

Fig. 3. Simulation of the collapse of the potentials upon reaching the breakdown voltage in accordance with measurements. Potential profile below breakdown, V_{OP}=8V (top); above breakdown, V_{OP}=13V (bottom).

Optical/Electrical Characterization

The current-voltage (I-V) characteristics of the APD is plotted in Fig. 4. The breakdown voltage is found to be typically 9.1V at room temperature.

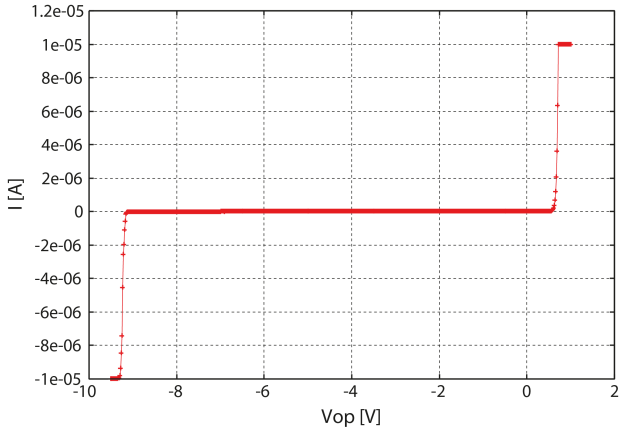

Fig. 4. Measured I-V characteristics of the APD at room temperature. The typical breakdown voltage in this technology is 9.1V (Compliance: 10μA).

Fig. 5 plots breakdown voltage at various temperatures for two bias currents. Note the variation in temperature behavior, suggesting the dominance of band-to-band tunneling. To validate the uniformity of the avalanche in the multiplication of the APD, the electric field was simulated in 3D.

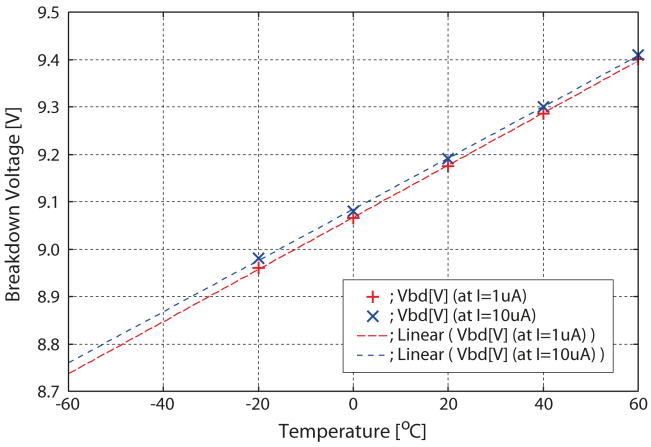

Fig. 5. Measurement of the breakdown voltage as a function of temperature.

As per design, the electric field exceeds critical values for impact ionization in silicon at the center of the sensitive area, as shown in Fig. 6, while premature edge breakdown is expected to emerge at higher excess bias voltges.

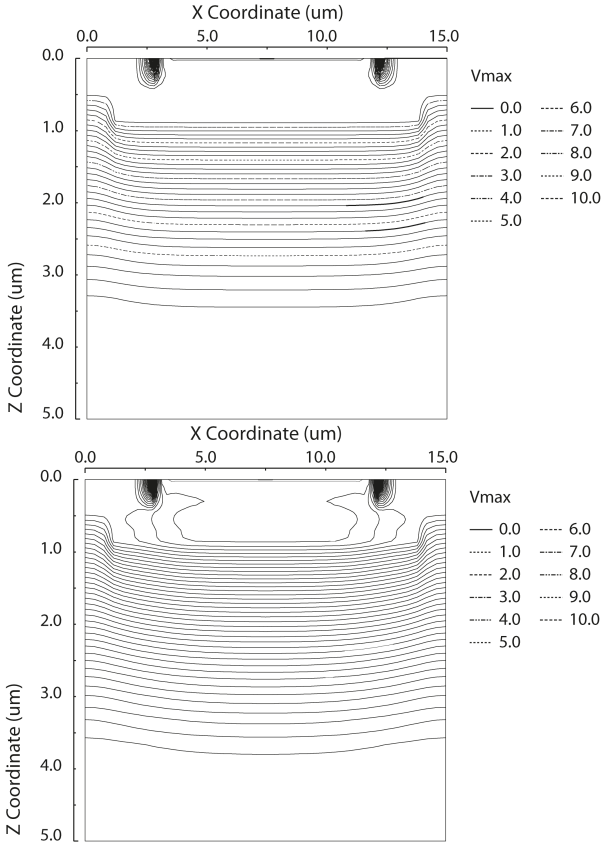

Fig. 6. Simulation of the electric field: below critical (<2.5×10^5V/cm in silicon at 300K) for a bias below breakdown (top), above critical (bottom).

A photomicrograph of the APD is shown in Fig. 7. The light emission test confirming premature edge breaddown at high excess bias is also shown in the figure.

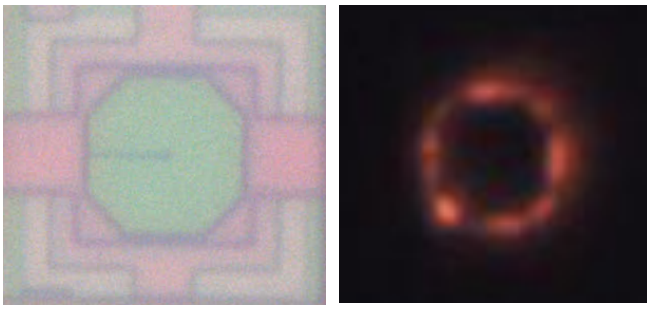

Fig. 7. Micrograph of the proposed APD (left). The active area of the device measures 8x8μm^2. Light emission test showing edge breakdown (right).

The APD was tested in Geiger mode using a ballast circuit as shown in Fig. 8. While an active recharge is possible, acting on Vbias, in our measurements an external 7kΩ resistance was used. A comparator with appropriate threshold voltage, implemented by an inverter, was used to convert Geiger pulses to digital signals and to perform impedance adaptation.

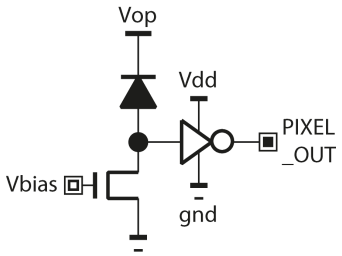

Fig. 8. The APDs were biased above breakdown (Geiger mode) using the above circuit. The ballast resistance R_Q is implemented as a transistor biased in sub-threshold or in saturation (depending on the needs) via Vbias for passive or active quenching and passive recharge. The anode lead is connected to the exterior via a buffer that acts as comparator and impedance adapter.

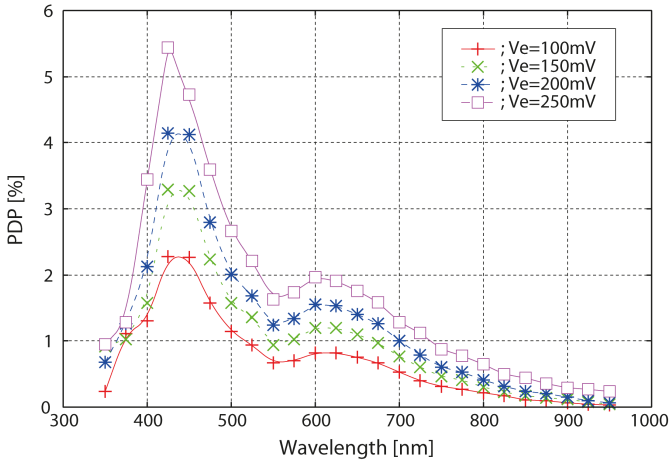

Fig. 9. Measurement of the photon detection probability (PDP) of the fabricated APD when operating in Geiger mode at various excess bias voltages at room temperature.

The photon detection probability (PDP) was measured at several excess bias voltages in the 350-950nm spectrum (Fig. 9). As expected, the PDP is virtually insensitive to temperature. The dark count rate (DCR) was measured at various temperatures (-60C to +60C) and excess bias voltages V_e, as shown in Fig. 10.

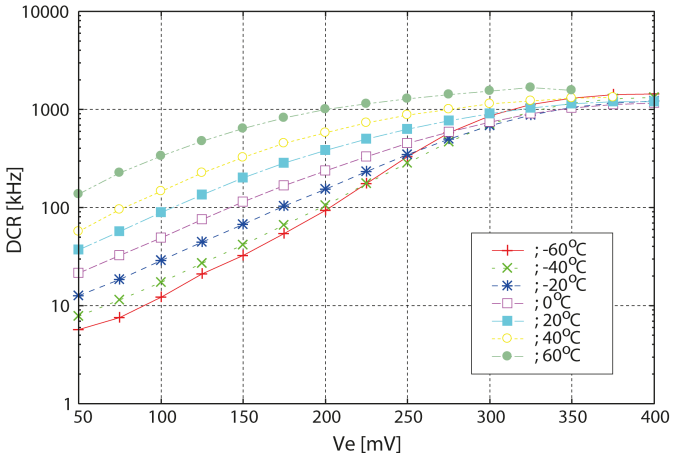

Fig. 10. Measured dark count rate (DCR) as a function of excess bias and temperature (-60C to +60C).

Fig. 11 shows the standard DCR plot in log scale as a function of the inverse of temperature for a range of excess bias voltages (50mV – 200mV).

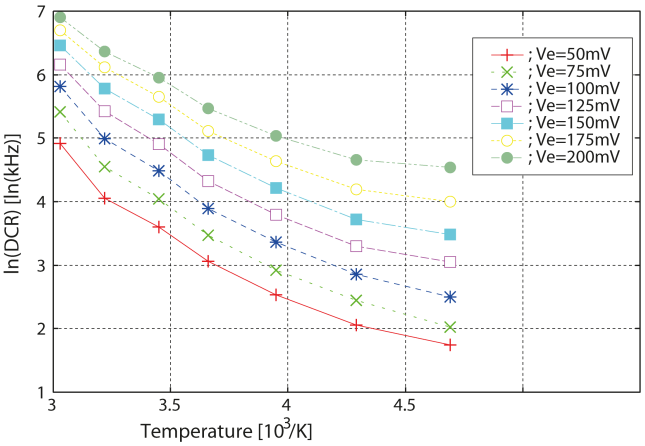

Fig. 11. Measured DCR (in log scale) as a function of the inverse of temperature for various excess bias voltages V_e.

Fig. 12 shows a histogram of the inter-arrival time rates measured in the device at room temperature. The afterpulsing probability is computed from this histogram as a function of the of dead time using standard techniques [7]. An afterpulsing probability of less than 1% was measured at a dead time higher than 5μs.

The jitter was characterized for a range of excess bias voltages. In Fig. 13 we report one such a response (in log scale). The full-width-at-half-maximum (FWHM) jitter measured with an excess bias voltage of 400mV was 235ps.

The measurement was obtained by time-correlated single-photon counting (TCSPC) using a time-to-digital converter built in a standard oscilloscope (LeCroy WaveMaster 6200). The laser source was a pulsed 637nm laser (Advanced Laser Diode Systems, GmBH, Germany) operating at 40MHz with a laser pulse width of less than 80ps.

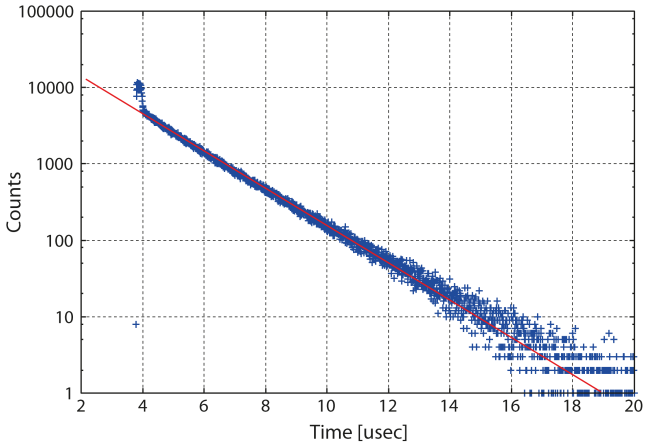

Fig. 12. Histogram of the inter-arrival time rates at room temperature as a function of time.

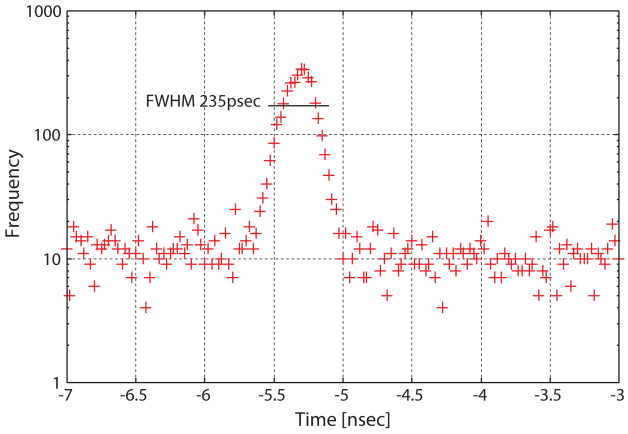

Fig. 13. Measured temporal response of the APD operating in Geiger mode at room temperature. The full-width-at-half-maximum (FWHM) jitter is better than 235ps for an excess bias of 400mV.

Tab. 1 summarizes the performance of the APD. The characterization was performed at room temperature, except when stated differently.

Conclusions

We presented the first Geiger mode APD fabricated in standard 65nm CMOS technology. The APD can be operated both in proportional and in Geiger mode with relatively high dark counts due to band-to-band tunneling and FWHM jitter under 300ps. The APD was extensively simulated before fabrication to optimize the design and after fabrication to construct a comprehensive model of the device. Edge breakdown emerges at higher excess bias voltages, in good agreement with our model. Also in agreement with our model, the device has well-behaved temperature dependence. The APD underwent extensive characterization for a wide variety of parameters and environmental conditions, reported in the paper.

Tab. 1. Performance summary for the proposed APD.

Performance (Prop. mode)	**Min.**	**Typ.**	**Max.**	**Unit**
Dark current @ 0.1V reverse bias	2		20	pA
Active area		64		μm^2
Breakdown voltage	9.0	9.1	9.2	V

Performance (Geiger mode)	**Min.**	**Typ.**	**Max.**	**Unit**
DCR @ V_e = 0.05V	5		105	kHz
PDP @ λ=350-750nm	1		5.5	%
Afterpulsing @ 5μs dead time			1	%
FWHM Time jitter @ V_e = 0.4V			235	ps
Excess bias voltage	0		0.4	V

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