Single-Photon Image Sensors

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ABSTRACT[1]

The main goal of this paper is to expose the EDA community to the emerging class of circuits operating with single quanta of energy (e.g. photons or electrical carriers). We describe recent developments in the field of single-photon detection and single-photon imaging based on the avalanche effect. Single-photon detection is useful in a number of applications, from time-of-flight based 3D vision systems to fluorescence lifetime imaging microscopy, from low-light cameras to quantum random number generators, from positron emission tomography to time-resolved Raman spectroscopy. These applications have speed and accuracy requirements that conventional systems cannot provide if not at a very high cost. EDA has not yet adapted to the revolution introduced by avalanching devices and, though tools capable of simulating these devices exist, there is little or no capability to do so in a coherent flow, let alone at system level. We challenge CAD designers to fill this gap and prepare them to the circuits of the future, quantum in nature but built in standard CMOS technology.

Keywords

Single-photon detection, photon counting, single-photon avalanche diode, SPAD, silicon photomultiplier, SiPM, time-resolved imaging, EDA

1. INTRODUCTION

Photon counting is a useful tool in many scientific and biomedical imaging sensors; it usually requires single-photon detection capability, as well as functionality such as counting and time-of-arrival evaluations. When photon counting is available in large arrays of independently operating pixels, it may enable emerging imaging modalities. Examples include fluorescence lifetime imaging microscopy (FLIM), fluorescence correlation spectroscopy (FCS), time-resolved Raman spectroscopy, time-of-flight cameras, etc. Photon-counting imagers can be useful in nuclear medicine, in particular in positron emission tomography (PET), single-photon emission computed tomography (SPECT), and in Gamma Cameras for 3D visualization of radionucleotides in living tissue. Photon-counting detection can also be used in embedded security techniques, where the quantum nature of light is used in the generation of true random numbers for encryption and other information hiding purposes.

Devices for photon counting have been in existence for some time; they have been introduced in non solid-state form, i.e. photomultiplier tubes (PMTs) and microchannel or multichannel plates (MCPs) already in the 1930s. These devices share a few properties: a large active area (cm^2), a high fill factor, and a single channel that generally requires amplification; they are also bulky and require vacuum for normal operation. Recently, compact photon counting devices have emerged, known as silicon photomultipliers (SiPMs), that operate in normal atmosphere and at room temperature. SiPMs have a single output, however their multi-channel counterparts are based on arrays of single-photon avalanche diodes (SPADs) that provide single-photon detection in tens or hundreds of thousands of locations independently. In addition to a (x,y)-position information of a photon hit, SPADs can also provide the time-of-arrival of a photon at picosecond resolutions millions of times-per-second. SPADs and SPAD arrays may be fabricated in dedicated silicon processes or in standard CMOS, thus enabling the implementation of megapixel cameras operating in single-photon regime.

Cova and McIntyre were among the first to advocate SPADs as an effective technology for fast timing applications in the 1980s [1,2]. High-resolution, time-resolved photon detection, as time-correlated single-photon counting (TCSPC) are natural applications for SPADs. Since the demonstration of CMOS SPADs at the beginning of the millennium, it has become possible to create true imagers [3].

This paper reports on innovations that have followed since 2005 in the domain of CMOS SPAD imagers with the intention of exposing the EDA community to the challenges of the design of this class of circuits, while emphasizing the limits of the current CAD tools to design such circuits.

2. SINGLE-PHOTON AVALANCHE DIODE (SPAD)

A SPAD is essentially a p-n junction that relies on impact ionization to create a large number of photon-generated electrons and holes from a single electron-hole pair. Fig. 1 shows the *steady-state* I-V characteristics of a typical p-n diode.

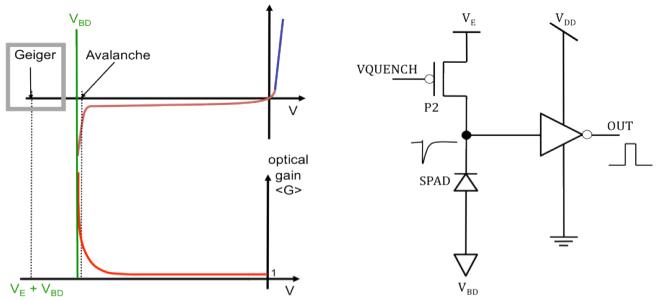

Fig. 1. Steady-state I-V characteristics for a p-n junction with Geiger and avalanche mode of operation (left). Passively quenched SPAD (right). V_E is known as the excess bias voltage at which a diode must be biased in Geiger mode. A comparator or inverter is used to shape the output pulse of the detector.

DAC '13, May 29-June 7, 2013, Austin, TX, USA

What this curve does not show is the pseudo-steady-state behavior in the breakdown operating condition. A voltage above the breakdown voltage can be applied so long as no carriers exist in the diode's depletion region. As soon as a carrier is injected into the depletion region, impact ionization may cause an avalanche, and the diode will shift operating points to the steady state [4].

In general, electrical simulators, such as SPICE, SPECTRE™, NanoSim™, and others do not take into account the pseudo-steady-state behavior of the junction at and above breakdown, thus making it impossible to simulate the actual behavior of a SPAD in the transient. Although macroscopic models have been built in Verilog-A and other languages, an accurate modeling of SPADs is still elusive.

When biased above breakdown, the SPAD is said to operate in Geiger mode; in this mode of operation, it is capable of detecting single photons, since the avalanche current generated upon photon detection can be easily converted to a digital signal, as shown in Fig. 1. The figure also shows the circuitry used for quenching the avalanche and to recharge the diode to its initial idle state. There exists a variety of avalanche quenching techniques, partitioned in active and passive methods. The literature on these variants is extensive [5]. In active methods, the avalanche is detected and stopped by acting on the bias. In passive methods, the p-n junction bias is self-adjusted using, for example, a ballast resistor. These mechanisms are clearly analog in nature and require accurate modeling capabilities to estimate speed and current requirements at a microscopic level. This characterization is especially important when hundreds or thousands of SPADs operate simultaneously on chip.

When regenerated in a comparator or an inverter, the signal becomes digital and thus acceleration techniques can be used to simulate the signal afterwards. However, conventional mixed-signal simulators are inefficient, as the actual analog segment of the circuit is actually very small. Thus, a new generation of modeling and simulation tools is sought.

One of the main requirements for a SPAD is that its junction does not cause premature edge breakdown (PEB). This phenomenon has the effect of limiting the zone where an avalanche can occur to the edge of the sensitive area, thereby strongly reducing the sensitivity of the SPAD by effectively slashing the fill factor. Several measures can be taken to prevent PEB; these measures generally involve the use of guard rings to reduce the electric field at the edge of the device or to increase the breakdown voltage locally. Fig. 2(a)-(d) show some of the structures used to achieve the goal. Shallow trench isolation (STI) was also demonstrated [6]. STI is used to delimit the junction, provided that it is surrounded by a multi-layer of doped silicon so as to force recombination of those charges generated in the defect-rich STI as shown in structure (d) [7]. The other structures may or may not be compatible with a CMOS process; this is an important requirement to construct images sensors, as understood early on by Rochas [8] and proposed by us and by others [3,7,9,10].

With proper knowledge of the doping profiles of the various CMOS layers and a device simulator, it is possible to predict whether a given structure is likely to achieve the goal. This is done implicitly by looking at a simulated electric field profile to see where it exceeds the critical value for a sustained avalanche ($\approx 3\times10^5$V/cm in silicon).

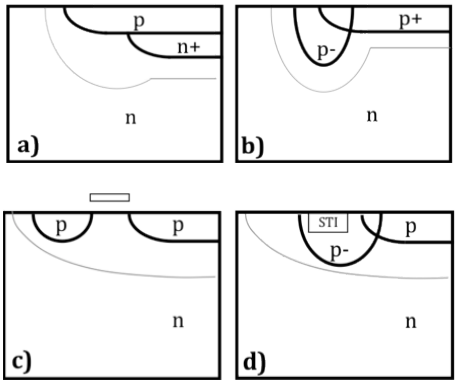

Fig. 2. Example of possible junctions with various types of guard rings: a) enhancement mode; b) explicit; c) implicit; d) STI based.

Fig. 3 shows a study of a guard ring performed before fabrication that shows the effectiveness of the guard ring (shown on the half-cross-section of the device).

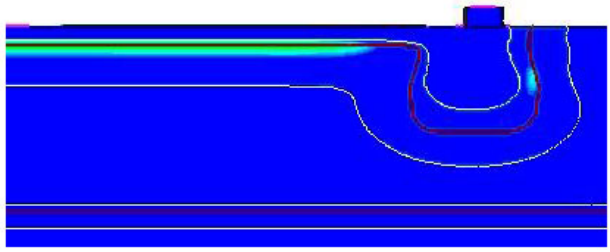

Fig. 3. Device simulation of the electric field distribution in a guard ring of a SPAD [7].

Though effective, this approach does not yield a guarantee that the SPAD will be free of PEB. Thus device simulation should be coupled with the conditions for a sustained avalanche in form of the well-known equation

$$1 < \int_{z_0}^{z_1} \alpha \, dz,$$

where α is the mean ionization per free carrier, and z_0 and z_1 are the limits of the depletion region.

Several more parameters in a SPAD are hard to predict. For example, the probability that a single photon's generated carriers are detected, called the photon detection probability (PDP), requires a deep knowledge of the optical stack and of the junction's quantum efficiency. Noise's sources include tunneling and fabrication defects, which ease valence-to-conduction band transitions, such as thermally generated or tunneling carriers. Dark counts are characterized by the dark count rate (DCR) and are difficult to predict with high degrees of certainty due to the non-deterministic nature of the noise sources and their localization.

The dead time is referred to as the time required in a detection cycle, generally in the ns~µs range. The dead time determines the maximum count rate a SPAD can support. In active quenching, such maximum count rate is the inverse of the dead time; when passive quenching is used the maximum count rate is divided by *e*. (*e* = 2.718281…) The ratio between maximum count rate and DCR gives an indication of the dynamic range that in SPAD imagers is usually over 80dB. Also in this case, accurate modeling of the quenching and recharge mechanisms are critical and often

overlooked by designers or simply unavailable due to limitations of the simulation tools.

3. SPAD IMAGE SENSORS

Creating large arrays of essentially independent digital pulse generators (the SPADs) implies the design of efficient data readout mechanisms that are not different from conventional imagers in terms of functionality and complexity, though of purely digital nature. Thus, they are more similar to clock trees than readout circuits. The simplest readout architecture implementing photon-counting on-chip in combination with random-access single-photon detection, was demonstrated for the first time in [3]. In this readout scheme, all time-sensitive operations had to be performed sequentially. The micrograph of the chip is shown in Fig. 4(a).

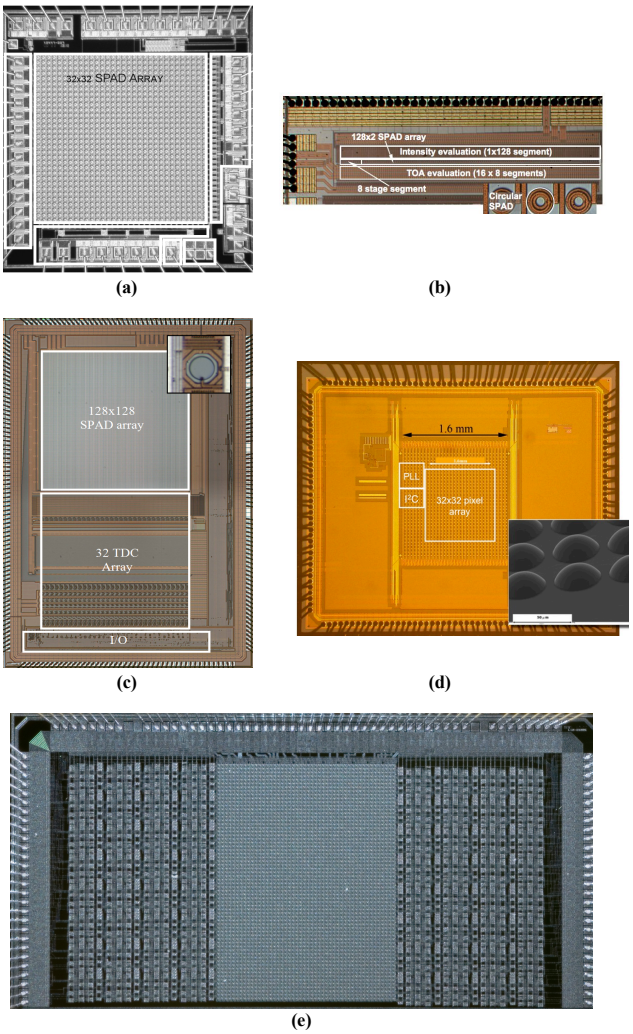

Fig. 4. SPAD arrays and readout architectures. (a) Random access 32x32 SPAD array [3]; (b) latchless access 128x2 SPAD array [11]; (c) event-driven access with column-parallel TDCs [12]; (d) pixel-parallel TDCs with microlenses in the inset [14]; (e) event-driven access array with auto-generated digital circuits, whereby the SPADs were instantiated in Verilog™ [19].

The readout bottleneck was partially addressed by means of a latchless pipeline, a technique proposed in [11] and shown in Fig. 4(b), where a time-to-digital converter (TDC) was used at the column level to determine where in the column and when the photon was received. The challenge of this design was the characterization of an unusual technique to transmit digital data through a channel with constant and uniform delay. The first fully integrated SPAD array was reported in LASP [12,13], shown in Fig. 4(c), where column-parallel TDCs were used to process photon arrivals in an event-driven fashion. Again, the clock tree-like readout required particular care during the design phase due to timing requirements. Finally, in the project MEGAFRAME [14,15,16], a pixel-parallel array of 32x32 TDC-SPAD pixels was implemented. The chip reported in [14] is shown in Fig. 4(d). A larger version of the chip (160x128 TDC-SPAD pixels) was later reported in [17], while other column-parallel arrays have recently been reported in [18].

In MEGAFRAME, each TDC had resolutions varying from 52ps to 119ps, with a depth of 10b and a cycle time of 1µs. In these chips the differential non-linearity (DNL) and integral non-linearity (INL) could typically range from 1 to 4LSBs and in LASP, they were recently improved to ±0.1LSB and ±0.25LSB, respectively [13]. The design of the readout and of the pixel required care as they were performed separately and independently. Timing closure techniques were essential, while advanced analog simulation tools had to be used at the pixel level.

The design reported in [19] is the first attempt to treat the SPAD as a device that can be instantiated like any other digital component within a library and placed/routed as such. The fabricated design is shown in Fig. 4(e); it required only 2 weeks for design and it was successfully fabricated and tested.

4. LESSONS LEARNED AND FUTURE CHALLENGES

Since the first CMOS SPAD, the growth of SPAD image sensors in resolution, format, and functionality has been tremendous, often matching Moore's Law. Optical detection and processing can now be performed in massively parallel systems, thanks to very large scale integration and miniaturization. However, limitations still exist, especially in EDA tools, from device modeling (micro and macroscopically) to pixel modeling, from system-level simulation to formal verification, while optical stacks and optical concentrators are generally ignored [20]. Digital SiPM have emerged with arrays of mini SiPMs instead of single SPADs. An example of this trend has been reported by [21], where four 10x10 mini SiPMs has been implemented in 0.18µm HV CMOS technology in combination with a mirror to scan large areas in TCSPC mode.

Modeling and simulation, as well as design support, has become even more challenging with the migration of SPAD structures to nanoscale CMOS [22,23,24], exhibiting improved DCR and spectral efficiency, as well as compatibility with through silicon vias (TSVs) and backside processing. These advanced processes also bring improvements in time resolution, fill factor, pixel pitch as well as the capacity to integrate on-chip time-of-flight computation to ease I/O data rate demands.

In-pixel analog approaches to time-resolved image sensing offer smaller pitch, provided uniformity issues are addressed [25]; on the other hand, the emergence of III-V materials in fully CMOS compatible solutions may bring these materials to the mainstream. Examples of this trend are two independent works reporting the first Ge-on-Si SPADs fabricated in a way that is fully compatible with a conventional CMOS technology [26,27]. Clearly, new modeling and design tools will be required in this domain as well.

5. ACKNOWLEDGMENTS

We acknowledge all our doctoral students and post-doctoral fellows that over the years made the advances in single-photon detection and single-photon imaging possible. The Swiss National Science Foundation, NCCR MICS, the European Commission (FP6 and FP7 programs), Xilinx, and the European Space Agency are also acknowledged.

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