

# A 128-Channel, 8.9-ps LSB, Column-Parallel Two-Stage TDC Based on Time Difference Amplification for Time-Resolved Imaging

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**Abstract**—This paper proposes a 128-channel column-parallel two-stage time-to-digital converter (TDC) utilizing a time difference amplifier (TDA) and shows measurement results obtained from an implementation in a 0.35- $\mu\text{m}$  CMOS process. The first stage operates as a coarse TDC, the time residue is amplified by a TDA, then converted by the second-stage TDC. As the gain of the time difference amplifier can be adjusted from 8.5 to 20.4, the time resolution of the TDC can be tuned from 21.4 to 8.9 ps. The time resolution variation due to process-voltage-temperature (PVT) effects is  $\pm 5.8\%$  without calibration when the time resolution is 12.9 ps. We propose a calibration method to compensate LSB changes due to the power supply fluctuation and temperature variation.

**Index Terms**—Fluorescence lifetime imaging microscopy (FLIM), positron emission tomography (PET), time-of-flight (TOF), time-to-digital converter (TDC).

## I. INTRODUCTION

**T**IME-TO-DIGITAL converters (TDCs) are widely used in time-resolved imaging applications, where photon time-of-arrival must be computed with high precision. Examples of such applications are time-of-flight (TOF) 3-D vision, positron emission tomography (PET), fluorescence lifetime imaging microscopy (FLIM), and so on. For these applications, numerous TDCs are often required to increase the frame rate and to acquire time information from as many detectors as possible [1]–[5]. Especially for PET application, it is known that multiple time information can help improve the arrival time estimation of a scintillation from a scintillator to improve timing resolution [6], [7]. A TDC can be implemented in an application specific integrated circuit (ASIC) or in a field programmable gate array (FPGA). While FPGAs enable full flexibility and fast development, ASICs are compact, reliable, and generally operate at lower power for comparable performance [8], [9]. In addition, ASICs can be used in conjunction with a photodetector array, thus minimizing parasitics. In ASIC-TDCs, the time resolution of a basic TDC consisting of a delay chain and D flip-flops (D-FFs) is determined by the unit delay element, which is often an inverter [10]. Of course, a small inverter delay could be achieved with advanced

CMOS processes with 90 or 65 nm feature size, but the price to pay is generally lower quantum efficiencies and narrower sensitivity spectra of the photodetector [11]. Some TDCs achieve subgate delay resolution by employing an interpolated delay chain or ring oscillators [12], [13], Vernier delay lines [14]–[16], pulse-shrinking [17], interpolation [18], and time difference amplification [19], [20]. TDCs employing noise shaping [21], [22] are also reported, however they occupy large area. Another approach consists of using column-level TDCs or pixel-parallel TDCs to raise the frame rate [1], [3]–[5], [23], employing a very simple structure of a delay chain, D-FFs, and counters, but at the expense of time resolution. Subgate resolution in these approaches is generally not used in the interest of a small area.

The main motivation of this paper is to achieve both high timing resolution and small area in column-parallel TDCs for TOF, PET, or FLIM applications. We employ a two-stage architecture, wherein the first stage operates as a coarse TDC (first TDC), the time residue is amplified by a time difference amplifier (TDA), then it is converted by the second-stage TDC (second TDC). The advantage of the two-stage TDC is not only simplicity, but also noise decrease of the second stage TDC by a factor equal to the gain of the TDA, in a similar fashion as in analog-to-digital converters (ADCs).

In Section II, the principle of the proposed column-parallel TDC is presented. We describe the architecture, the circuit design, and the operation of the TDA and the proposed TDC in Section III. In Section IV, the measurement results, the performance of the TDA, and the proposed TDC are shown, including environmental effects due to the power supply and temperature fluctuations. The time resolution variation in the entire TDC array is also measured. Finally, the results are discussed in Section V.

## II. PROPOSED TDC

### A. TDC Structure

A two-stage ADC and a two-stage TDC are similar conceptually since they both have double conversion and amplification of the residue, as shown in Fig. 1, whereas a two-stage TDC calculates the time residue instead of the voltage residue. The LSB of the two-stage TDC,  $\text{LSB}_{\text{two\_stage}}$ , is calculated using the LSB of each stage,  $\text{LSB}_{\text{one\_stage}}$ , and the gain of the TDA,  $G$ , as follows:

$$\text{LSB}_{\text{two\_stage}} = \frac{\text{LSB}_{\text{one\_stage}}}{G}. \quad (1)$$

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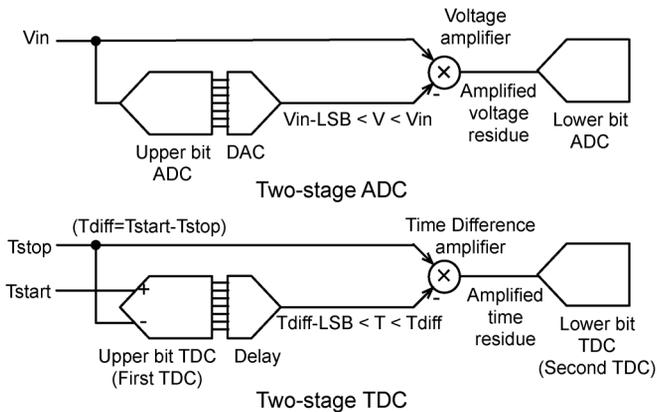


Fig. 1. Concept of a two-stage ADC and a two-stage TDC based on time difference approximation.

Time resolution is thus proportional to  $G$ , and it can be arbitrarily increased. The difficulty of the TDC, compared to the ADC, is the amplification of the time difference. Unlike an ADC, the time residue of a TDC cannot be easily stored on a capacitance. In [19], the authors implemented a large number of TDAs to calculate all possible time residues. However, the area required by such an approach can be large. The proposed TDC consists of a first-stage TDC (first TDC), a second-stage TDC (second TDC), and the TDA. We utilize only one TDA to reduce the area employing the synchronizer described in the next section. The structure of the first TDC and the second TDC are almost the same.

### B. Column-Parallel TDC

Fig. 2 shows a block diagram of the column-parallel TDC with readout module. The column-parallel TDC consists of 128 TDCs and two dummies at both ends of the array. Each TDC is connected to a single-photon avalanche diode (SPAD) [1] to not only measure differential nonlinearity (DNL) and integral nonlinearity (INL) using density tests, but also to capture line-based 3-D images using TOF and lifetime images for FLIM applications. The readout multiplexers are designed between the first TDC and the TDA, and the back of the second TDC.

## III. DETAILED STRUCTURE AND CIRCUIT DESIGN

### A. First TDC and Second TDC Structure

Fig. 3(a) shows the schematic of the first TDC in the proposed two-stage TDC. The first TDC contains a dual-rail voltage controlled oscillator (VCO), which is free-running after EN is issued, a phase detector, a VCO cycle counter, and a synchronizer, which calculates the time residue from the first conversion. The AND gate is used for gating the oscillation of the VCO just after the first conversion finishes to reduce power consumption. Delay  $\Delta t$  was added for reducing the time difference between STOP and SYNC to fit to the input range of the TDA. The second TDC is almost identical, except for the lack of a synchronizer and a 5-bit counter instead of a 6-bit counter. Fig. 3(b) and (c) shows a differential inverter in the VCO and the comparator in the phase detector. The delay of the differential inverter depends on power supply, so the frequency of the

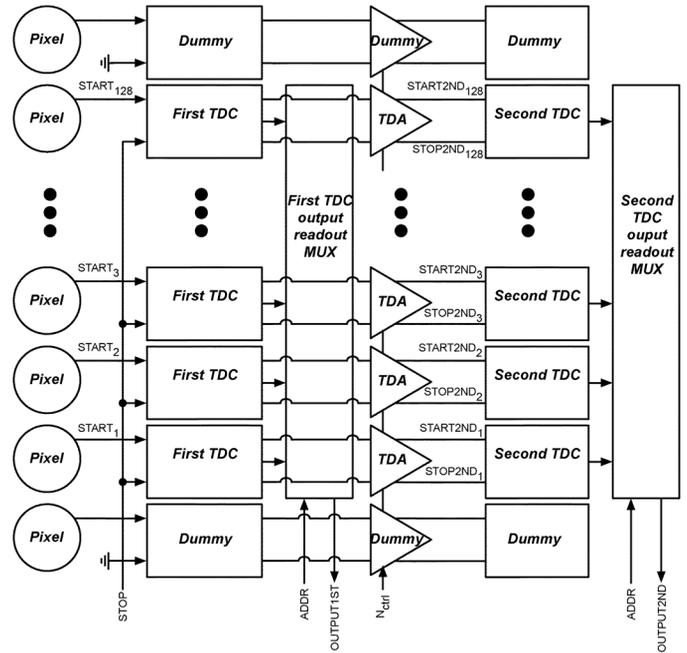


Fig. 2. Block diagram of the proposed column-parallel TDC.

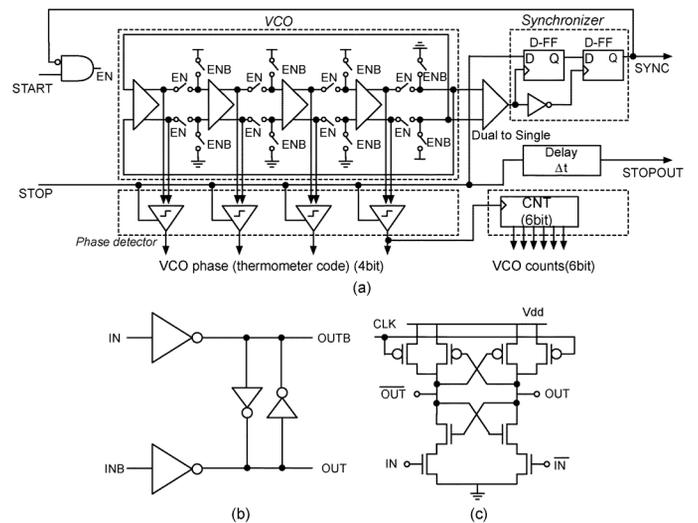


Fig. 3. Block diagram of the first TDC. (a) Schematic of the first TDC. (b) Differential inverter in the VCO. (c) Comparator in the phase detector.

VCO is constant with the constant power supply. Fig. 4 shows the timing diagram for generating the time residue from the first TDC and the relation between the time residue and time difference between START and STOP. Fig. 4(a)–(c) shows three examples of possible timing diagram. The counter counts the pulses up to the rising edge of signal STOP. The first D-FF in the synchronizer is triggered by the rising edge, while the second D-FF is triggered by the falling edge by the inverter between the first D-FF and the second D-FF. After the STOP signal is issued, STOPOUT is generated after a fixed delay,  $\Delta t$ . Then, STOPOUT and SYNC are given to the TDA as an input. Thus, the range of the time residue of the first TDC is from 0.5 to 1.5 VCO clock cycles, which is noted as  $T_{VCO}$ . Fig. 4(d) shows the relation between the time residue and the START STOP time

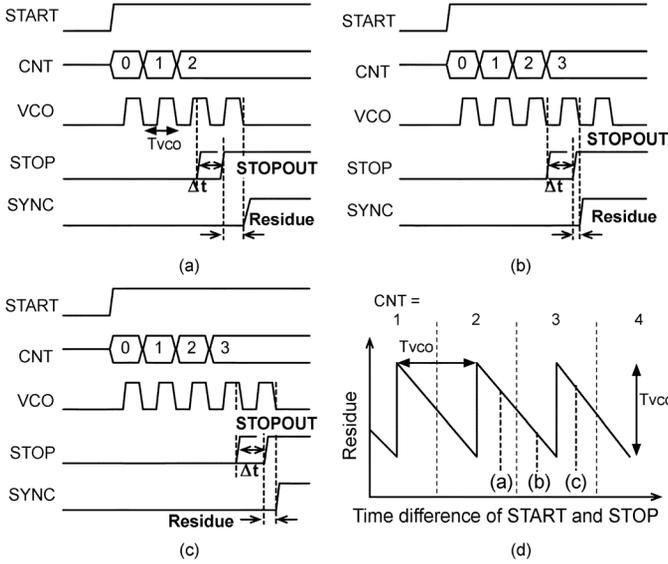


Fig. 4. Timing diagram for the time residue from the first TDC. (a)–(c) Examples of the timing diagram to calculate the time residue. (d) Relation between START and STOP time difference and the time residue.

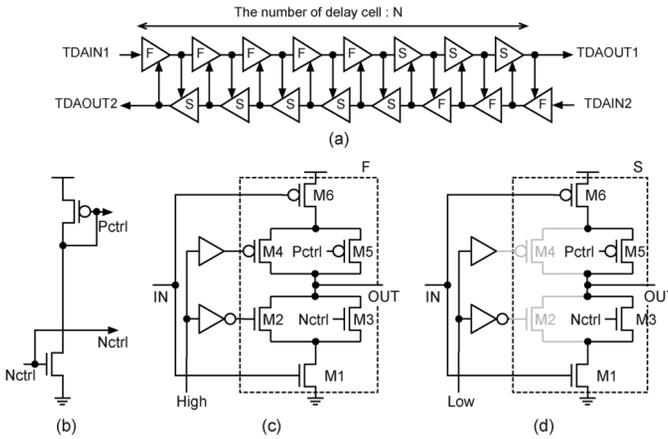


Fig. 5. TDA structure. (a) Delay chain. (b) Current mirror for the TDA control signal. (c) Fast delay cell. (d) Slow delay cell.

difference. The time residue waveform is a sawtooth wave, and the maximum of the time residue is smaller than the maximum input time difference of the TDA.

### B. TDA Structure

Fig. 5 shows the basic structure of the TDA [24]. Fig. 5(a) shows a delay chain consisting of a variable delay cell. “F” and “S” mean a fast delay cell and a slow delay cell. The two input signals propagate along the chains at two different speeds. After the two signals cross over, fast delay cells become slow, and slow delay cells become fast. The input time difference is amplified by the ratio of F and S, which is the TDA gain. Fig. 5(b)–(d) shows the schematic of the bias generator, the fast delay cell, and the slow delay cell. The fast delay cell and the slow delay cell is switched digitally by activating or deactivating transistors M4 and M2. The gain of a TDA is controlled by bias voltage,  $N_{ctrl}$ , that also controls  $P_{ctrl}$  to change the current flowing through delay cells. When the  $N_{ctrl}$  is larger than the threshold voltage,

the gain is decided by the ratio of the on-current of a fast and a slow delay cell as follows:

$$G = 1 + \frac{\beta_f (V_{dd} - V_t)^2}{\beta_s (V_{N_{ctrl}} - V_t)^2} \quad (2)$$

where  $\beta_f$  and  $\beta_s$  are the geometry and technology-dependent parameters for transistors M2 and M3 or M4 and M5;  $V_t$  is the threshold voltage. When we define the gate delay of a fast delay cell,  $T_s$ , and the number of delay cells in a chain,  $N$ , the input range  $T_{tda\_range}$  is

$$T_{tda\_range} = N \times T_s. \quad (3)$$

The TDA has 16 delay cells in each chain in this design, but it is possible to increase the input range by employing larger numbers of delay cells.

### C. Calculation of TDC Digital Code

The LSB of the proposed TDC,  $LSB_{total}$  is calculated by using the gate delay  $T_d$  of a differential inverter in the VCO as follows:

$$LSB_{total} = \frac{T_d}{G}. \quad (4)$$

$T_d$  can be expressed in terms of the frequency of the VCO,  $f_{vco}$ , as follows:

$$T_d = \frac{1}{f_{vco} \times 8} \quad (5)$$

where the factor 8 is a consequence of the fact that the VCO is composed of four differential inverters. Hence, the  $LSB_{total}$  becomes

$$LSB_{total} = \frac{1}{f_{vco} \times 8 \times G}. \quad (6)$$

The dynamic range DR (bit length) is calculated using the maximum counter value of the first TDC,  $C_{1st\_max}$ . Suppose that the frequency of each VCO in the first TDC and the second TDC is same, then

$$DR = \log_2(8 \times C_{1st\_max} \times G) \quad (7)$$

Fig. 6 shows the output code from the first and the second TDC. The time residue is amplified by the TDA and then digitized by the second TDC.  $N_{max}$  and  $N_{min}$  are the maximum and the minimum digital value by the second TDC when the time residue is maximum and minimum, respectively.  $N_{th}$  is a digital value for the time residue when the counter value of first TDC just changes. PDM is the phase of the first TDC when the time residue changes from minimum to maximum. The TDA gain,  $G$ , and  $LSB_{total}$  are calculated using  $N_{max}$  and  $N_{min}$  as follows:

$$G = \frac{N_{max} - N_{min}}{8} \quad (8)$$

so the  $LSB_{total}$  is rewritten from (6) with  $N_{max}$  and  $N_{min}$  as follows:

$$LSB_{total} = \frac{1}{f_{vco} \times (N_{max} - N_{min})}. \quad (9)$$

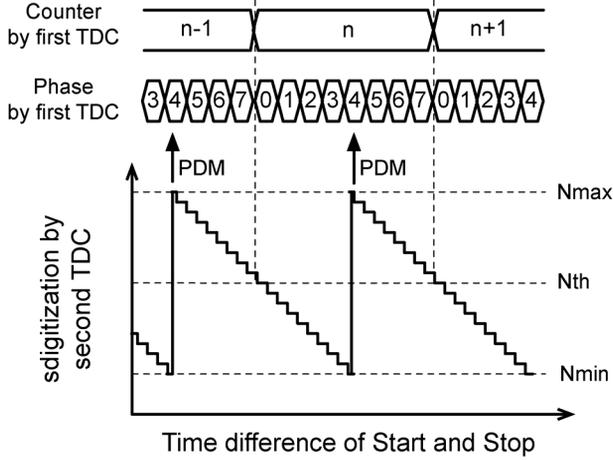


Fig. 6. Digital code calculation using outputs from the first TDC and the second TDC.

When the counter value and the phase from the first TDC are defined as  $C_{1st}$  and  $P_{1st}$ , the counter value and the phase from the second TDC are defined as  $C_{2nd}$  and  $P_{2nd}$ , the row digital code from the second TDC,  $D_{2nd}$ , is calculated as follows:

$$D_{2nd} = 8 \times C_{2nd} + P_{2nd}. \quad (10)$$

When the output codes from the first TDC and the second TDC are summarized,  $D_{2nd}$  should be modified to  $D_{2nd\_mod}$  because the counter and the time residue from the first TDC are not synchronized. Therefore,  $D_{2nd\_mod}$  is calculated as follows:

$$D_{2nd\_mod} = \begin{cases} N_{max} - D_{2nd} \\ + (N_{th} - N_{min} + 1), & (P_{1st} > PDM - 1 \ \& \ D_{2nd} > N_{th}) \\ N_{th} - D_{2nd}, & (\text{else}). \end{cases} \quad (11)$$

Finally, the TDC code,  $D_{total}$ , is calculated as follows:

$$D_{total} = C_{1st} \times (N_{max} - N_{min}) + D_{2nd\_mod} \quad (12)$$

where  $N_{max}$ ,  $N_{min}$ ,  $N_{th}$ , and  $PDM$  should be calibrated in advance.

#### D. Pixel Circuit

Fig. 7 shows the schematic of one pixel. A separate pixel is connected to each TDC. The pixel consists of a  $6\text{-}\mu\text{m}$ -diameter SPAD, a quenching transistor, a reset transistor, an off transistor, and a buffer to pulse-shape the output from the SPAD. A SPAD is a p+/deep n-well junction using p-well as a guard ring [1]. The breakdown voltage is 19.2 V [25]. The pixel circuit has both passive recharge and active recharge circuitries, controlled by signals VB and RST. The SPAD can be disabled by the OFF signal.

#### E. TDC Operation

Fig. 8 shows the timing diagram of the two-stage TDC. After RST is applied to reset the VCOs, the counters, and the phase detectors, the TDC is ready for the START signal. Upon arrival of the START signal, the VCO in the first stage TDC begins oscillating and the counter counts the number of cycles of the VCO.

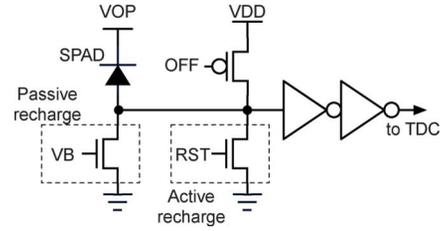


Fig. 7. Pixel structure.

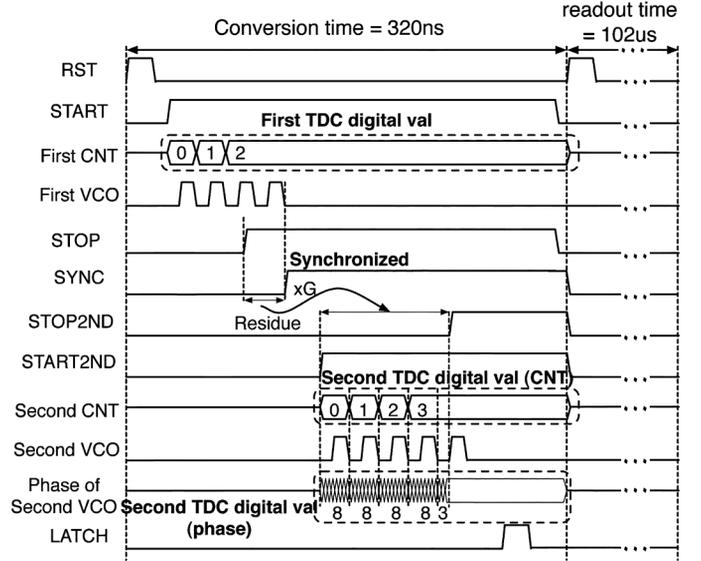


Fig. 8. Timing diagram.

SYNC, which is an output from synchronizer in Fig. 3, rises as it is synchronized with the second falling edge of the VCO after the STOP arrives. The inputs for the TDA are STOP and SYNC, and the time difference between STOP and SYNC is less than 1.5 clock cycles of the VCO because the synchronizer uses a dual-edge of the output from the VCO to reduce the maximum time residue. Thus, the time residue of the first TDC is larger than 0.5 clock cycles but smaller than 1.5 clock cycles. After amplifying the time residue, START2ND and STOP2ND operate in the second TDC as START and STOP in the first TDC. After completing the conversion, the digital data are latched by LATCH and read out by the first TDC output and the second TDC output multiplexer to the shift-register outside the TDC array after the address of the TDC is input. The output from the multiplexer is stored in the shift-register and read out 1 bit by 1 bit outside the chip. All control signals are generated by an FPGA and sent to the host PC through the FPGA. The host PC calculates the final digital codes. The conversion time is 320 ns, but it takes 102  $\mu\text{s}$  to read out all data because of the use of a 1-bit shift-register for readout.

## IV. MEASUREMENTS

#### A. Chip Implementation and Measurement Setup

We have designed and fabricated the proposed 128-channel column-parallel TDC using a high-voltage  $0.35\text{-}\mu\text{m}$  CMOS process [26]. Fig. 9 shows the microphotograph. Besides 128 TDCs, two dummy TDCs were also added to ensure edge

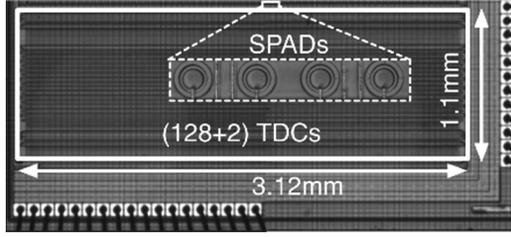


Fig. 9. Chip microphotograph.

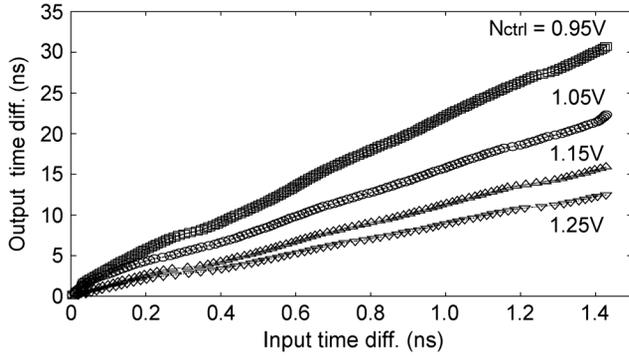


Fig. 10. TDA input-output measurement result.

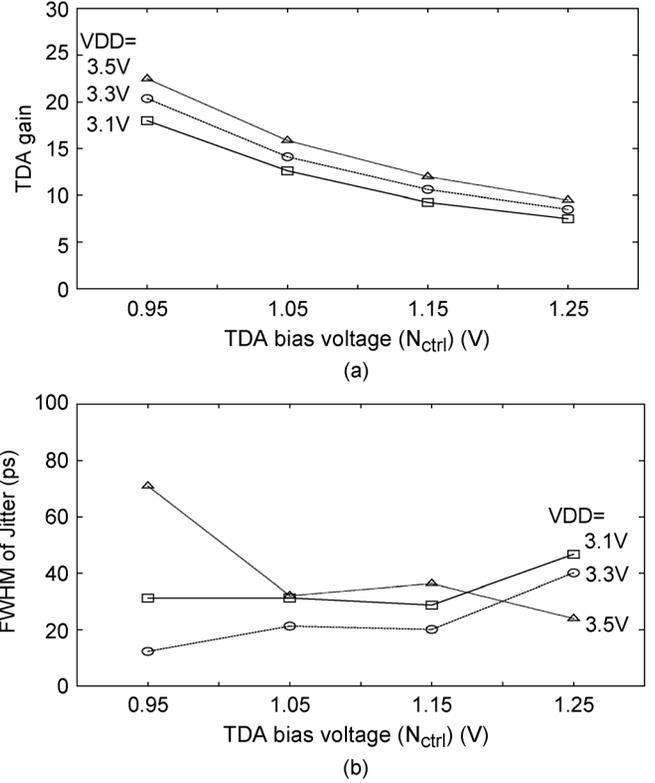
uniformity, and one SPAD [1] is connected to each TDC, thus minimizing parasitics and propagation time between SPAD and TDC. The TDC, including the readout multiplexer, occupies  $24 \times 1100 \mu\text{m}^2$ , of which the first and the second TDC occupy  $24 \times 130 \mu\text{m}^2$ , the TDA  $24 \times 550 \mu\text{m}^2$ , and the readout multiplexer  $24 \times 300 \mu\text{m}^2$ . The total size of the TDC array, including dummies, is  $3.12 \times 1.1 \text{ mm}^2$ . The printed circuit board (PCB) for the TDC array chip is connected to a Xilinx ML507 board. The embedded Virtex 5 FPGA generates control signals and receives outputs from the TDC array chip, and then communicates with the PC used for data acquisition over Ethernet.

### B. TDA Characterization

Fig. 10 shows the measurement of the relation between the input time differences and the output time differences in a TDA as a function of bias voltage. The gain changes from 8.5 to 21.6 as the TDA bias voltage,  $N_{\text{ctrl}}$ , changes from 1.25 to 0.95 V following (2). Fig. 11(a) shows the summary of TDA gain in each  $N_{\text{ctrl}}$  with three power supply voltages: 3.1, 3.3, and 3.5 V. When the power supply voltage changes, by  $\Delta V$ , the gain changes as follows:

$$G(T) = 1 + \frac{\beta_f(V_{dd} + \Delta V - V_t)^2}{\beta_s(V_{N_{\text{ctrl}}} - V_t)^2}. \quad (13)$$

Fig. 11(b) shows the jitter of a single TDC introduced by the TDA. This measurement was carried out by iterating the same measurements using the identical input time difference between the external electrical START and the STOP signal generated by the FPGA. This measurements include the input signals jitter and jitter caused by the first TDC and the second TDC. The measured jitter indicates the SPAD's single-shot precision, which

Fig. 11. (a) TDA gain changes by  $N_{\text{ctrl}}$ . (b) TDC jitter changes by  $N_{\text{ctrl}}$ .

shows the timing accuracy for a single measurement. The measurement shows that the jitter does not increase even if the gain increases, though the jitter is worse when decreasing the power supply voltage from nominal (3.3 V) at 0.95 V  $N_{\text{ctrl}}$ . This result means the jitter of input signal or the jitter caused by the first TDC is small, if compared to the intrinsic jitter of TDA itself.

### C. TDC Characterization

We measured one TDC to characterize the LSB, DNL, and INL as a function of TDA bias voltage,  $N_{\text{ctrl}}$ , and power supply at room temperature. Fig. 12 shows the measurement results of the density test to acquire DNL and INL when the input range is 29.3 ns; the SPAD is used to generate random START signals for the TDC [27]. According to the DNL/INL measurement, the number of digital codes increases by reducing  $N_{\text{ctrl}}$ . The LSB is thus smaller due to higher gain of the TDA as  $N_{\text{ctrl}}$  decreases, varying from 21.4 to 8.9 ps. The spurs of the DNL measurement occur when the time residue of the first TDC is close to minimum or maximum. The short period fluctuation of the INL measurement results from the TDA gain fluctuation against the input time difference to the TDA as shown in Fig. 10. Fig. 13 shows peak-to-peak INL error globally (whole input range) and locally (shortly fluctuated period from the one maximal to the next maximal) as a function of  $N_{\text{ctrl}}$ . The global peak-to-peak error increases as  $N_{\text{ctrl}}$  decreases according to the LSB, but the global peak-to-peak error does not vary appreciably. The reason is that the global error comes from the first TDC nonlinearity due to dynamical power supply noise. Therefore, we can see that the INL error of the TDA is independent of its gain.

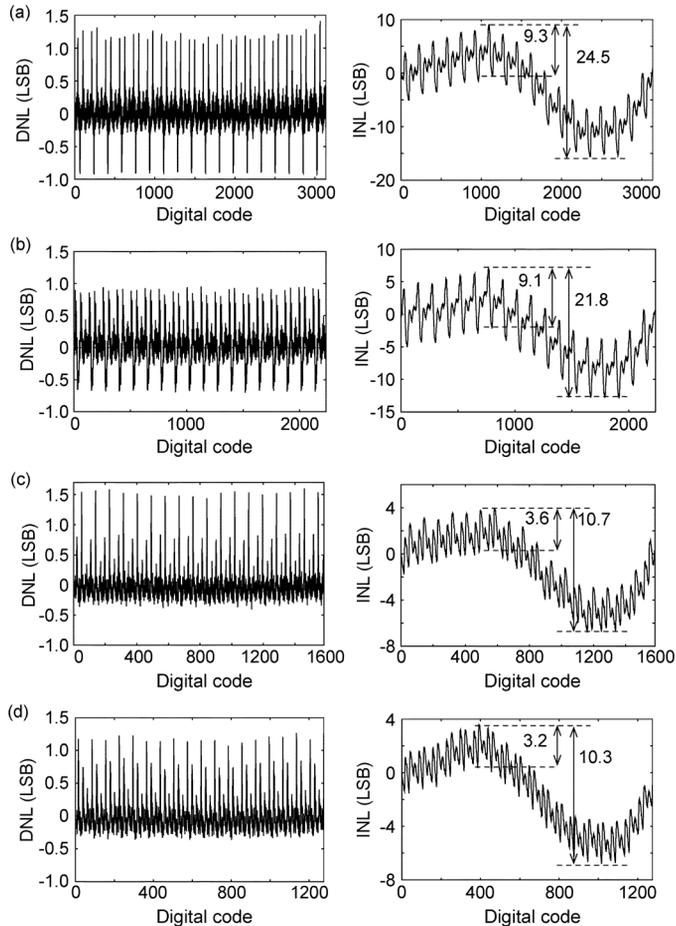


Fig. 12. Measured DNL and INL in  $N_{ctrl}$  of the TDA: (a) 0.95, (b) 1.05, (c) 1.15, and (d) 1.25 V.

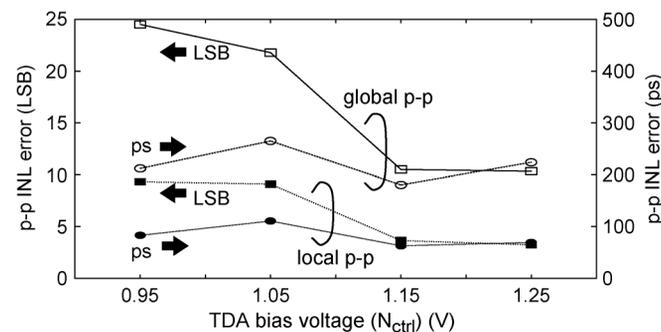


Fig. 13. Global and local INL error in each  $N_{ctrl}$  from the point of view of LSB and picoseconds (ps): Global INL error means a peak-to-peak value in the whole TDC input range, and local INL error means a peak-to-peak value in a periodic INL fluctuation.

#### D. Environmental Tolerance

As the TDA gain is dependent on power supply fluctuations, the TDC LSB also suffers from power supply and temperature fluctuations. Fig. 14 details such dependence. When the power supply voltage increases, both the frequency of the VCO and the TDA gain increase, so the LSB will decrease according to (6). Fig. 14(a) shows the measurement results when the power supply voltage changes from 3.1 to 3.5 V:  $+19.2\% / -13.7\%$

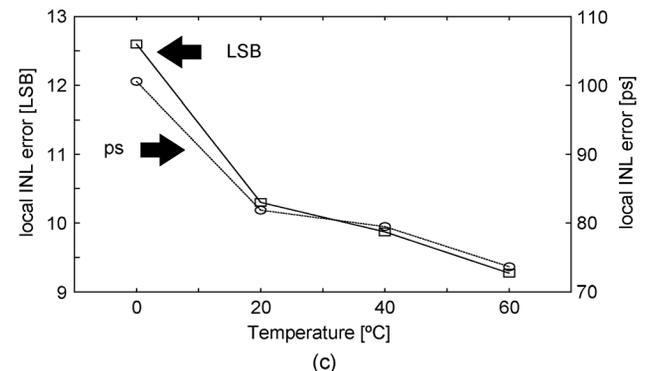
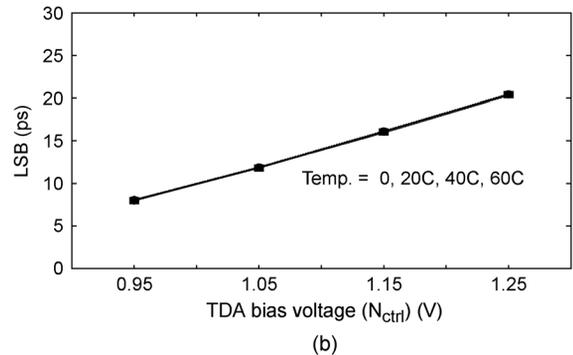
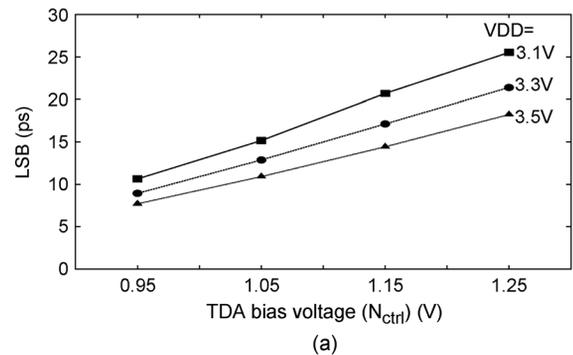


Fig. 14. LSB versus  $N_{ctrl}$ : (a) with  $\pm 0.2$  V power supply fluctuation; (b) with temperature fluctuation from  $0^\circ\text{C}$  to  $60^\circ\text{C}$  with  $20^\circ\text{C}$  step. (c) Local INL error varies in temperature.

and  $+19.3\% / -14.8\%$  in the  $\pm 0.2$ -V power supply voltage range when  $N_{ctrl}$  is 0.95 and 1.25 V, respectively. These variations can be reduced by calibrating the VCO frequency and the TDA gain using a lookup table made in advance or placing the VCO and TDA in phase-locked loops. For the calibration of the VCO frequency and the TDA gain by lookup table, we show the digital code distribution of 4 million hits when the input time difference is fixed to be 40 ns with 0.95 V of TDA bias voltage as shown in Fig. 15. Before calibration, the digital codes for each power supply voltage vary more than 15%, as shown in Fig. 15(a). When the digital codes are compensated by the lookup table, then the variation is about 1% as shown in Fig. 15(b). To reduce power supply fluctuation, one can also employ a CML logic delay cell instead of a CMOS inverter-type delay cell, as the TDA variable delay cell will reduce the influence of power supply fluctuations. This is due to the fact that the tail current controls the delay of fast and slow delay cells, hence the ratio of the two delays is decided independently of the

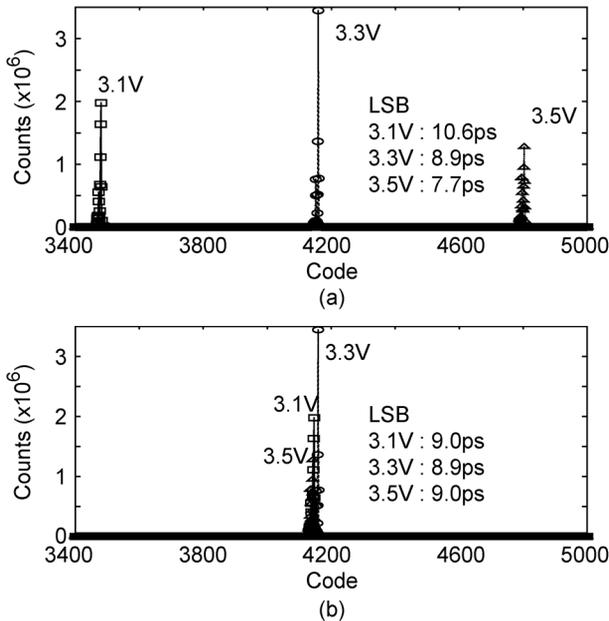


Fig. 15. TDC output code at 40 ns input time difference (a) without calibration and (b) with calibration.

power supply. The VCO could also be made tolerant to power supply fluctuation as shown in [28].

When one changes the temperature from 60°C to 0°C, the VCO frequency increases 5.6% faster. By the shift of the VCO frequency, the input range of the TDA becomes insufficient to cover the whole time residue from the first TDC. It means that the TDA cannot amplify time residue properly, so the gain also changes. As a result, the changes of the frequency are offset by the change of the TDA gain. Fig. 14(b) shows the temperature effects of the LSB from 0°C to 60°C. The local INL error increases 36% when the temperature changes from 0°C to 60°C as shown in Fig. 14(c). To cover the whole time residue, the number of delay cells in the TDA should be increased to increase the input range, and then the lookup table method can be utilized to compensate the LSB shift by temperatures.

### E. Uniformity Measurement Results

We measured the LSB variation on all 128 TDCs by means of the density test using SPADs for 1.25- and 1.15-V  $N_{ctrl}$ ; the gain is 8.5 and 12, so the LSB should be 21.4 and 17.1 ps, respectively. Fig. 16 shows the LSB variation. When  $N_{ctrl}$  is 1.25 V, the average of the LSB is 12.93 with 0.75 ps standard deviation corresponding to 5.8% LSB, and when  $N_{ctrl}$  is 1.15 V, the average LSB is 7.55 with 0.51 ps standard deviation corresponding to 6.8% LSB. The variation is due to the frequency variation of both VCOs in the first and the second TDCs, and of the gain of the TDA. The IR drop of the power supply voltage and  $N_{ctrl}$  are also another reason for the LSB variation because many TDCs operate at the same time, thus the actual LSB is lower than the predicted LSB. This behavior implies that the IR drop of the power supply voltage affects  $N_{ctrl}$  because the  $V_{ctrl}$  is generated by using the power supply voltage. From Fig. 14(a), we can estimate the IR drop of  $N_{ctrl}$  to be about 200 mV because

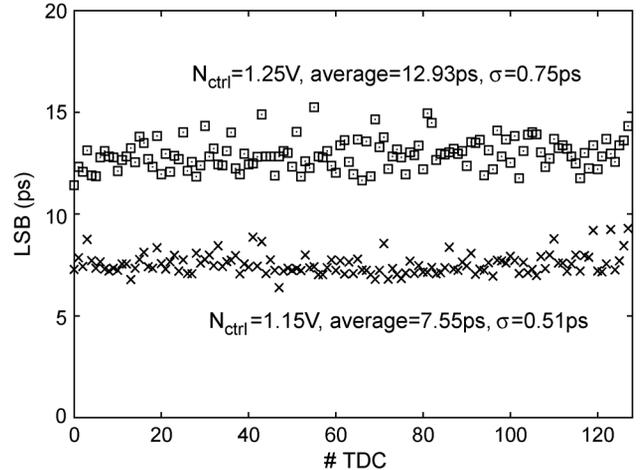


Fig. 16. LSB variation in 128 column-parallel TDC in 1.25-V  $N_{ctrl}$  and 1.15-V  $N_{ctrl}$ .

the LSB by this uniformity measurement at 1.25- and 1.15-V  $N_{ctrl}$  becomes close to the LSB characterized in a single TDC measurement at 1.05- and 0.95-V  $N_{ctrl}$ , respectively. However, The effects of the IR drop can be easily compensated for off-line since the number of TDCs that fired is known and a simple model of the IR drop can be built. However, they are negligible when the TDCs operate in photon-starved mode.

## V. CONCLUSION

We have proposed a 128-channel column-parallel two-stage TDC utilizing a TDA implemented in a 0.35- $\mu$ m CMOS process. The first stage operates as a coarse TDC, the time residue that is not converted in the first stage is amplified by a TDA, then converted by the second-stage TDC. As the gain of the time difference amplifier can be adjusted from 8.5 to 20.4, the time resolution of the TDC can be tuned from 21.4 to 8.9 ps. The time resolution variation due to PVT effects is  $\pm 5.8\%$  without calibration when the time resolution is 12.9 ps. We also shows the calibration technique for the VCO frequency and the TDA gain shift by power supply fluctuation, resulting in only 1% variation from 3.1 to 3.5 V.

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