A wide spectral range single-photon avalanche diode fabricated in an advanced 180 nm CMOS technology

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Abstract: We present a single-photon avalanche diode (SPAD) with a wide spectral range fabricated in an advanced 180 nm CMOS process. The realized SPAD achieves 20 % photon detection probability (PDP) for wavelengths ranging from 440 nm to 820 nm at an excess bias of 4 V, with 30 % PDP at wavelengths from 520 nm to 720 nm. Dark count rates (DCR) are at most 5 kHz, which is 30 Hz/μm^2, at an excess bias of 4V when we measure 10 μm diameter active area structure. Afterpulsing probability, timing jitter, and temperature effects on DCR are also presented.

OCIS codes: (040.0040) Detectors; (040.1345) Avalanche photodiodes (APDs); (040.6040) Silicon.

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1. Introduction

Single-photon avalanche diodes (SPADs) [1] are used as imaging devices in various fields, including 3-D vision [2,3], medical applications such as positron emission tomography (PET) [4], bio-imaging (fluorescence lifetime imaging microscopy or FLIM) citemegaframe. After Rochas succeeded in integrating SPADs in a standard CMOS technology [6], SPAD scaling has been promoted, achieving large integration [7–11], targeting future high-resolution 3-D vision chips or silicon photomultipliers with high energy resolution for PET applications. However, SPADs using an advanced CMOS technology (smaller minimum feature size than 0.18μm CMOS) tend to have photon detection probability (PDP) peaks at a small range of wavelengths [8]– [10], usually centered in the blue or green spectrum, because their multiplication region tends to be shallow. On the other hand, [11] shows an infra-red sensitive SPAD, but by burying the multiplication region this SPAD shows less sensitivity to blue light. However, some applications, such as fluorescence correlation spectroscopy (FCS), need high PDP in two or more wavelengths, so SPADs for these application should have a wide spectral range [12].

The Single Photon Counting Module (SPCM-AQR) from [13] can realize high PDPs at a wide spectral range when compared with SPADs using an advanced CMOS process. However, it is desirable to develop a SPAD with high PDP with a wide spectral range using an advanced CMOS process if one is interested in building large SPAD pixel arrays for highly integrated applications or SPAD with heavily integrated digital circuits.

In Section 2, the structure of the proposed SPAD is presented. Section 3 presents device measurements, including DCR's dependence on temperature, PDP, afterpulsing probability, and timing jitter. PDP measurement results are also compensated by inactive area using a technique introduced previously [14]. Finally, conclusions are given in Section 4.

2. SPAD structure

A conventional, blue or green sensitive SPAD structure is a P-type diffusion(P+) as a anode and N-type well(NWELL) or deep-well(DNEWLL) as a cathode, as shown in Fig. 1 (a) [8,9]. This structure's junction lies between P+ and NWELL/DNEWLL, and is generally quite shallow, say much smaller than 1 μm. Three regions contribute to the PDP. First, electrons in P+ will diffuse from P+ to the junction after absorbed light generates an electron-hole pair, possibly triggering an avalanche. Second, generated electrons or holes in the multiplication region may trigger an avalanche. Finally, generated holes by absorbed light in NWELL/DNEWLL also move from NWELL to the junction and may trigger an avalanche, but the impact ionization coefficient of holes is lower than that of electrons, with the PDP decreasing at longer wavelengths, because PDP is a function of the impact ionization coefficient and PDP will be lower as the impact ionization coefficient decreases. Furthermore, The impact ionization coefficient of electrons is higher than that of holes, so the peak of PDP will be biased towards shorter wavelengths of light, which generates carriers closer to the surface [6]. On the other hand, Fig. 1(b) shows an infra-red sensitive SPAD by burying the multiplication region [11], and achieve high PDP for longer wavelength because generated electrons in the deep may trigger the avalanche

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with high impact ionization possibilities. However, this SPAD shows less sensitivity to blue light. Figure 1(c) shows the structure of possibly wide spectral [10], but the substrate doping is too high, so the depletion region become small, which lead to poor PDP.

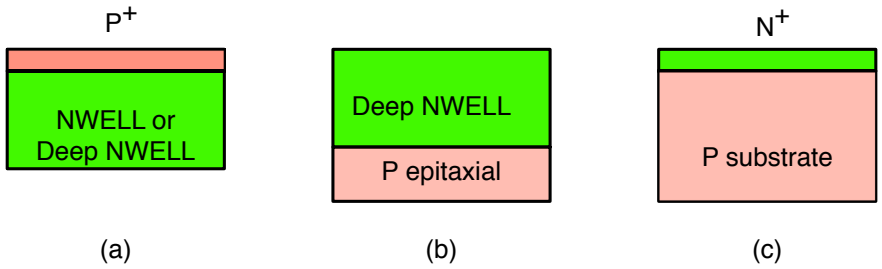

Fig. 1. Active area structure excluding guard ring region: (a) Conventional blue or green sensitive SPAD structure. (b) Infra-red sensitive structure. (c) Wide spectral structure.

Figure 2(a) shows the structure of the proposed SPAD. N-type diffusion(N^+) and P-type well(PWELL) are used as a cathode and anode of a SPAD, respectively, with NWELL comprising the 2 μm width guard ring around the 10 μm diameter active area. Between the contact to the anode and cathode, shallow trench isolation (STI) is generated. The multiplication region is below the junction between N^+ and PWELL. Below PWELL, a very low doped P-type epitaxial layer is fabricated on a P-type substrate. The PDP peak will be shifted to a longer wavelength when compared with blue-sensitive or green sensitive SPADs because photon-generated electrons in the PWELL are more likely to initiate an avalanche than if holes were used as in the standard structure. Furthermore, the doping value of PWELL is generally lower than that of P^+, so the drift of generated electrons in PWELL is longer than that in P^+. This implies that the PDP will have a wider spectral range because the thickness of PWELL is thicker than P^+. In the proposed diode, there is also a P-type epitaxial layer below the multiplication region, so generated electrons in the P-type epitaxial layer easily diffuse to the multiplication region the P-type epitacial layer is very low doped. As a result, we can implement wide spectral range sensitivity. The guard ring is for preventing edge breakdown due to higher electrical fields around the edge of the active area than that of the active area and give a uniform electrical field to the active area To verify this guard ring effect, we also simulate the device to observe the electrical fields in the active area and guard ring area, as Fig. 2(b) shows. The depletion region is generated below active area. The line shows the electrical field and the dark color means low electrical fields and blight color means high electrical fields. Besides active area, the NWELL is implemented as a guard ring, and the electrical fields around guard ring are lower than that of multiplication region. Note that the simulation doesn't include STI but the electrical field simulation does not necessarily need STI because the important region is near to active area to know if there is an edge breakdown or not. The basic structure itself is not new [10, 15, 16], but the SPAD is designed using an advanced 180 nm standard CMOS process, demonstrating the possibility for the large scale integration in the future.

When using the SPAD with transistors, there are two ways to implement avalanche sensing. One way is to connect the cathode to an excess bias voltage(V_e) via a quenching resistor, and connect the anode to the negative breakdown voltage($-V_{bd}$). In this case, deep NWELL must isolate transistors because the substrate will be a negative voltage. The other way is to connect cathode to the sum of an excess bias voltage and the breakdown voltage($V_e + V_{bd}$) via a quenching resistor, and connect the anode to ground. In this case, the output from the SPAD will be a high voltage modulated by V_e, so a coupling capacitance is required between the SPAD and

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transistors to shift the voltage to an acceptable range for transistors. In the present measurement setup, there are no transistors, only the SPAD and I/O PADs with huge parasitic capacitance and variable capacitance, connected to an oscilloscope. The variable capacitance is for changing the capacitance value connected to SPAD to measure the effect on an afterpulsing probability described later. Thus, V_e is applied via a quenching resistor to the cathode, and $-V_{bd}$ to the anode as shown in Fig. 2(c). Even if negative voltage is applied to the substrate, logic or buffers will not have a big effect except for higher leak current from deep NWELL to substrate as far as we can use deep NWELL. When the substrate should be grounded, the coupling capacitance will be necessary. However, metal-to-metal capacitance will be realized easier with high capacitance using a more advanced CMOS process than a mature CMOS process, because the metal-to-metal distance is closer. Then the circuit itself will be compact.

3. Measurement results

3.1. DCR measurement

Following fabrication in an advanced 180nm CMOS technology, the chip is packaged and then measured. The diameter of active area of the measured SPADs is 10μm. Each SPADs is connected to PADs directly. Unless noted, measurements are performed at room temperature.

The dark count rate (DCR) is measured by counting the number of avalanches while the SPAD is operating at an excess bias voltage above the SPAD's breakdown voltage. The DCR measurement is carried out in the dark condition where the chip is shielded completely not to receive any light. Three chips are available for the measurement and all three chips work as a SPAD. The SPAD's anode is connected to a high performance oscilloscope (LeCroy 8600A) to count DCR. The average breakdown voltage of a SPAD is 19.7 V, and excess biases ranging from 0.5 V to 4 V are applied with a 0.5 V step. Figure 3 shows the DCR measurement results of three 10 μm diameter SPADs. As shown in Fig. 3(a), DCR increases with the excess bias due to the trap-assisted tunneling and band-to-band tunneling carrier generation. The chips' DCRs vary from 0.252 kHz to 5.06 kHz (3.21Hz/μm^2– 64.5Hz/μm^2) and from 0.5 kHz to 13.7 kHz (6.37 Hz/μm^2– 175 Hz/μm^2) at 2 V and 4 V excess bias, respectively. CHIP 2, which has the median DCR, shows a DCR density of 10.8 Hz/μm^2 at 2 V excess bias and 30.6 Hz/μm^2 at 4 V excess bias. DCR is varied a lot if you use sub-180 nm CMOS process because of process variation, but it is possible to disable these SPAD with high DCR by circuit technique with the memory embedded with SPAD in each pixel, if noisy DCR SPADs are not arrowed. Figure 3 shows the DCR temperature dependence of CHIP 3. As temperature increases, the DCR increases exponentially between -20 °C to 60 °C because of Shockley Read Hall (SRH) thermal generation [6].

3.2. PDP measurement

To measure the sensitivity of the SPAD, the light from a monochromator (Oriel/Newport part 77250) was projected into an integration sphere (Oriel/Newport part 819D-SL-2) with a reference diode (Hamamatsu part S1226-BQ) at one port of the sphere and the SPAD at the other. By the integration sphere, the amount of photons is same for reference diode and the SPAD, and by decreasing the intensity of the light source, the SPAD works with single-photon regime.

A SPAD's sensitivity to incident photons is characterized by the photon detection probability (PDP), that quantify the probabilities that a photon impinging on the detection triggers a digital response. When the PDP is measured, the afterpulsing which is an unwanted avalanche triggered by trapped carriers released during the SPAD's recharge should be negligible not to overestimate the PDP. It means that the deadtime of the SPAD, which is the time to restore the anode voltage to the excess bias after the SPAD has an avalanche, is set to be long by using high quenching resister, typically 500 kΩ.

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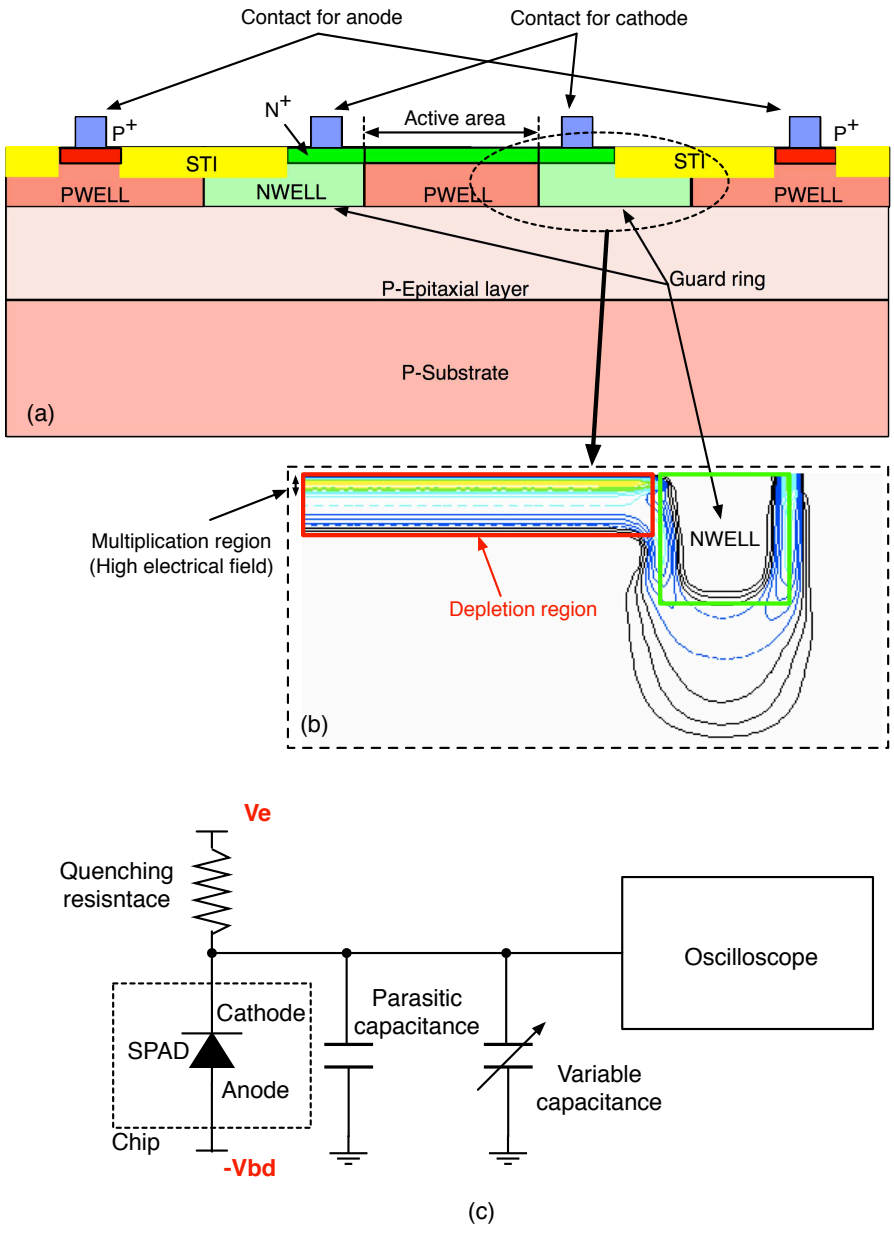

Fig. 2. (a) SPAD strucuture. (b) Simulation result of electrical fields. (c) Measurement setup.

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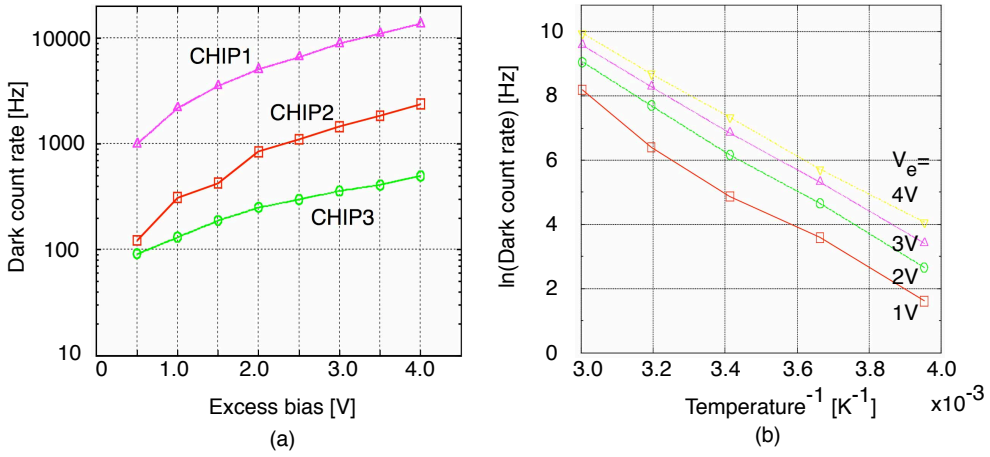

Fig. 3. DCR measurement results of 10μm diameter SPADs: (a) Excess bias dependence. (b) Temperature dependence.

Figure 4(a) shows a light emission test (LET) measurement results at 4 V excess bias [14] to check that the SPAD works properly and no edge breakdown. The light intensity varies inside the active area, which means that the breakdown voltage varies point-to-point inside a SPAD because there is process variations. Then, point-to-point PDPs should vary inside a SPAD and our PDP measurement cannot tell each point PDP. However average PDP as a single SPAD is most important for the almost application. Figure 4(b) shows the PDP measurement results as a function of wavelength. SPAD achieves 20 % PDP from 440 nm to 820 nm at 4 V excess bias, wider than previous work in advanced CMOS processes [11] and comparable with conventional products with wide spectral sensitivity [13]. A PDP of 30 % is also realized for wavelengths from 520 nm to 720 nm.

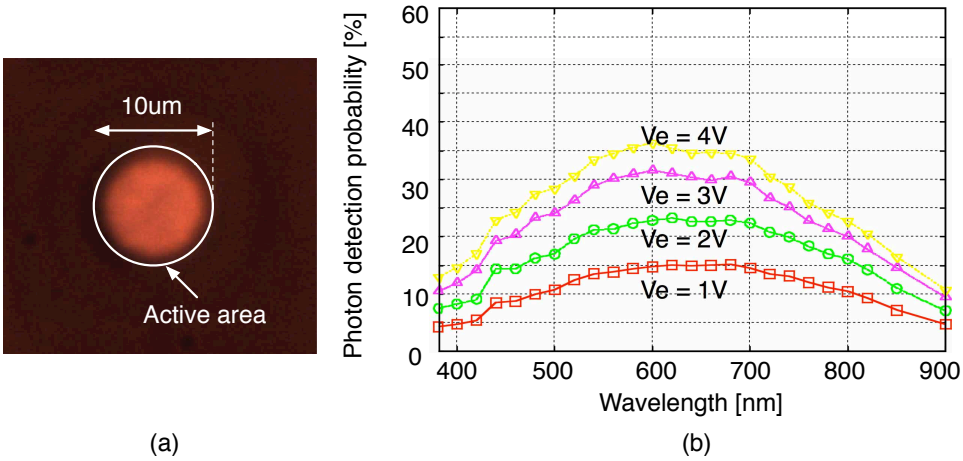

Fig. 4. PDP measurements from a 10 μm diameter SPAD: (a) Light-emission test. (b) PDP results.

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3.3. *Afterpulsing probability*

Under the constant light intensity, the distribution of times between a SPAD's avalanches, which is inter-avalanche time, should follow the poisson statistics. An afterpulse is an unwanted avalanche triggered by trapped carriers released during the SPAD's recharge time [1, 6]. As a result, a SPAD's count distribution for each inter-avalache time doesn't follow a pure exponential curve and the afterpulsing probability can be calculated by summing the counts in an inter-avalanche time histogram above an exponential line fitted to infinite inter-avalanche times, or in practice larger than a value of roughly 25 µs, as shown in Fig. 5(a). Then the afterpulsing probablity is calculated by dividing the summed counts above the fitted exponential line by the total counts until 25 µs.

The afterpulsing probability was measured for the proposed SPADs with two kinds of quenching. Because the SPAD is connected to pads directly, the parasitic capacitance is quite large. When the parasitic capacitance is large, a large number of carriers flow through the SPAD during an avalanche. The afterpulsing probability is a function of the number of change carriers in the pulse from SPAD [6]. Hence, large capacitances cause high probability of secondary avalanches. Figure 5(b) shows the measurement result of the afterpulsing probability with two kinds of quenching mechanisms at 3 V of excess bias. As is shown, the afterpulsing probability decreases as the quenching time increases or the rise time decreases. The rise time is defined as the time required for the response to rise from 10% to 90% of its final value. Comparing the afterpulsing probability at 750 ns deadtime, the probability at 20 ns rise time is about 20 % lower than at a rise time of 110 ns. Theoretically, the afterpulsing probability is proportional to the parasitic capacitance. The parasitic capacitance in our setup is around 10 pF because the capacitance of PAD and bonding wire is dominant that that of SPAD itself, but the parasitic capacitance will be less than 100 fF because the gate capacitance of an inverter or a comparator is only few femto farad. Therefore the afterpulsing probability is expected to be decreased dramatically when integrated inverter or comparator is implemented, and then negligible afterpulsing will be realized with shorter deadtime than 1 us.

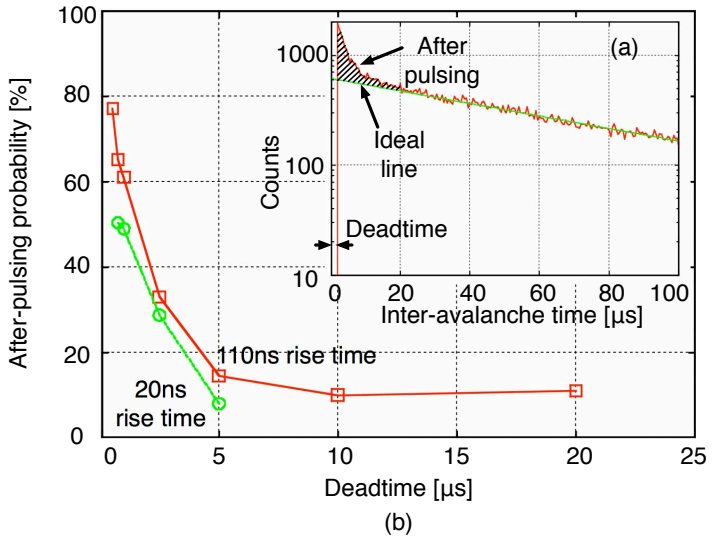

Fig. 5. (a) Counts in each inter-avalanche time. (b) Afterpulsing probability.

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3.4. *Timing jitter*

Timing jitter of SPADs is the uncertainty of the time interval between the arrival time of the photon at the SPAD and the time when the pulse is generated. Timing jitter is important to time-correlated applications, like 3-D vision and FLIM. To evaluate the timing jitter, the SPAD is illuminated by a picosecond laser diode source emitting 34 ps pulses at 40 MHz repetition rate with 405nm of wavelength and 100 MHz repetition rate with 790 nm of wavelength (Advanced Laser Diode Systems GmBH, Berlin, Germany). The laser intensity is quite strong, so the neutral density filter (NDF) is inserted between the laser and the SPAD non-perpendicularly to the laser light to prevent multiple reflection between NDF and the laser, as shown in Fig. 6(a). The time interval between the trigger from the laser and the rising edge of the pulse from the SPAD was measured using the high performance oscilloscope (LeCroy 8600A). By iterating this measurement, a histogram of the time interval is created by way of the time-correlated single photon counting (TCSPC) technique. The timing jitter for a 405nm of wavelength and a 790nm of wavelength are shown in the plot of Figs. 6(b) and 6(c), respectively. Each laser has own specific fixed delay from the laser trigger to the laser output, so the time intervals are also shifted individually. At 2 V of excess bias, the timing jitter including laser and detector jitter, at full-width-half-maximum (FWHM) was measured to be 334 ps and 316 ps at 405 nm and 790 nm of wavelength, respectively, but at 4 V of excess bias, the timing jitter at FWHM was 182 ps and 165 ps at 405 nm and 790 nm of wavelength, respectively. The jitter increase clearly as wavelength increase when the depletion region is shallow and compact. However, when the depletion region is wide, the timing fluctuation by a carrier to cross the wide depletion region will be dominant in the timing jitter because a chance to impact ionize is distributed. As a result, the timing jitter will be worse even if you use a blue laser.

Summary on the performance of the measured SPAD and comparison with other SPAD using advanced CMOS processes are shown in Table 1.

Table 1. Performance Summary and Comparison

Parameter	Our work	[8]	[9]	[10]	[11]
Breakdown voltage [V]	19.7	9.4, 12.8	14.4	10.4	14.9
DCR					
V_e [V]	2	2	1.4	0.13	2.4
Active area [μm^2]	78.5	58	50.3	45.3	32.2
Value [kHz]	0.252-5.06	0.22	0.025	8.1	0.1-10
PDP peak [%]	36 (600 nm)	36 (480 nm)	28 (500 nm)	12 (520 nm)	44 (690 nm)
PDP$>$20% [nm]	440-820	380-660	420-630	n.a.	500-850
PDP$>$30% [nm]	520-720	430-580	n.a.	n.a.	480-820
Afterpulsing probability [%]	50	$<$1	0.02	32	0.375
deadtime (ns)	750	180	100	1200	n.a.
FWHM timing jitter					
815nm laser [ps]			200(V_e=1.4 V)		
790nm laser [ps]	316 (V_e=2 V) 165 (V_e=4 V)				
637nm laser [ps]		128 (V_e=1 V)		398 (V_e=0.13 V)	
470nm laser [ps]			200 (V_e=1.4 V)		84 (V_e=2.36 V)
405nm laser [ps]	334 (V_e=2 V) 182 (V_e=4 V)			435 (V_e=0.13 V)	

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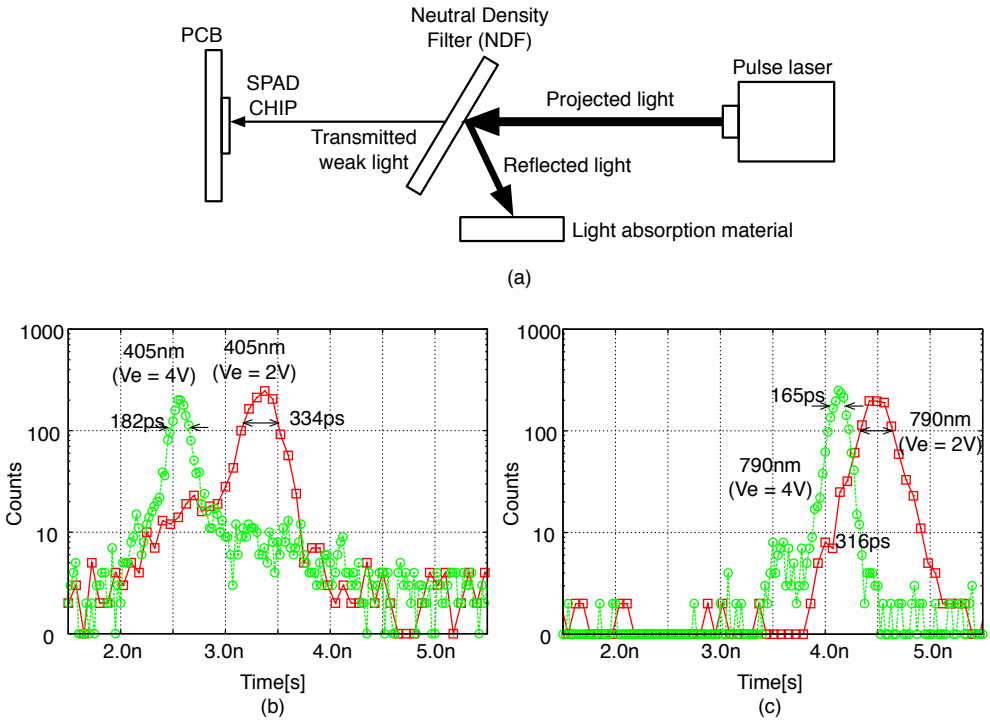

Fig. 6. Timing response: (a) Measurement setup. (b) Timing response for a 405nm of wavelength. (c) Timing response for a 790nm of wavelength.

4. Conclusion

A wide spectral range single-photon avalanche diode (SPAD) implemented in an advanced 180nm CMOS has been simulated, fabricated, and demonstrated. The SPAD achieves 20% PDP from 440nm to 820nm at 4V excess bias. 30% PDP is achieved over wavelengths ranging from 520nm to 720nm. Dark count rates of two SPADs are lower than 30Hz/μm^2 at 4V excess bias. Temperature effects for DCR, afterpulsing probability, and timing jitter measurement also have been characterised.

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